Integrated Systems Architectures

Lab 1: design and implementation of a digital filter Assignment

Read the Lab 1 description and address the following points.

1 Reference model development

- Design the filter with Matlab/Octave.
- Develop the fixed point model as a C program.
- Evaluate the THD (maximum allowed is -30dB).
- Compare and comment the results.

2 VLSI implementation

- Develop the VHDL model of the filter (direct-form for FIR filters and direct-form-II/canonical-direct-form for IIR filters) and verify it against the fixed point C model with a proper testbench.
  The results given by the VHDL model must be equal to the ones obtained with the C model.
  Show that the results of the VHDL model are correct (equal to the results of the C model) even when VIN moves from '1' to '0' and then back to '1'.
  Be sure that the interface of your architecture is exactly equal to the one shown in *es1v2.0_description.pdf* as an automtic tool will be used to check your design.
- Peform the logic synthesis → find the maximum clock frequency at which the design can correctly run (minimum period giving slack equal to zero). Then, find the area.
- Set $f_{clk} = f_M/4$, find the area, verify the design and estimate the power consumption.
- Place & Route the design at $f_{clk} = f_M/4$, find the area, verify the design and estimate the power consumption.

3 Advanced architecture development

Repeat all the step in 2