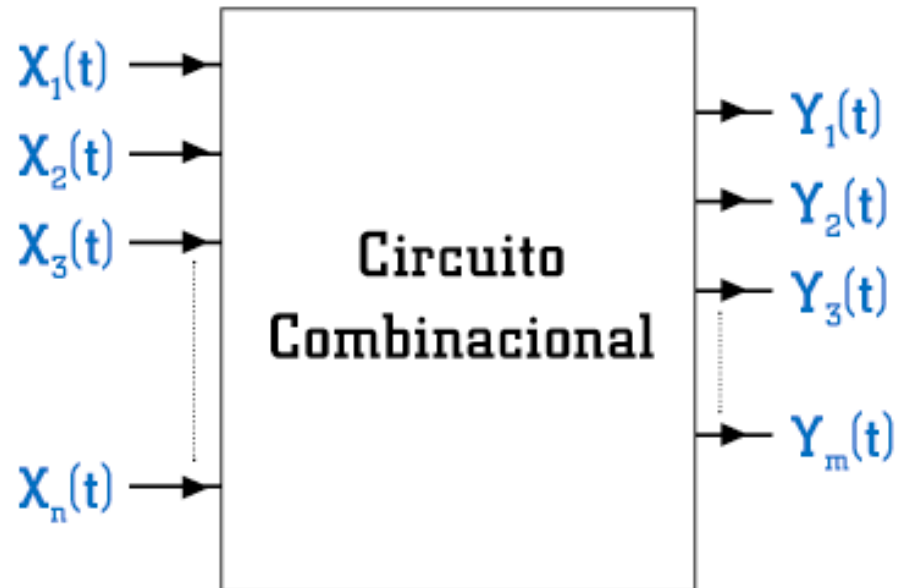


ANÁLISE DE CIRCUITOS SEQÜENCIAIS BÁSICOS

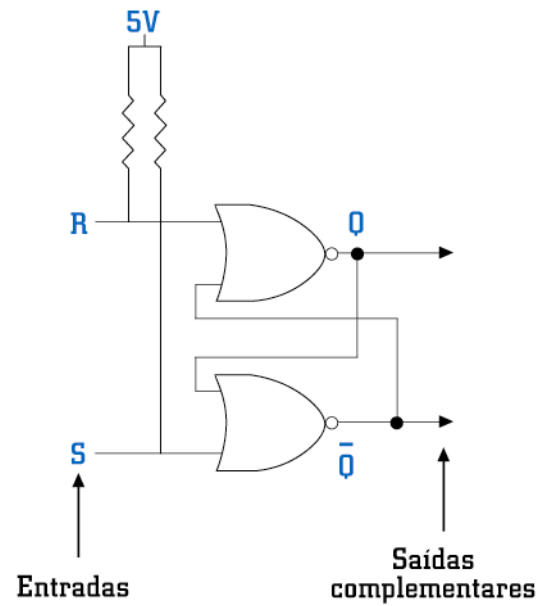
Objetivos

- Identificar e fazer a análise de circuitos seqüenciais.
- Identificar e usar os “latches” e os “flip-flops”.

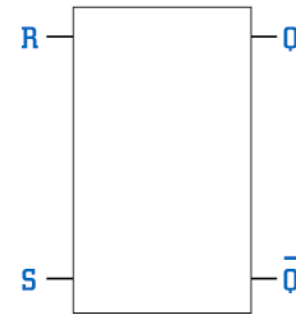


Circuito combinatorial típico.

"LATCH" RS



(a)



(b)

Entradas		Saídas	
R	S	Q	\bar{Q}
0	0	Não muda	
0	1	1	0
1	0	0	1
1	1	0	0

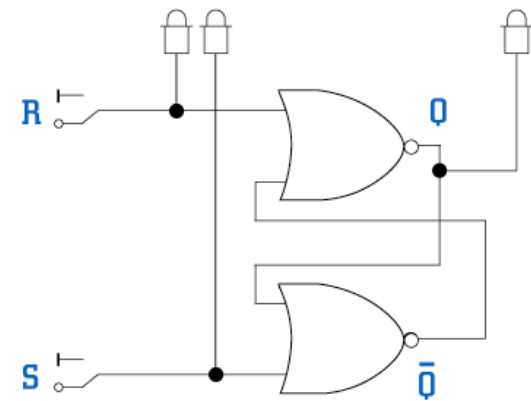
Região de operação

Indeterminado "latch"

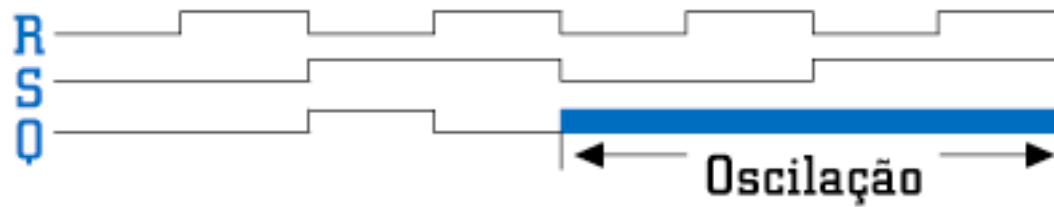
Erro lógico

Evitar

(c)



(d)



Instabilidade no “latch” RS.

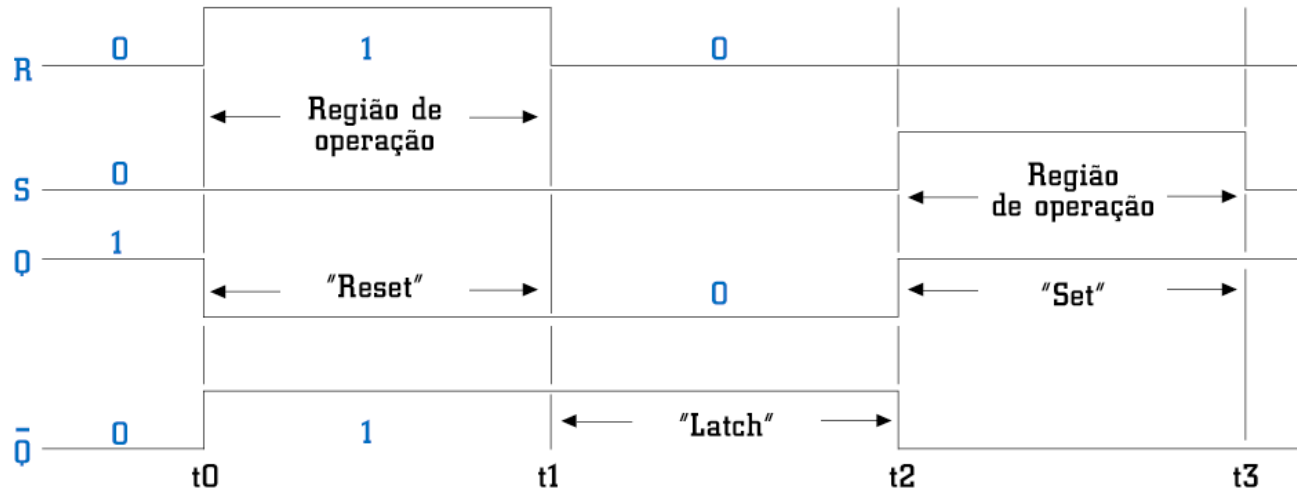
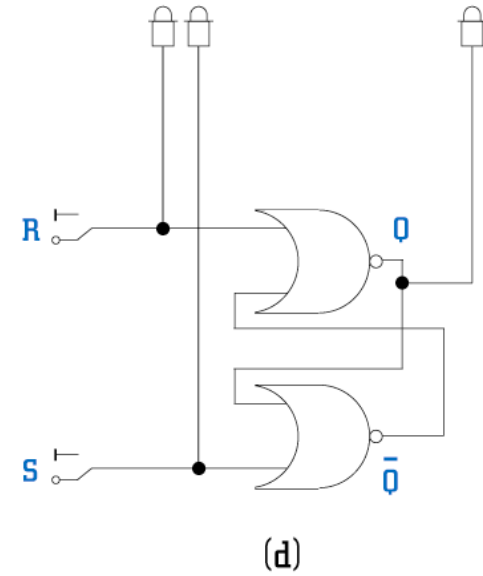
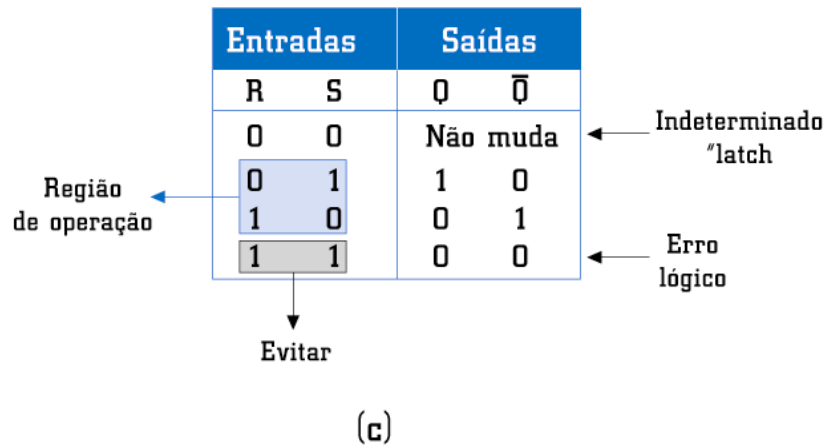
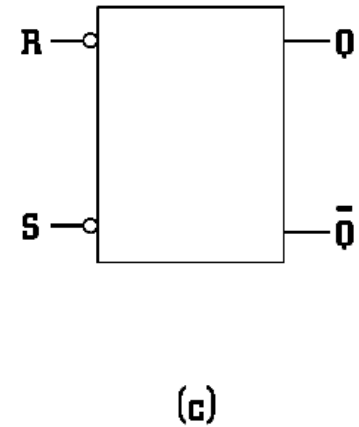
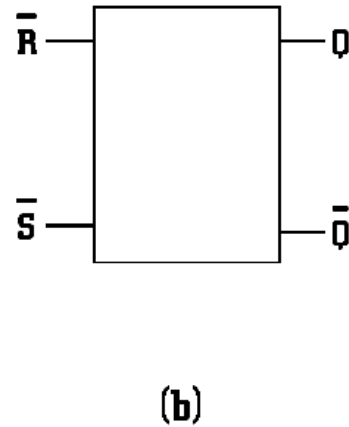
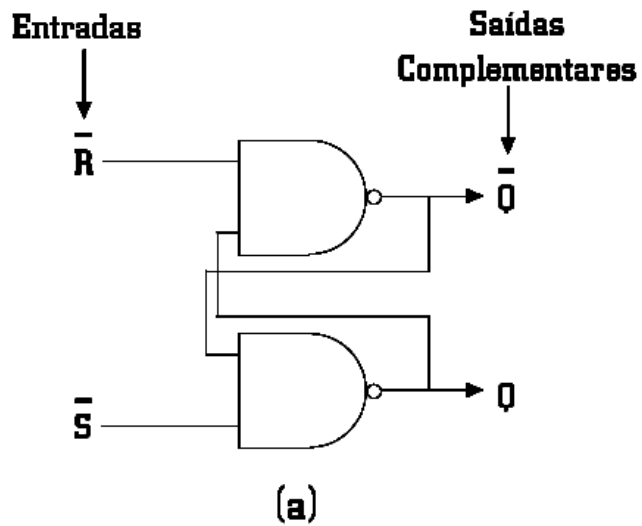


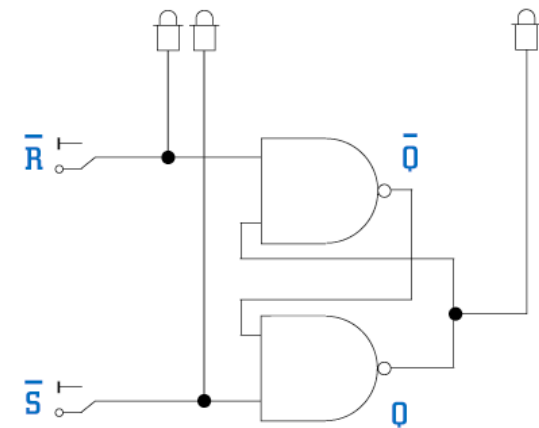
Diagrama no tempo do "latch" RS.



Entradas		Saídas	
\bar{R}	\bar{S}	Q	\bar{Q}
0	0	1	1
0	1	0	1
1	0	1	0
1	1	Não muda	

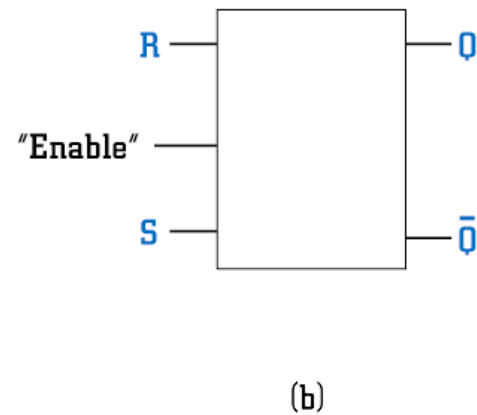
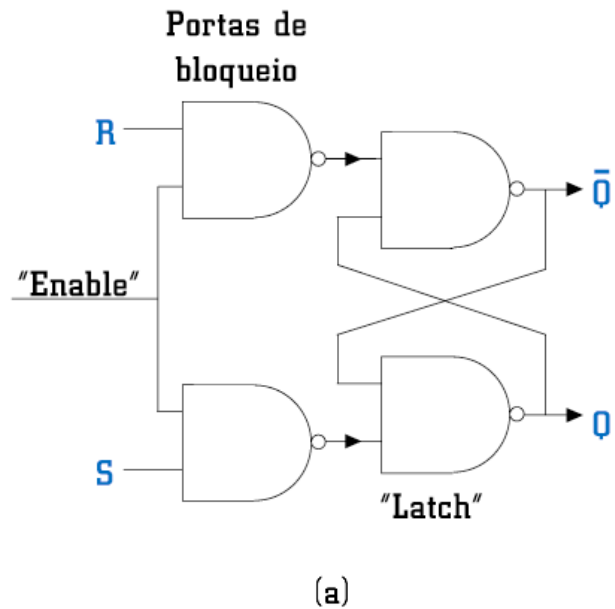
Evitar → (0, 0)
 Região de operação → (0, 1), (1, 0), (1, 1)
 Indeterminado - latch - (0, 0)

(d)



“Latch” RS com “NAND”; (b) e (c) Símbolos; (d) Tabela de combinações; (e) Sugestão para simulação.

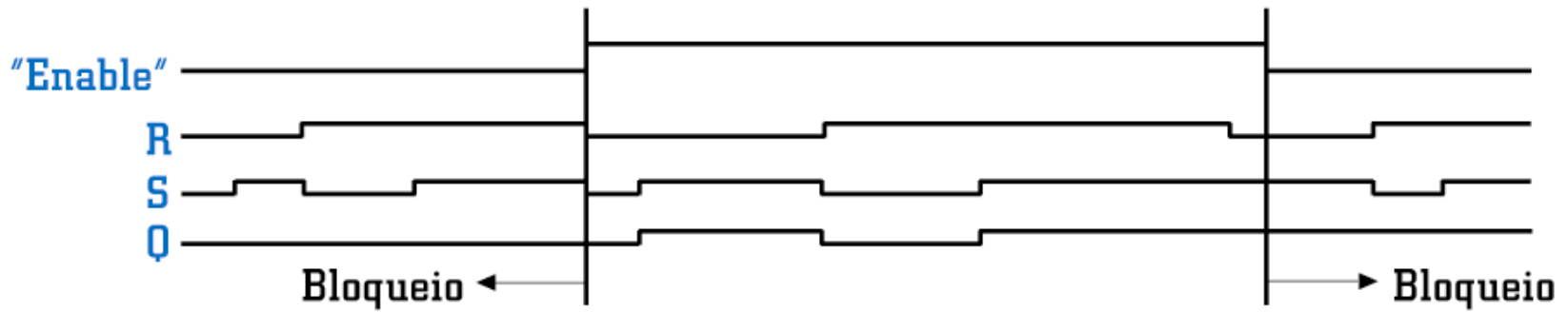
"LATCH" RS SÍNCRONO



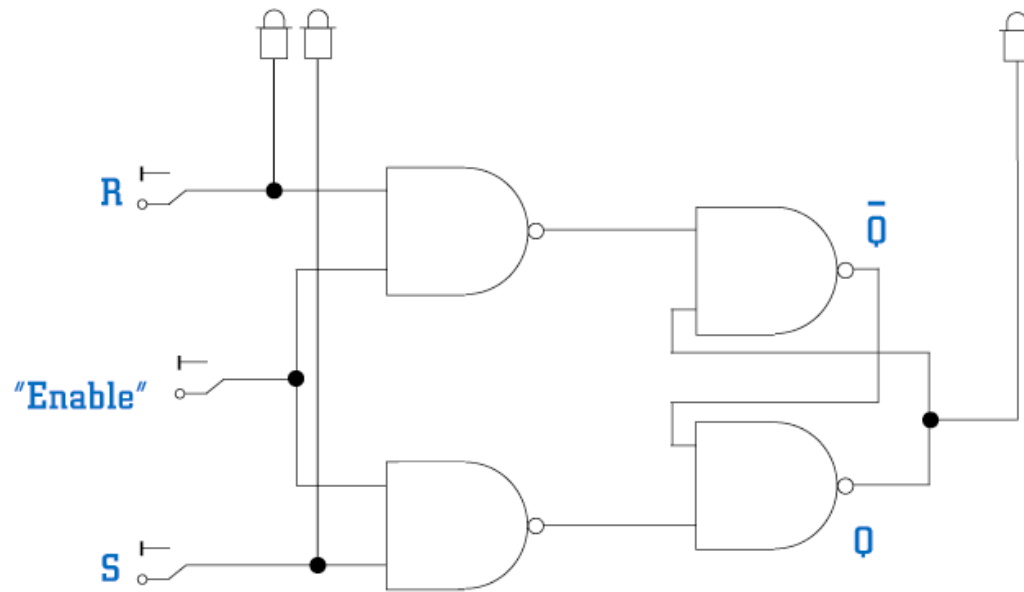
Entradas			Saídas	
"Enable"	R	S	Q	\bar{Q}
0	X	X	Não muda	
1	0	0	Não muda	
1	0	1	1	0
1	1	0	0	1
1	1	1	1	1

→ Bloqueio - "Latch"
 → Indeterminado

(c)



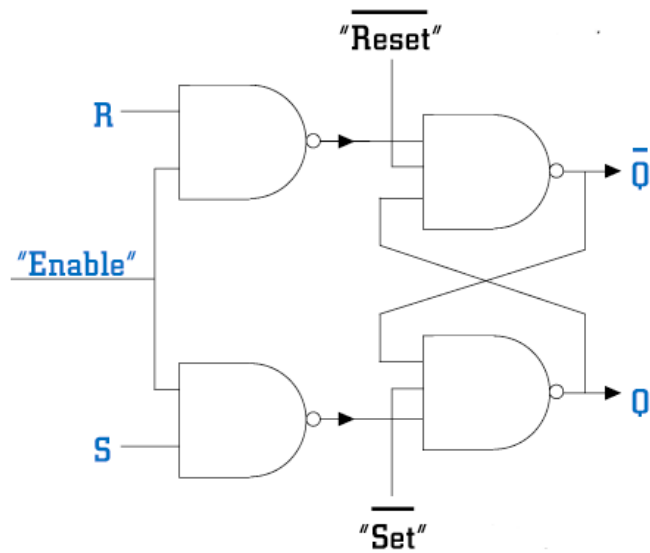
(d)



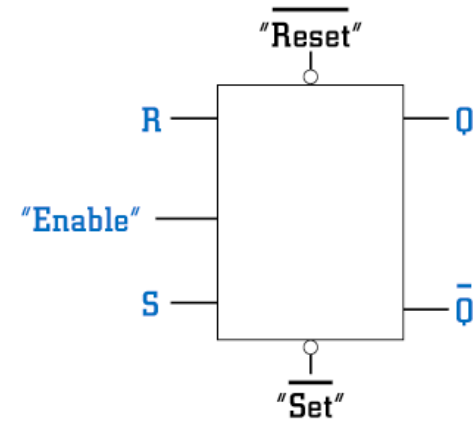
(e)

"Latch RS" Síncrono. (a) Circuito; (b) Símbolo; (c) Tabela de combinações; (d) Diagrama no tempo; (e) Sugestão para simulação.

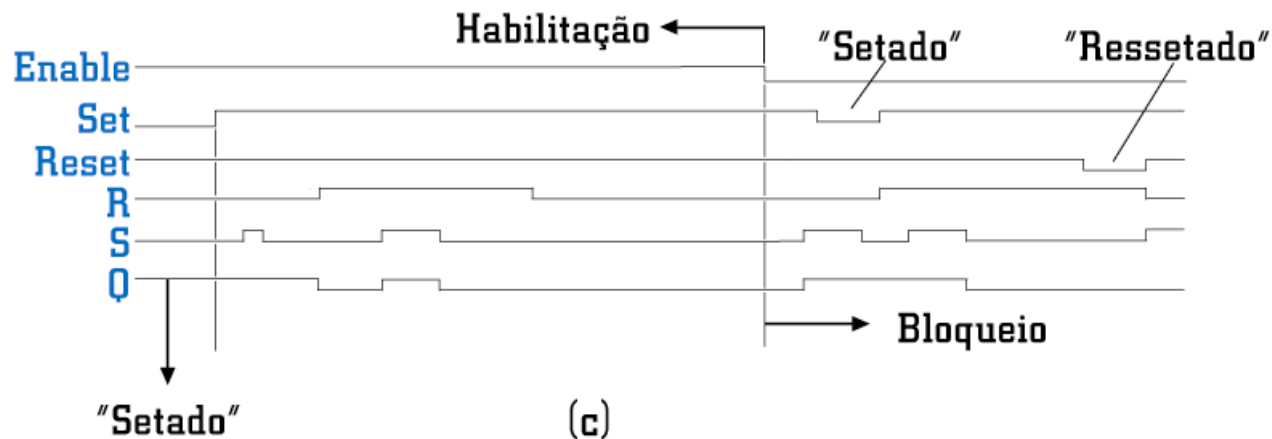
"Latch" RS com entradas diretas





(a)





(b)

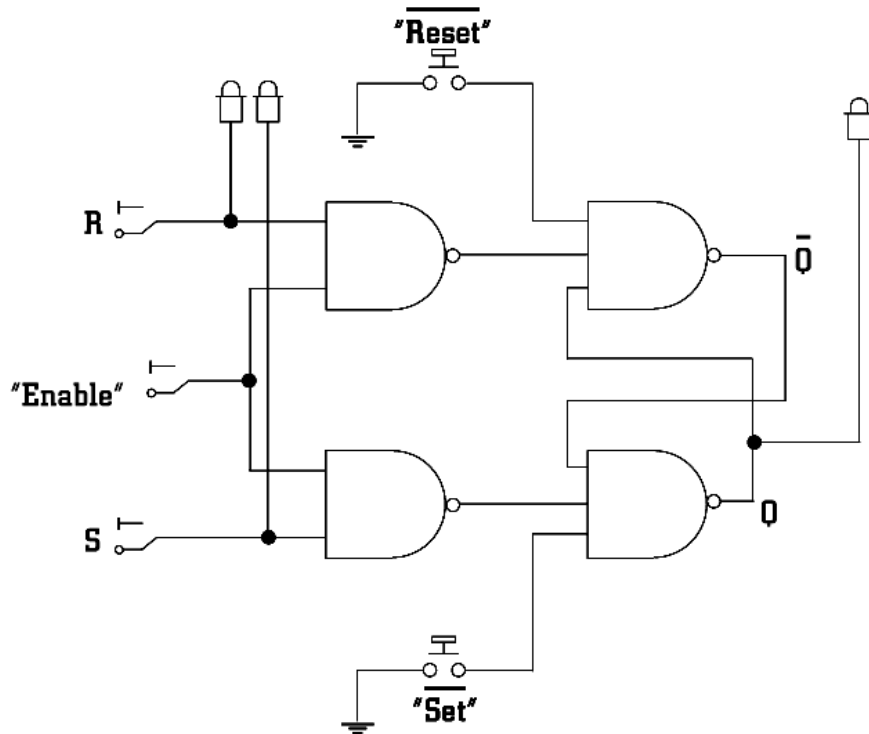


(c)

		Entradas			Saídas			
		"Enable"	"Set"	"Reset"	R	S	Q	\bar{Q}
Liberado		1	1	1	0	0	Não muda	
		1	1	1	0	1	1	0
		1	1	1	1	0	0	1
		1	1	1	1	1	1	1
Bloqueio		0		1	X	X	1	0
		0	1		X	X	0	1

 "Set"
 "Reset"

(d)



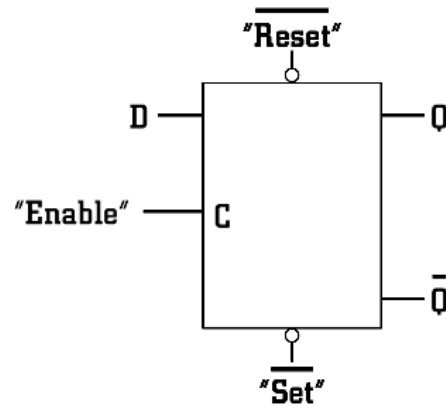
(e)

“Latch RS” Síncrono
com entradas diretas
(a) Circuito; (b)
Símbolo; (c) Diagrama
no tempo; (d) Tabela de
combinações; (e)
Sugestão para
simulação.

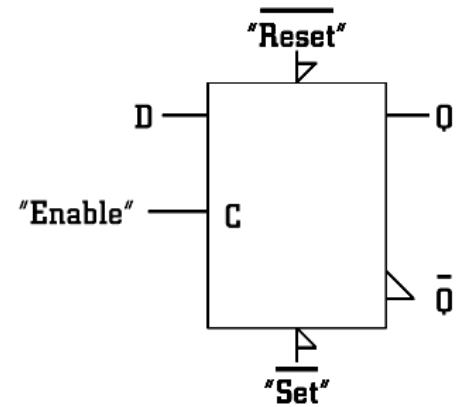
“LATCH” D

“Enable”	D	Q
0	X	Não muda
1	1	1
1	0	0

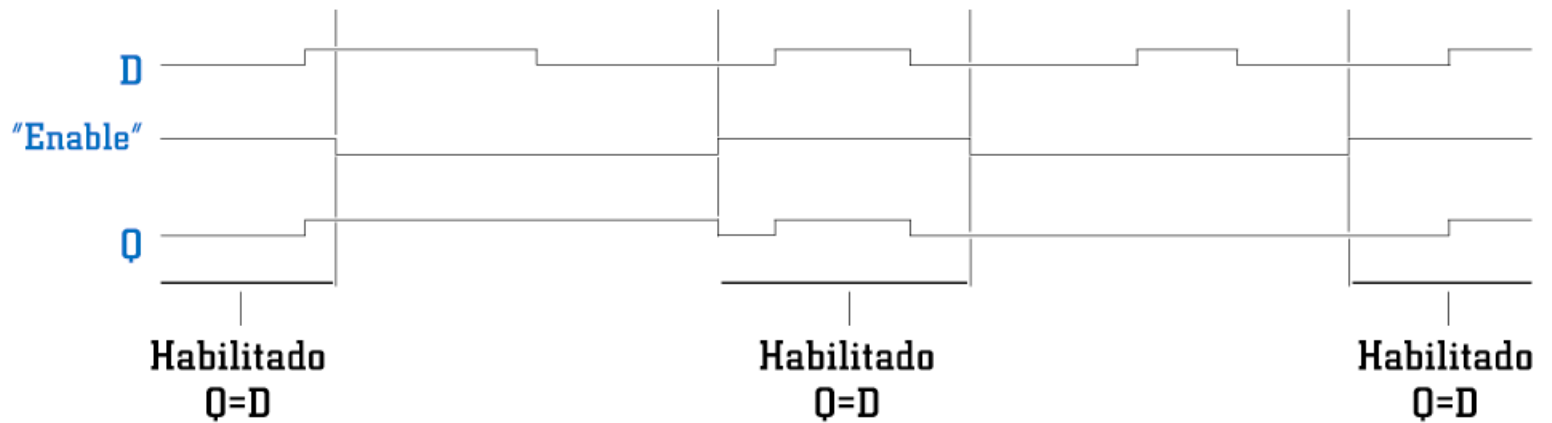
(b)



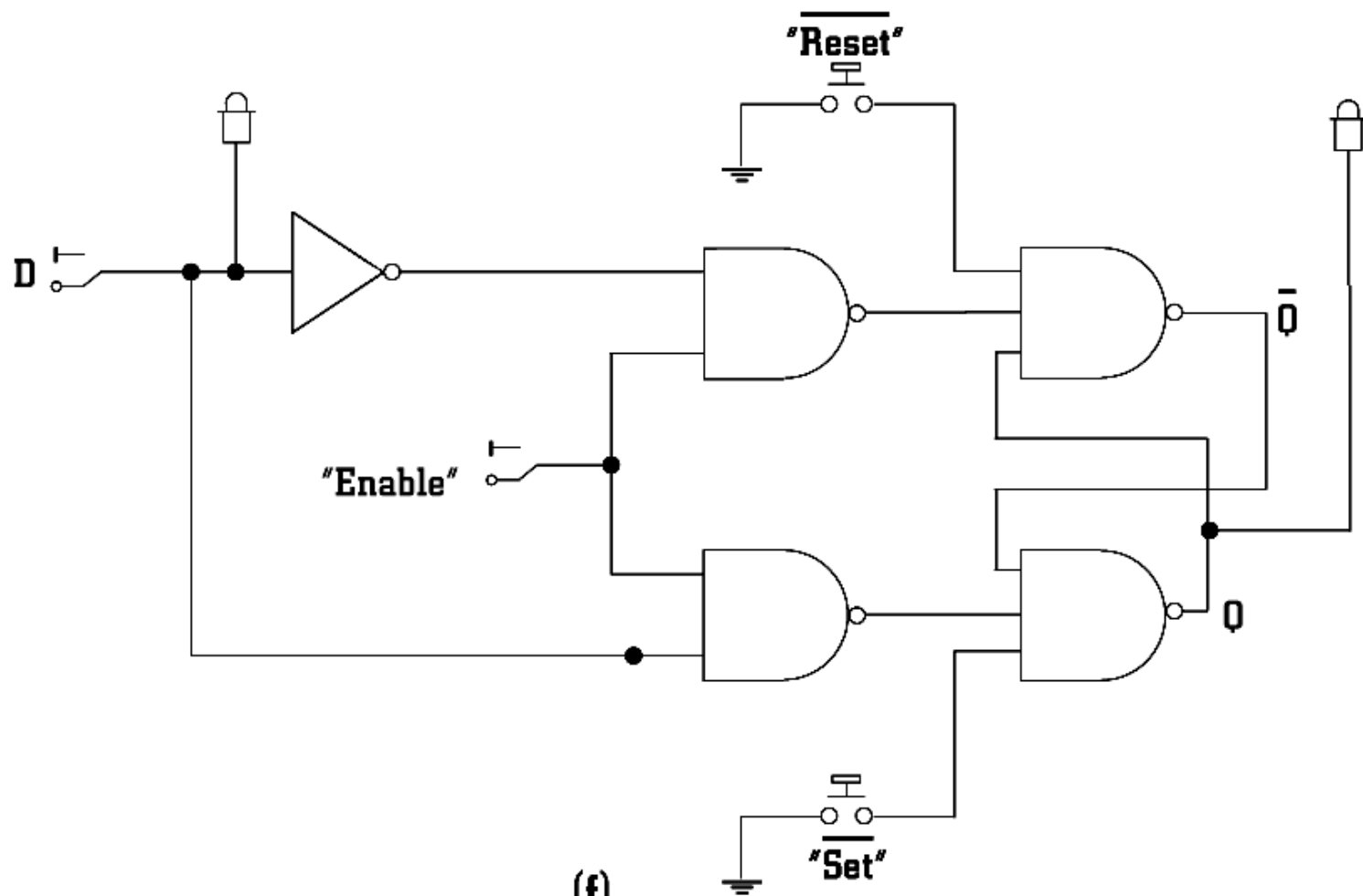
(c)



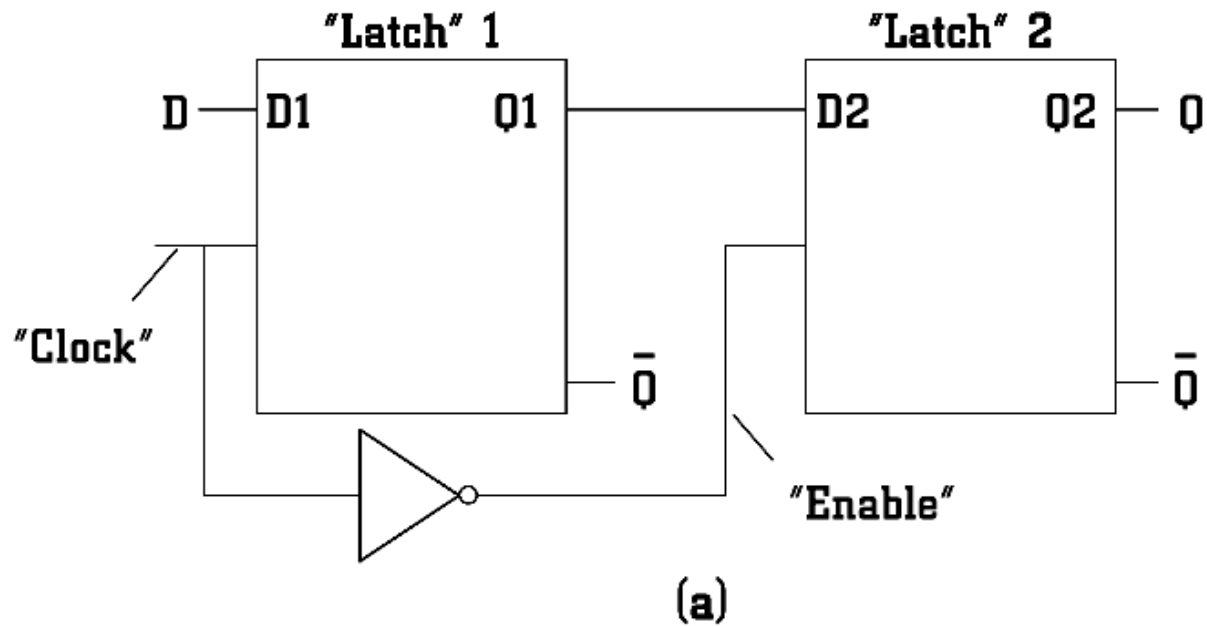
(d)



(e)

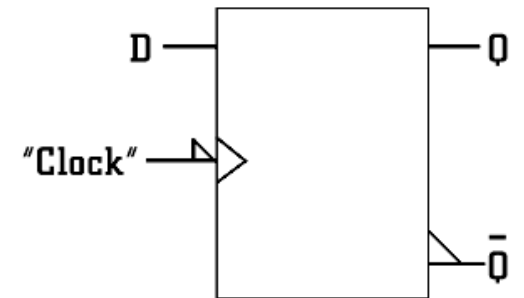
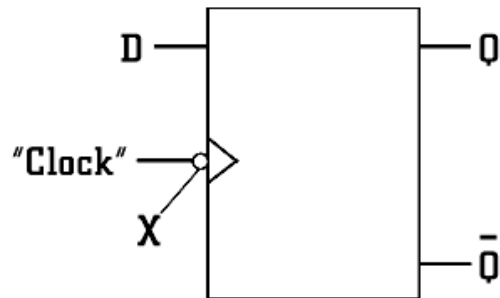


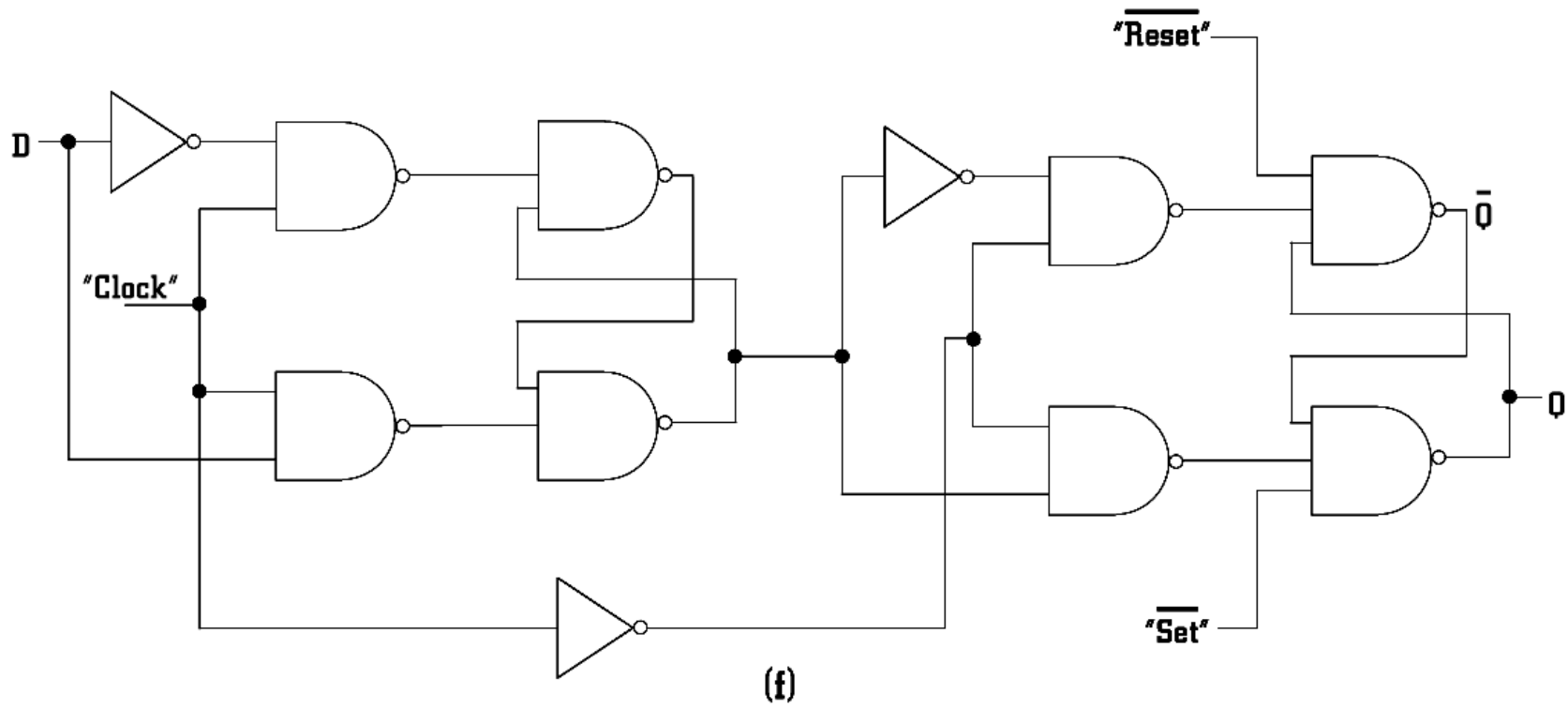
“FLIP-FLOP” D



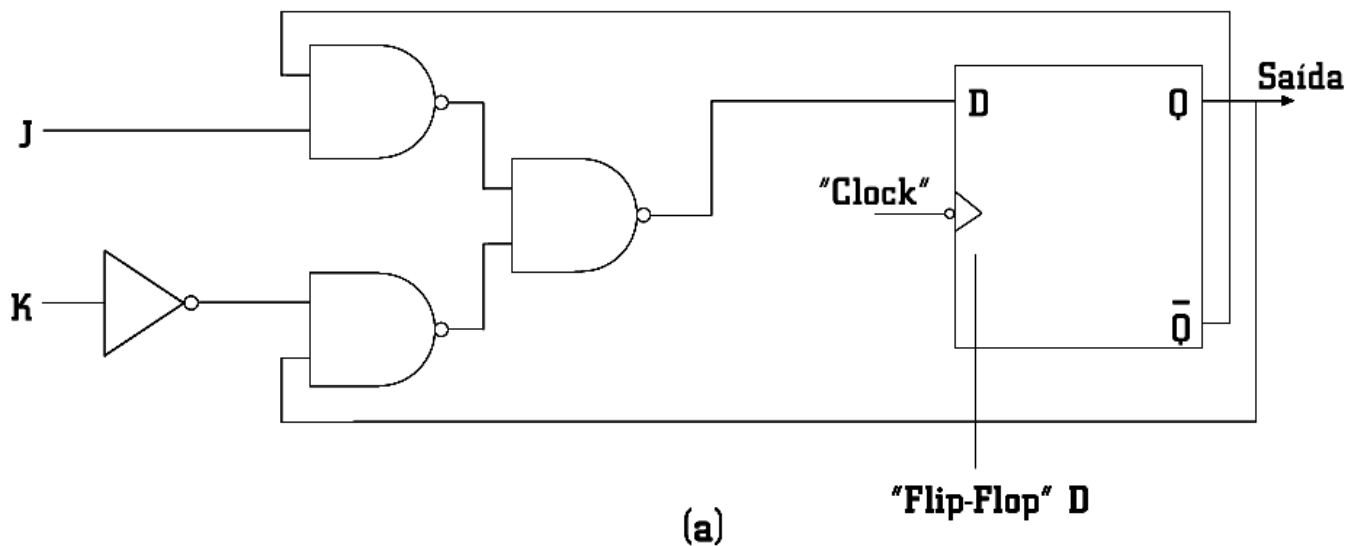
"Clock"	D	Q
↓	1	1
↓	0	0
1	X	Não muda
0	X	Não muda

(b)





"FLIP-FLOP" JK "EDGE-TRIGGERED"

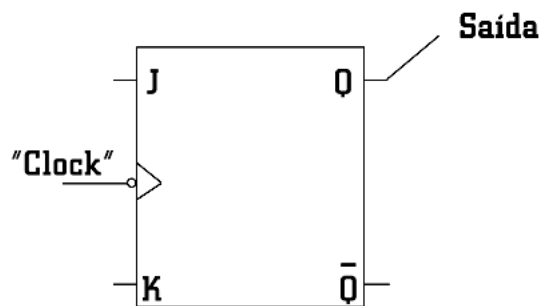


Entradas		Saídas
J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	\bar{Q}_n

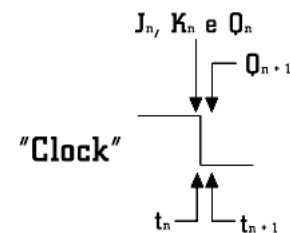
← Não muda

← Complementa

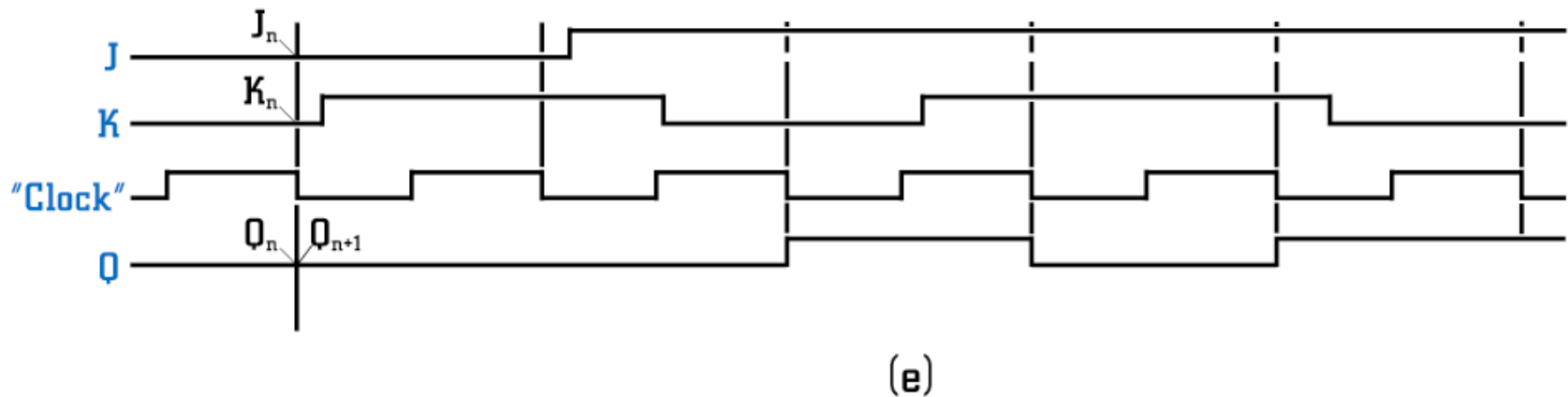
(b)



(c)

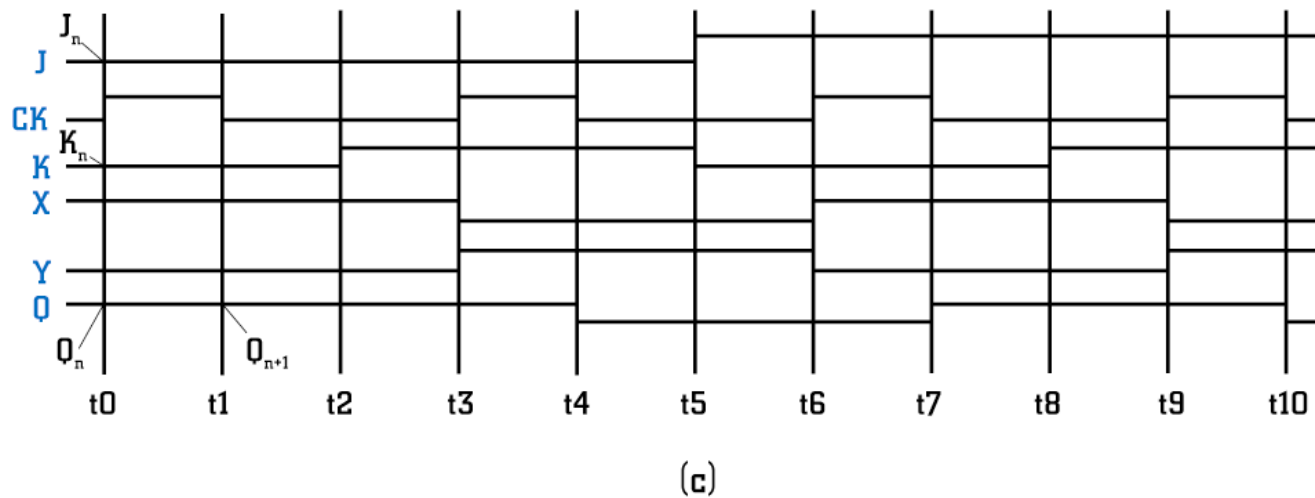
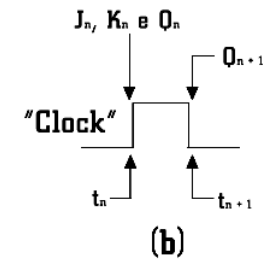
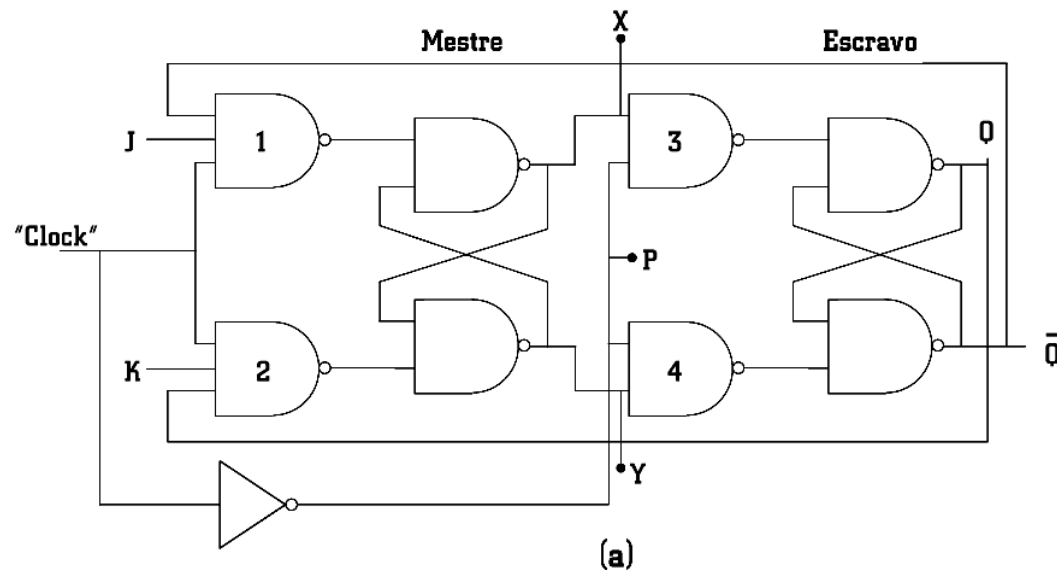


(d)



“Flip-Flop” JK. (a) Circuito; (b) Tabela de combinações; (c) Símbolo; (d) Entradas na transição; (e) Diagrama no tempo.

“FLIP-FLOP” JK “Master-Slave”



PARÂMETROS NO TEMPO

1º) Tempo “set-up” (estabilização) – t_E

Intervalo de tempo mínimo, antes da transição do “clock” ou “enable”, durante o qual as entradas, tais como, R, S, D, J ou K, devem permanecer estáveis.

2º) Tempo “hold” (sustentação) – t_S

Intervalo de tempo mínimo, após a transição do “clock” ou “enable”, durante o qual as entradas, tais como, R, S, D, J ou K, devem permanecer estáveis. Seu valor é da ordem de ns.

3º) Largura de pulso (t_w)

Largura de pulso “clock” para operação confiável do “flip-flop”. Existe a largura mínima para nível 1 denominada de $t_w(H)$ e a largura mínima para nível 0 denominada de $t_w(L)$.

4º) Frequência máxima de operação

Frequência máxima que pode ser aplicada à entrada “clock” para garantir uma operação correta do “flip-flop”.

5º) Atraso (“delay”) de propagação

Tempo decorrido desde o instante de uma transição conveniente do “clock” até uma eventual mudança na saída. Denominado t_{PLH} quando o “flip-flop” opera na subida do “clock” e denominado t_{PHL} quando o “flip-flop” opera na descida do “clock”.

6º) Largura dos pulsos nas entradas diretas

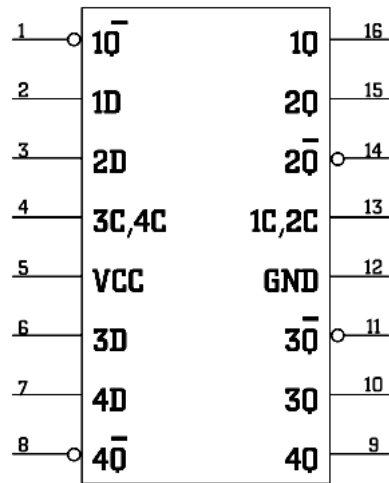
Larguras mínimas, para níveis alto e baixo, nas entradas diretas “reset” e “set” para forçar, respectivamente, uma saída 0 ou 1.

7º) Transição na entrada “clock”

Os tempos de subida e descida do sinal “clock” devem ser pequenos para uma operação correta do “flip-flop”.

CIRCUITOS INTEGRADOS

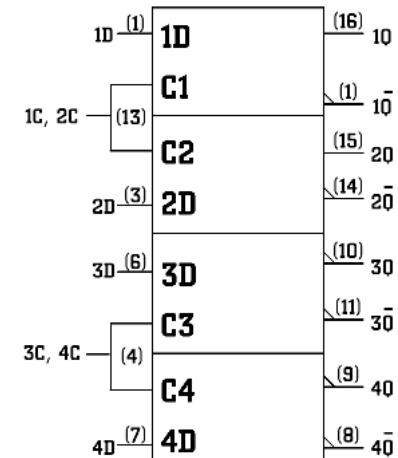
Quatro “latches” tipo D: 7475, 74L75, 74LS75, 74C75, 74HC/HCT75



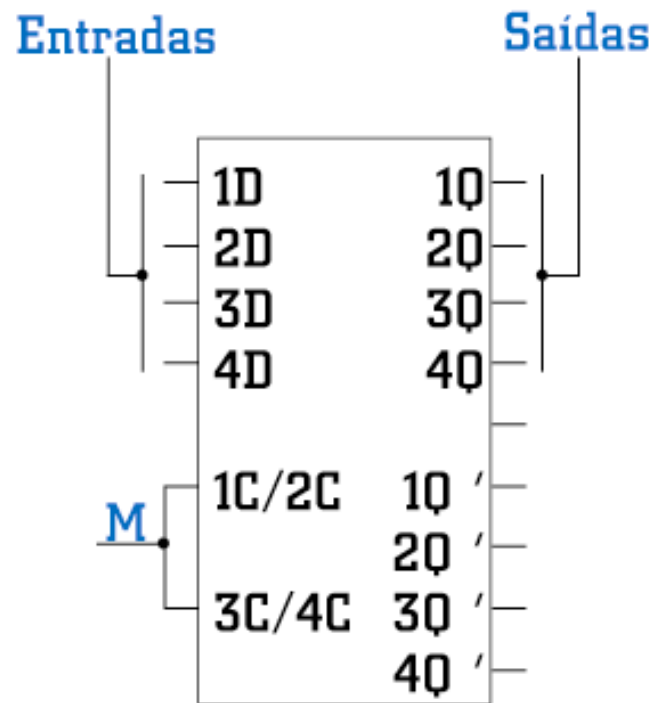
(a)

D	C	Q	\bar{Q}
0	1	0	1
1	1	1	0
X	0	Não muda	

(b)

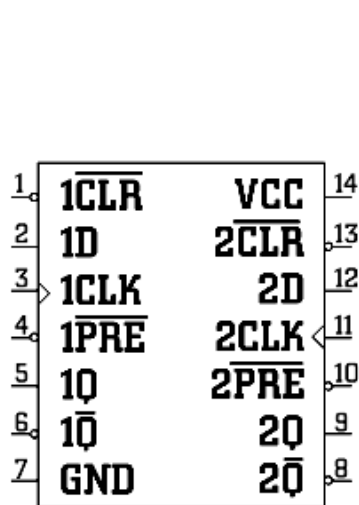


(c)



Aplicação com 74LS75.

Duplo “flip-flop” D: 74LS74, 74HC/HCT74



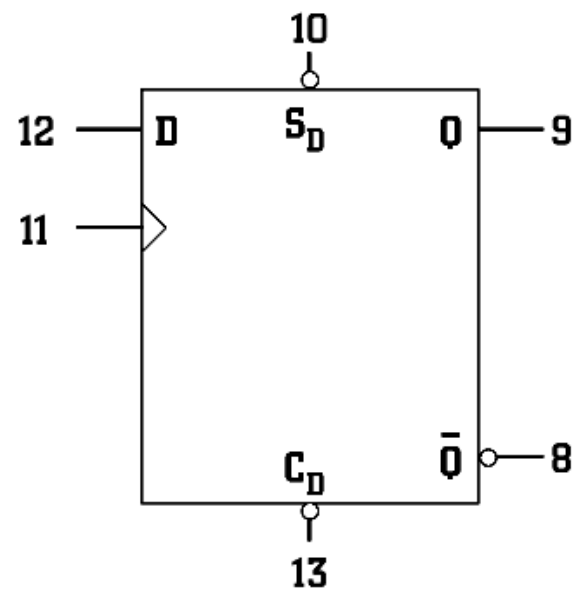
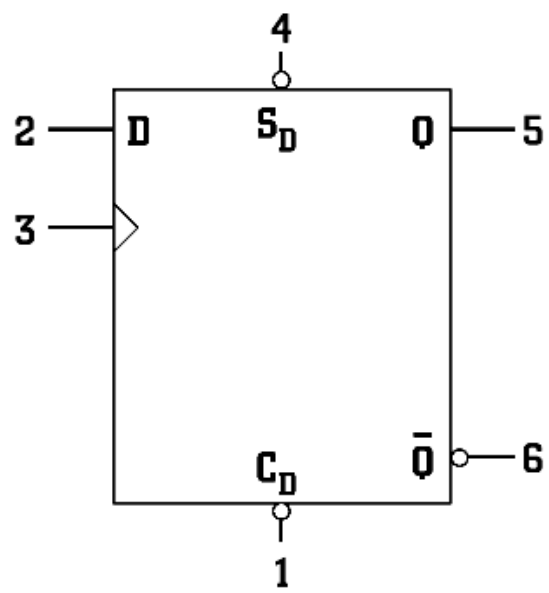
(a)

Pinos 4 ou 10 Pinos 1 ou 13

PRE	CLR	CLK	D	Q	Q̄
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1	1
1	1	POS	1	1	0
1	1	POS	0	0	1
1	1	0	X	Não muda	

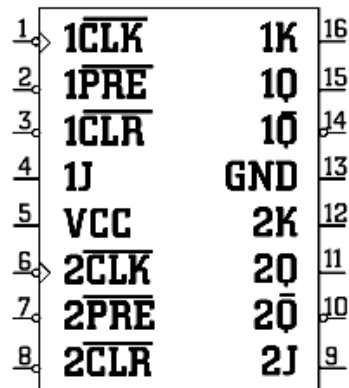
POS = transição positiva de "clk"

(b)



(c)

Duplo “flip-flop” JK “edge-triggered”: 7476, 74LS76, 74C76, 74HC/HCT76

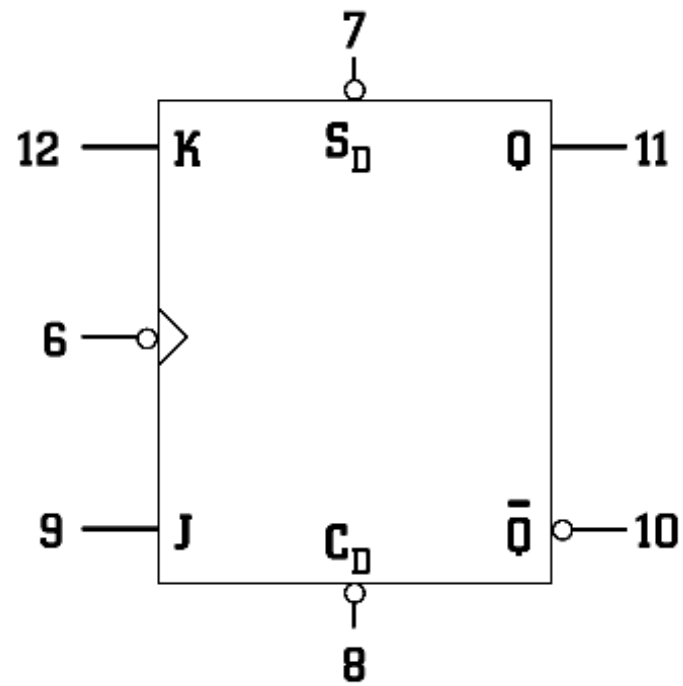
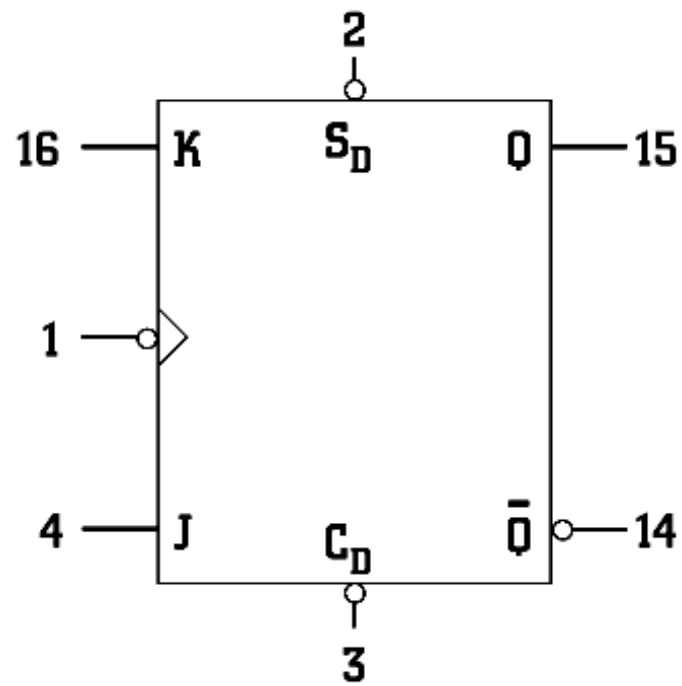


(a)

$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	J	K	Q	$\overline{\text{Q}}$
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	1	1
1	1	NEG	0	0	Não muda	
1	1	NEG	1	0	1	0
1	1	NEG	0	1	0	1
1	1	NEG	1	1	Inverte	

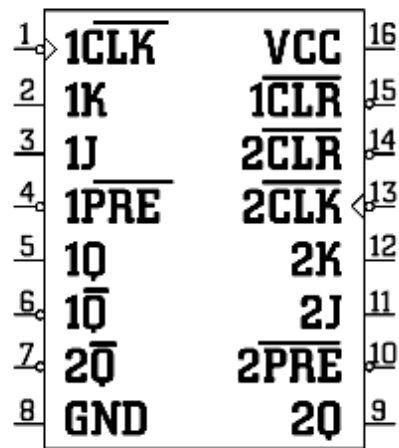
NEG = transição negativa de “clk”

(b)



(c)

Duplo “flip-flop” JK “edge-triggered” com “Clear” e “Preset”: 74LS112,74F112,74LVC112



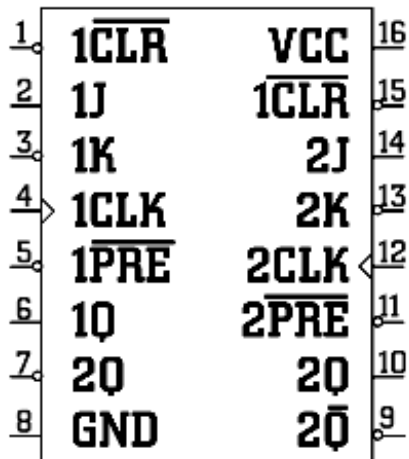
(a)

$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	J	K	Q	$\overline{\text{Q}}$
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	1	1
1	1	NEG	0	0	Não muda	
1	1	NEG	1	0	1	0
1	1	NEG	0	1	0	1
1	1	NEG	1	1	Inverte	
1	1	0	X	X	Não muda	

NEG = transição negativa de “clk”

(b)

Duplo “flip-flop” JK “edge-triggered”: 74LS109, 74HC/HCT109, 74F109



(a)

$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	J	K	Q	$\overline{\text{Q}}$
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	1	1
1	1	POS	0	0	Não muda	
1	1	POS	1	0	0	1
1	1	POS	0	1	1	0
1	1	POS	1	1	Inverte	
1	1	0	X	X	Não muda	

POS = transição positiva de “Clk”

(b)

Seis “flip-flops” D: 74LS174, 74HC/HCT174

1	1CLK	VCC	16
2	1Q	6Q	15
3	1D	6D	14
4	2D	5D	13
5	2Q	5Q	12
6	3D	4D	11
7	3Q	4Q	10
8	GND	CLK	9

(a)

Clear	CLK	D	Q	\bar{Q}
0	X	X	0	1
1	POS	1	1	0
1	POS	0	0	1
1	0	X	Não muda	

POS = transição positiva de “clk”

(b)