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20150465

P2 - Circuitos Digitais

1)

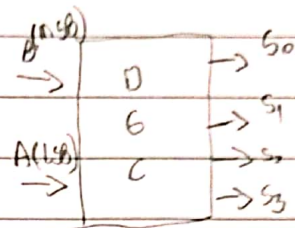
G	B	A	S ₀	S ₁	S ₂	S ₃
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0
1	X	X	1	1	1	1

$$S_0 = B + A$$

$$S_1 = B + \bar{A}$$

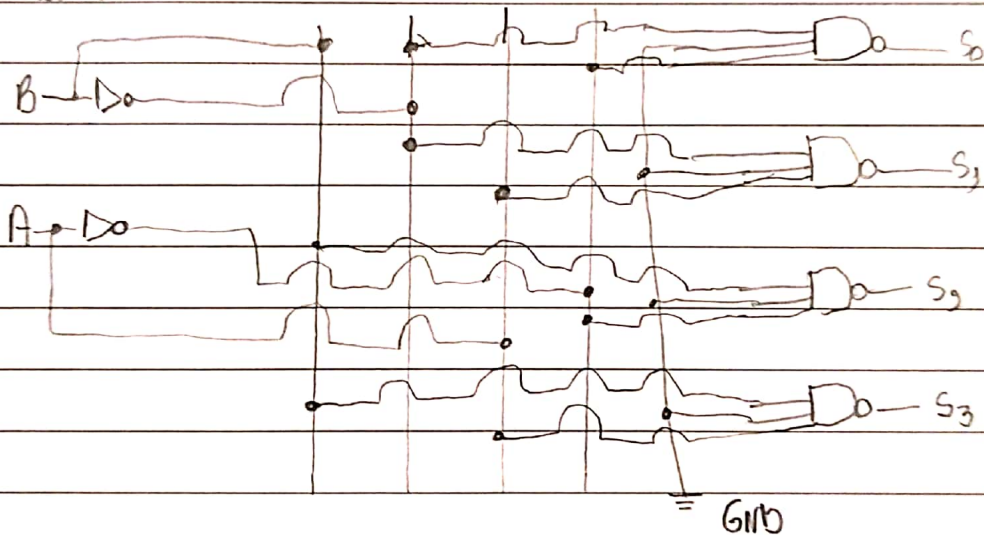
$$S_2 = \bar{B} + A$$

$$S_3 = \bar{B} + \bar{A}$$



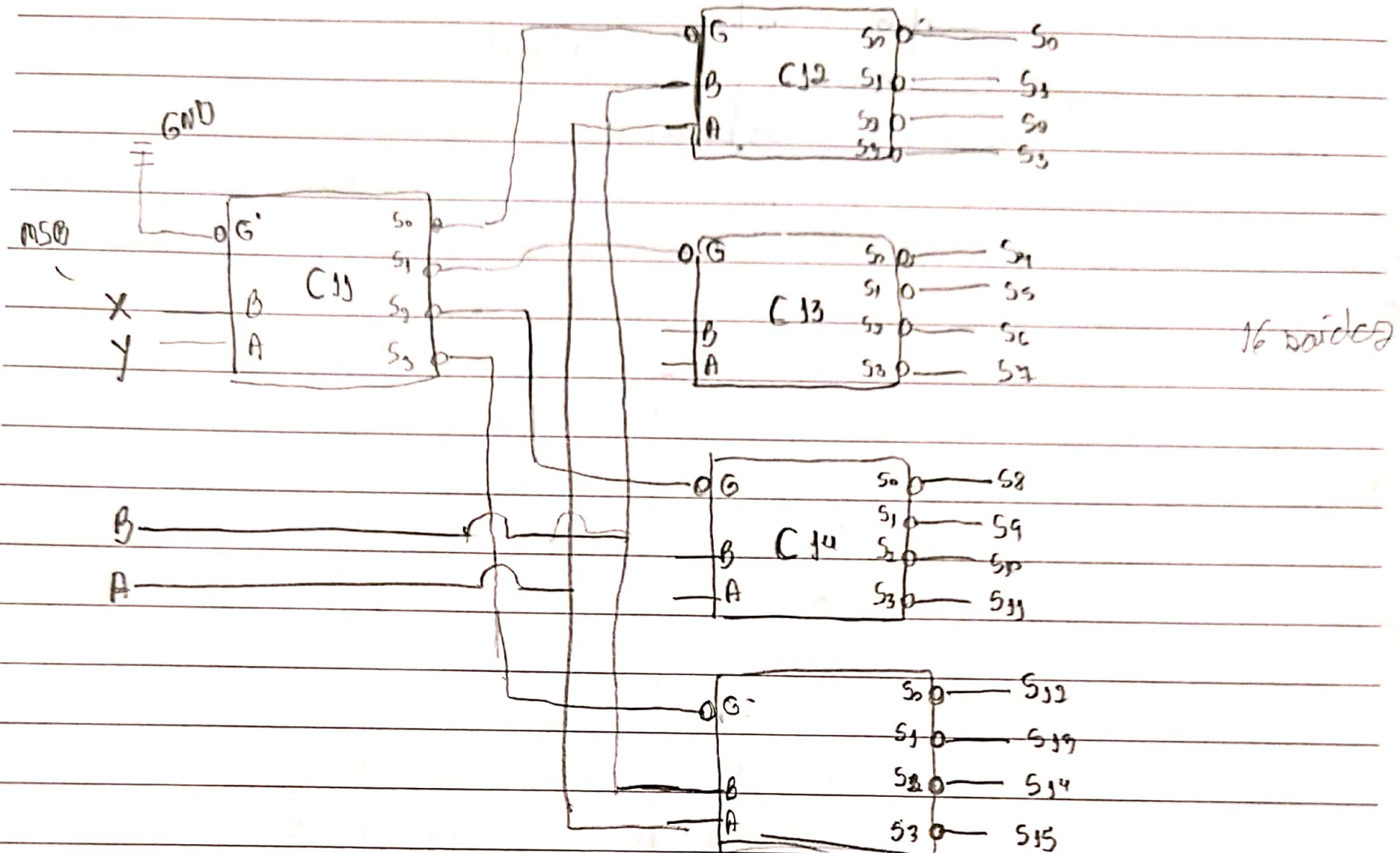
0: Habilitado

1: Desabilitado



"Enable" (0/1)

Associação de decodificadores:



② Associação de multiplexadores. Construir um circuito capaz de representar a equação lógica.

$$f(a,b,c,d) = (\bar{a}\bar{b}c)(\bar{a}\bar{b})(\bar{a}d)$$

2 multiplexadores de 8 entradas

2^8

DIGA: C174151 - 90

$S_0 - S_3$: Entradas de seleção;

E: Entrada de habilitação do CI;

$I_0 - I_7$: Entradas multiplexadas;

Y : Saída;

\bar{Y} : Saída invertida;

$$(\bar{A}\bar{B}C)(\bar{A}\bar{B})(\bar{A}D)$$

$$\overline{X+Y} = \bar{X} \cdot \bar{Y}$$

$$\overline{X \cdot Y} = \bar{X} + \bar{Y}$$

$$(\bar{A}\bar{B}C) + (\bar{A}\bar{B}) + (\bar{A}D)$$

$$\bar{A}(\bar{B}+C) + (\bar{A}+\bar{B}) + (\bar{A}+D)$$

$$\bar{A} + (\bar{B}+C) + (\bar{A} \cdot \bar{B}) + (\bar{A} \cdot D)$$

$$\bar{A} + \bar{B} \cdot C + \bar{A} \cdot \bar{B} + \bar{A}D$$

$$A + \bar{B}C + \bar{A}\bar{B} + \bar{A}D$$

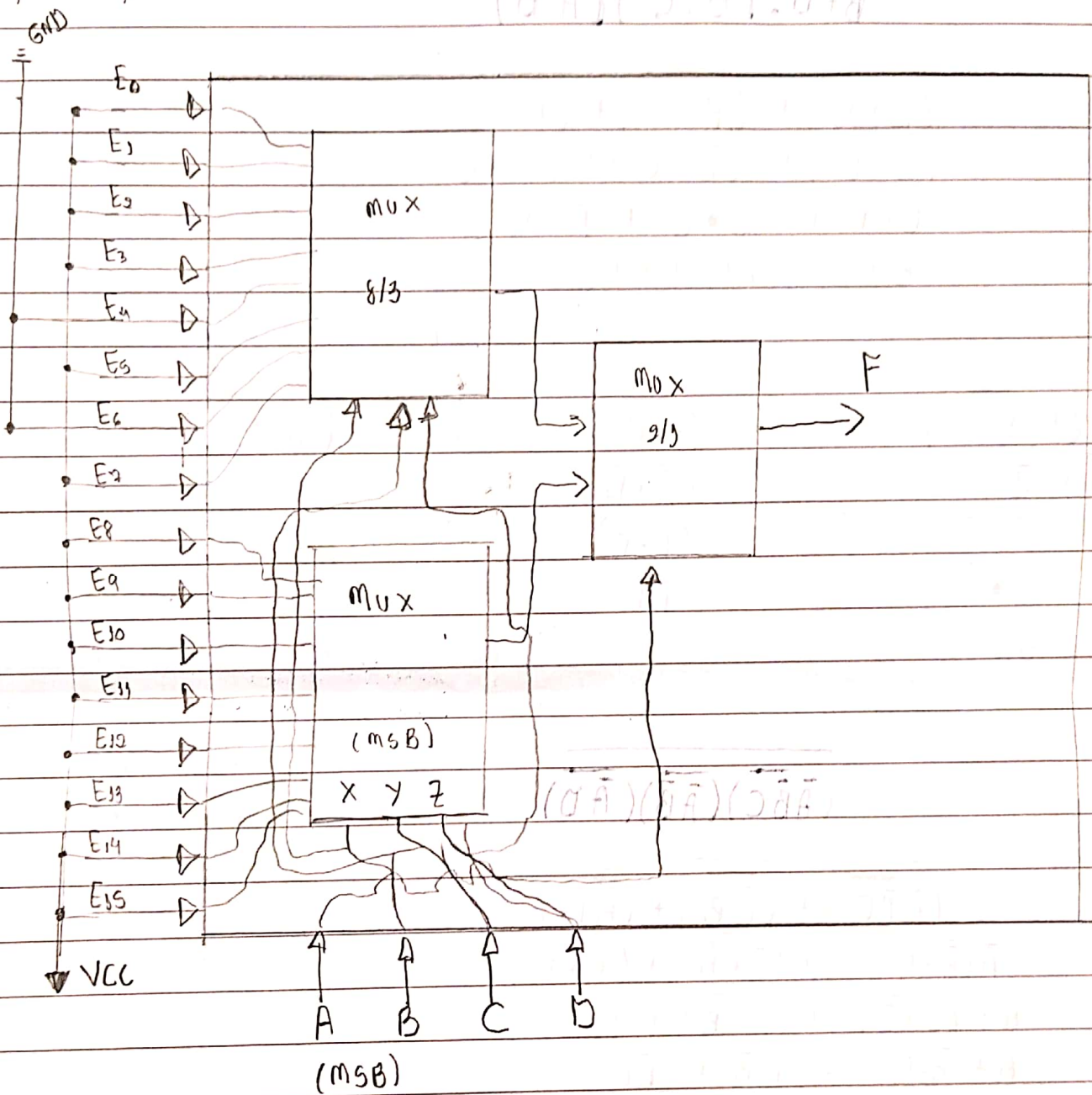
$$\begin{matrix} 1 & 0 & 1 & & 0 & 0 & & 0 & 1 \end{matrix}$$

AB \ CD		00	01	11	10
CD	00	1	0	1	1
	01	1	1	1	1
	11	1	1	1	1
	10	1	0	1	1

$$= \bar{B} + D + A$$

\bar{B}

$\Sigma m(0, 1, 2, 3, 5, 7, 8, 9, 10, 11, 12, 13, 14, 15)$



3) Projete o decodificador (como uma função lógica) que receba números binários A e B de 2 bits cada, apresente as equações de saída e construa em portas lógicas o circuito eletrônico.

mapa para Saída

A	B	C _{in}	S	C _{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

A \ BC	00	01	11	10
0		1		1
1	1		1	

$$S = A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C$$

mapa para Carry out (C_{out})

$$S = \bar{C}(\bar{A}B + A\bar{B}) + C(\bar{A}B + A\bar{B})$$

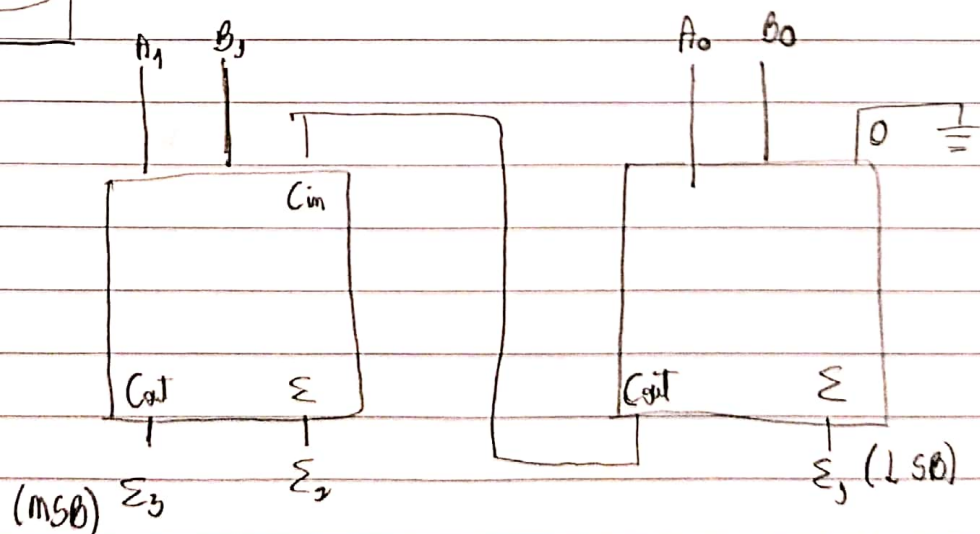
$$S = \bar{C}X_{01} + C\bar{X}_{00}$$

$$S = A \oplus B \oplus C$$

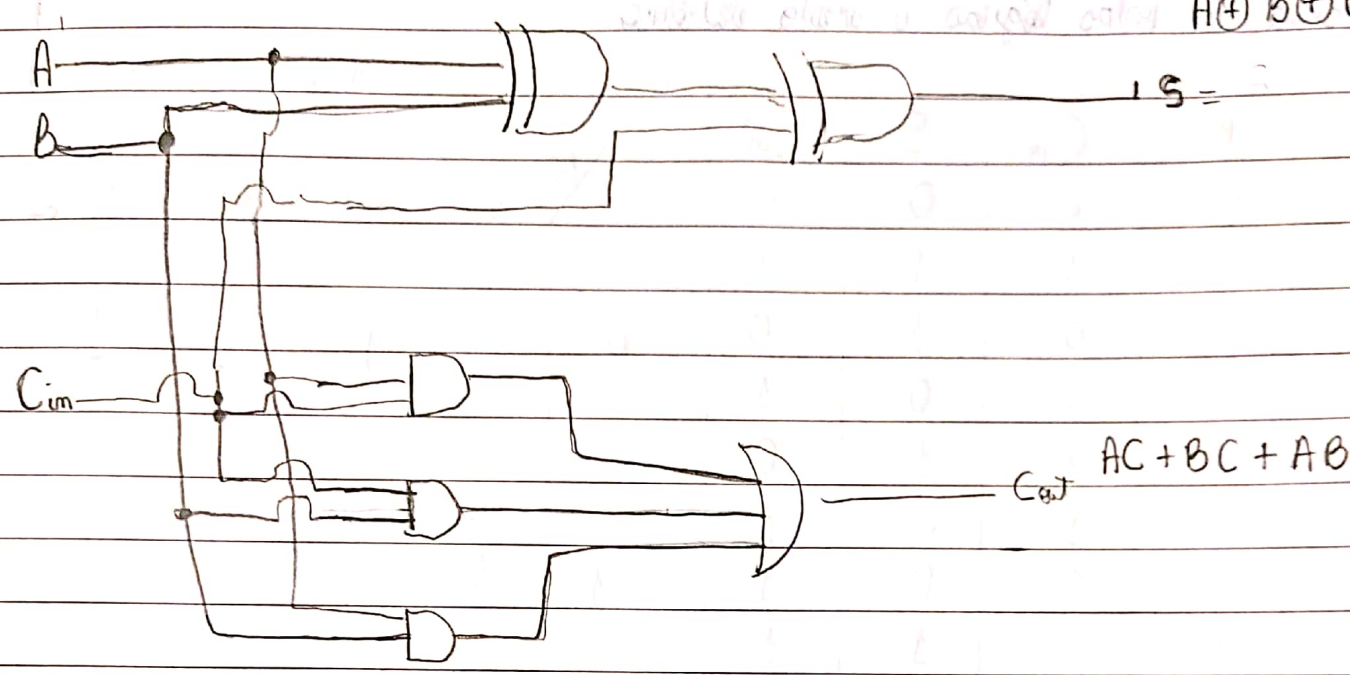
A \ BC	00	01	11	10
0			1	
1	1	1	1	

$$C_{out} = AC + BC + AB$$

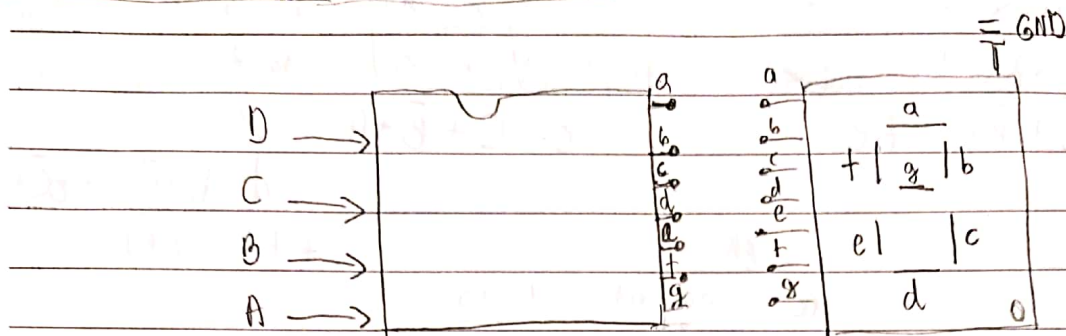
$$\begin{array}{r} A_1 A_0 \\ + B_1 B_0 \\ \hline \Sigma_3 \Sigma_2 \Sigma_1 \end{array}$$



construa um circuito lógico para implementar a função booleana $S = A \oplus B \oplus C$



④ Projete o circuito decodificador de display de 7 segmentos. Apresente a tabela verdade e as equações dos segmentos a, b, c, ..., g, no formato reduzido de soma de produtos. O decodificador é de 4 bits comum, nível alto.



D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	→ 0
0	0	0	1	0	1	1	0	0	0	0	→ 1
0	0	1	0	1	1	0	1	1	0	1	→ 2
0	0	1	1	1	1	1	1	0	0	1	→ 3
0	1	0	0	0	1	1	0	0	1	1	→ 4
0	1	0	1	1	0	1	1	0	1	1	→ 5
0	1	1	0	1	0	1	1	1	1	1	→ 6
0	1	1	1	1	1	1	0	0	0	0	→ 7
1	0	0	0	1	1	1	1	1	1	1	→ 8
1	0	0	1	1	1	1	1	0	1	1	→ 9
1	0	1	0	x	x	x	x	x	x	x	
1	0	1	1	x	x	x	x	x	x	x	
1	1	0	0	x	x	x	x	x	x	x	
1	1	0	1	x	x	x	x	x	x	x	
1	1	1	0	x	x	x	x	x	x	x	
1	1	1	1	x	x	x	x	x	x	x	

DC	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	x	x	x	x
10	1	1	x	x

$$a = D + B + \bar{C}\bar{A} + CA$$

DC \ BA	00	01	11	10
00	1	1	1	1
01	1		1	
11	x	x	x	x
10	1	1	x	x

$$b = C + \bar{B}\bar{A} + AB$$

DC \ BA	00	01	11	10
00	1	1	1	
01	1	1	1	1
11	x	x	x	x
10	1	1	x	x

$$c = C + \bar{B} + A$$

DC \ BA	00	01	11	10
00	1		1	1
01		1		1
11	x	x	x	x
10	1	1	x	x

$$d = D + \bar{C}\bar{A} + \bar{B}\bar{C} + \dots$$

$$\dots + \bar{A}B + A\bar{B}C$$

DC \ BA	00	01	11	10
00	1			1
01				1
11	x	x	x	x
10	1		x	x

$$e = \bar{C}\bar{A} + \bar{B}\bar{A}$$

DC \ BA	00	01	11	10
00	1			
01	1	1		1
11	x	x	x	x
10	1	1	x	x

$$f = D + \bar{B}A + C\bar{B} + C\bar{A}$$

DC \ BA	00	01	11	10
00			1	1
01	1	1		1
11	x	x	x	x
10	1	1	x	x

$$g = D + C\bar{B} + C\bar{A} + \bar{C}\bar{B}$$