CIRCUITOS E DISPOSITIVOS ESPECIAIS

OBJETIVOS

No final deste capítulo, o leitor será capaz de:

- Entender o Funcionamento dos Circuitos Decodificadores;
- Associar Decodificadores para obter equivalentes mais complexos;
- Entender o Funcionamento do Diodo Emissor de Luz (“LED”);
- Trabalhar com “Displays” com “Leds” e tipo Cristal Líquido;
- Entender o Funcionamento dos Multiplexadores e Demultiplexadores;
- Associar Multiplexadores visando a equivalentes mais complexos;
- Implementar Funções com Multiplexadores;
- Associar Demultiplexadores visando a equivalentes mais complexos.

RESUMO

Projeto de um Decodificador 2/4

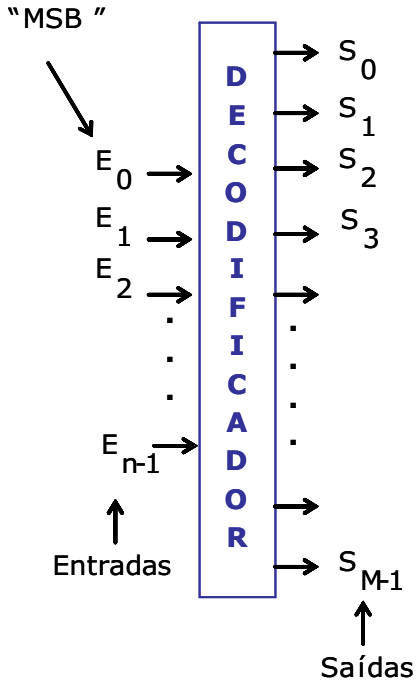
“Leds” e “Displays”

Multiplexador

Demultiplexador

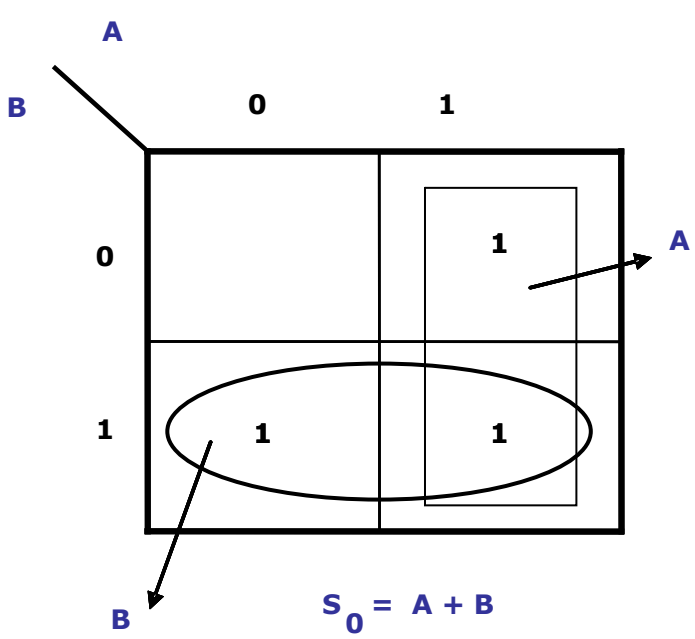
Comparador

Codificador



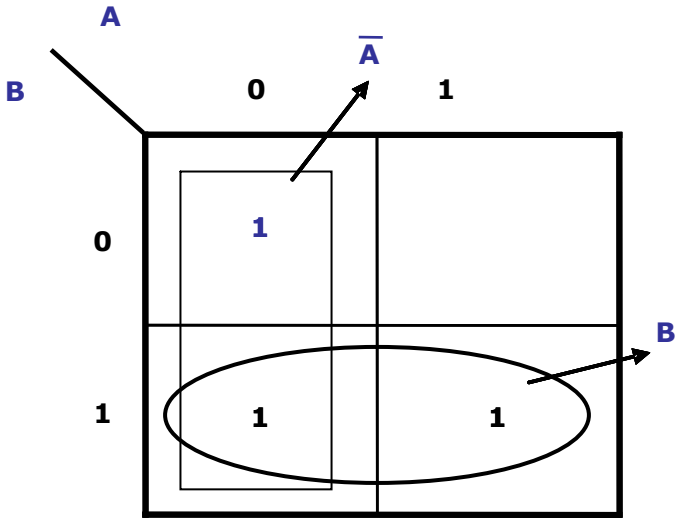
PROJETO DE UM DECODIFICADOR 2/4

Entradas	Saídas			
BA	S0	S1	S2	S3
00	0	1	1	1
01	1	0	1	1
10	1	1	0	1
11	1	1	1	0



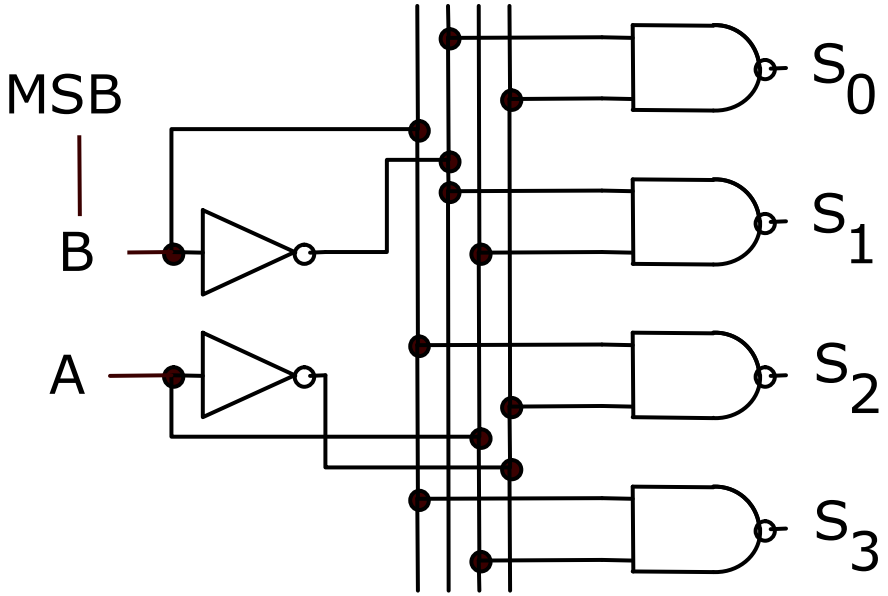
$S_0 = A + B$

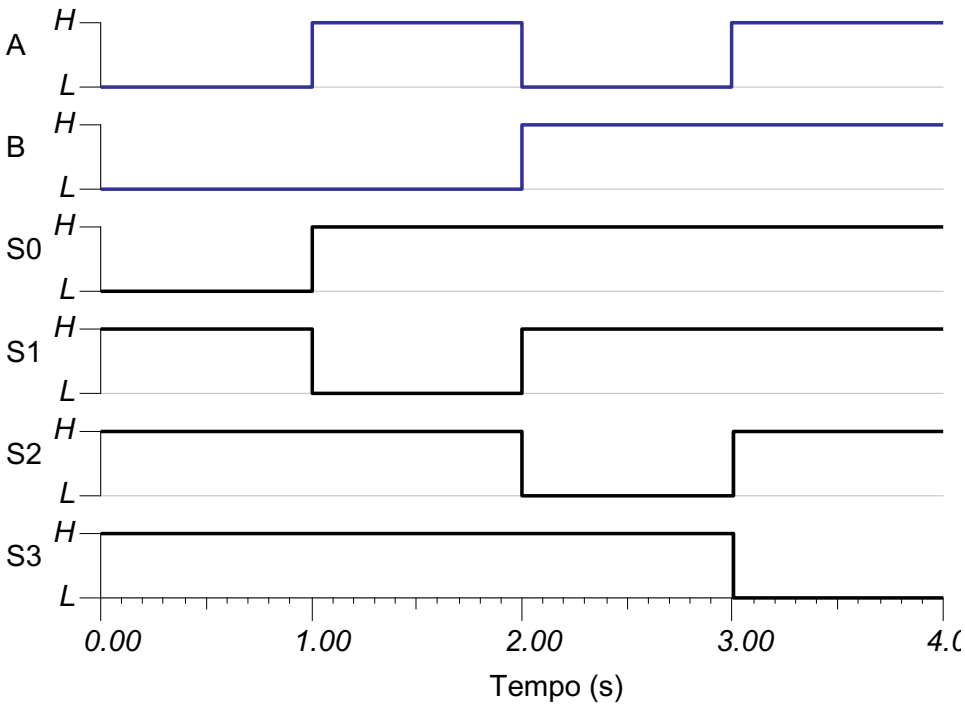
$S_0 = B + A = \overline{\overline{B} + \overline{A}} = B \cdot A$

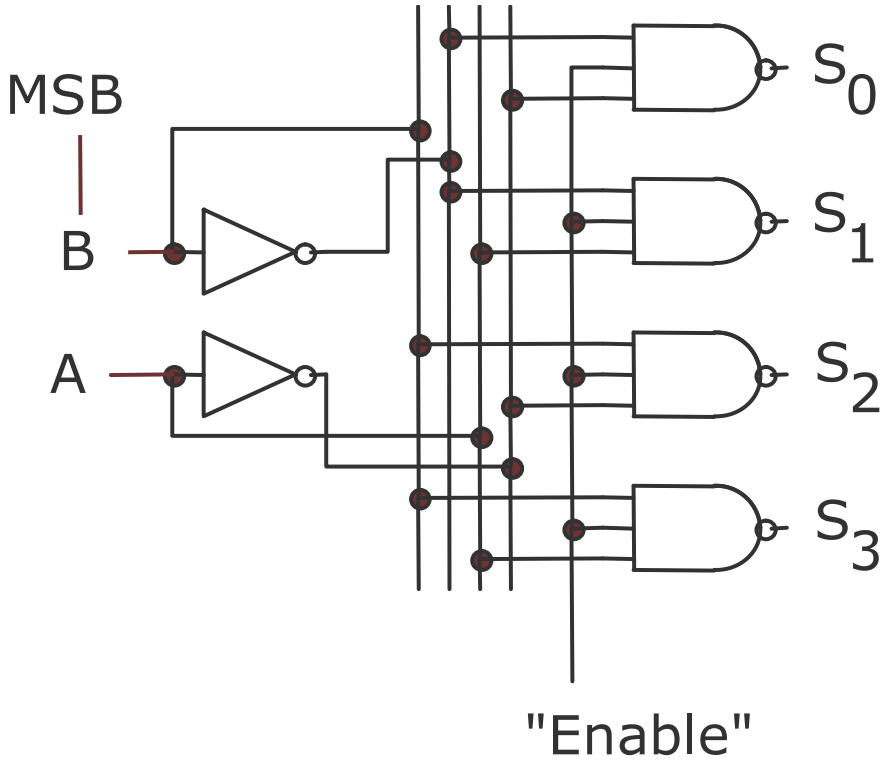


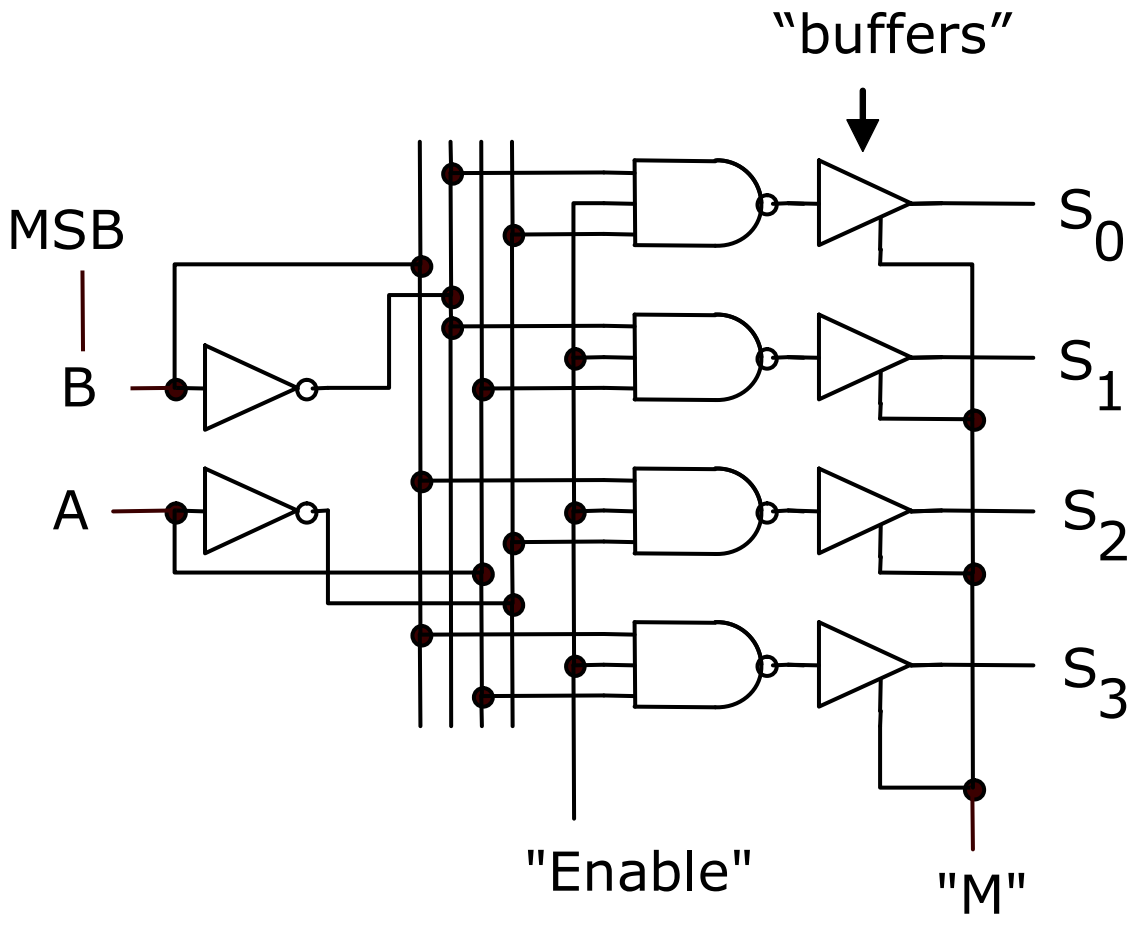
$S_1 = B + \overline{A}$

$S_1 = B + \overline{A} = \overline{\overline{B} + \overline{\overline{A}}} = B \cdot A$

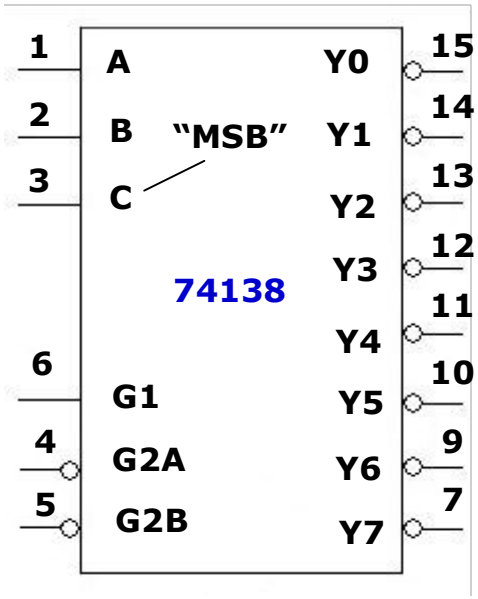

MSB
B
A
S0
S1
S2
S3

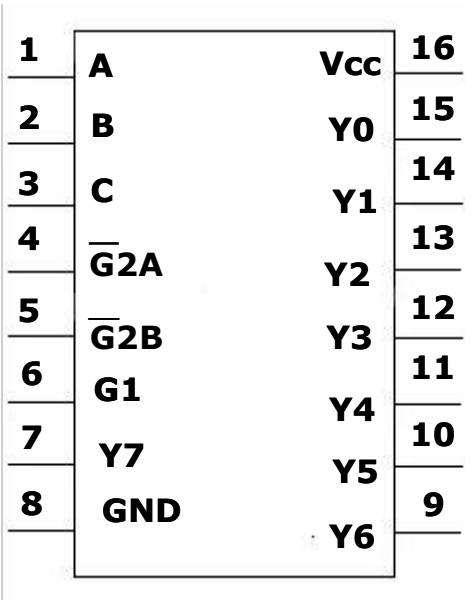

A
B
S0
S1
S2
S3
H
L
0.00
1.00
2.00
3.00
Tempo (s)

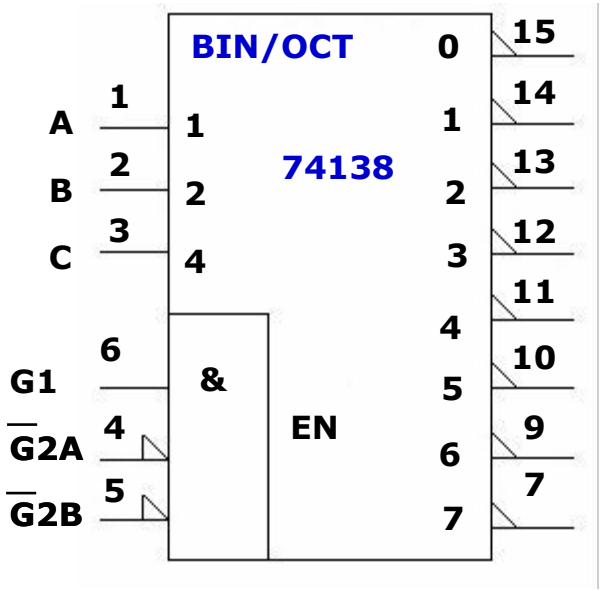

MSB
B
A
S0
S1
S2
S3
"Enable"


“buffers”
MSB
B
A
S0
S1
S2
S3
"Enable"
"M"

Circuito Integrado 74138, 74XX138





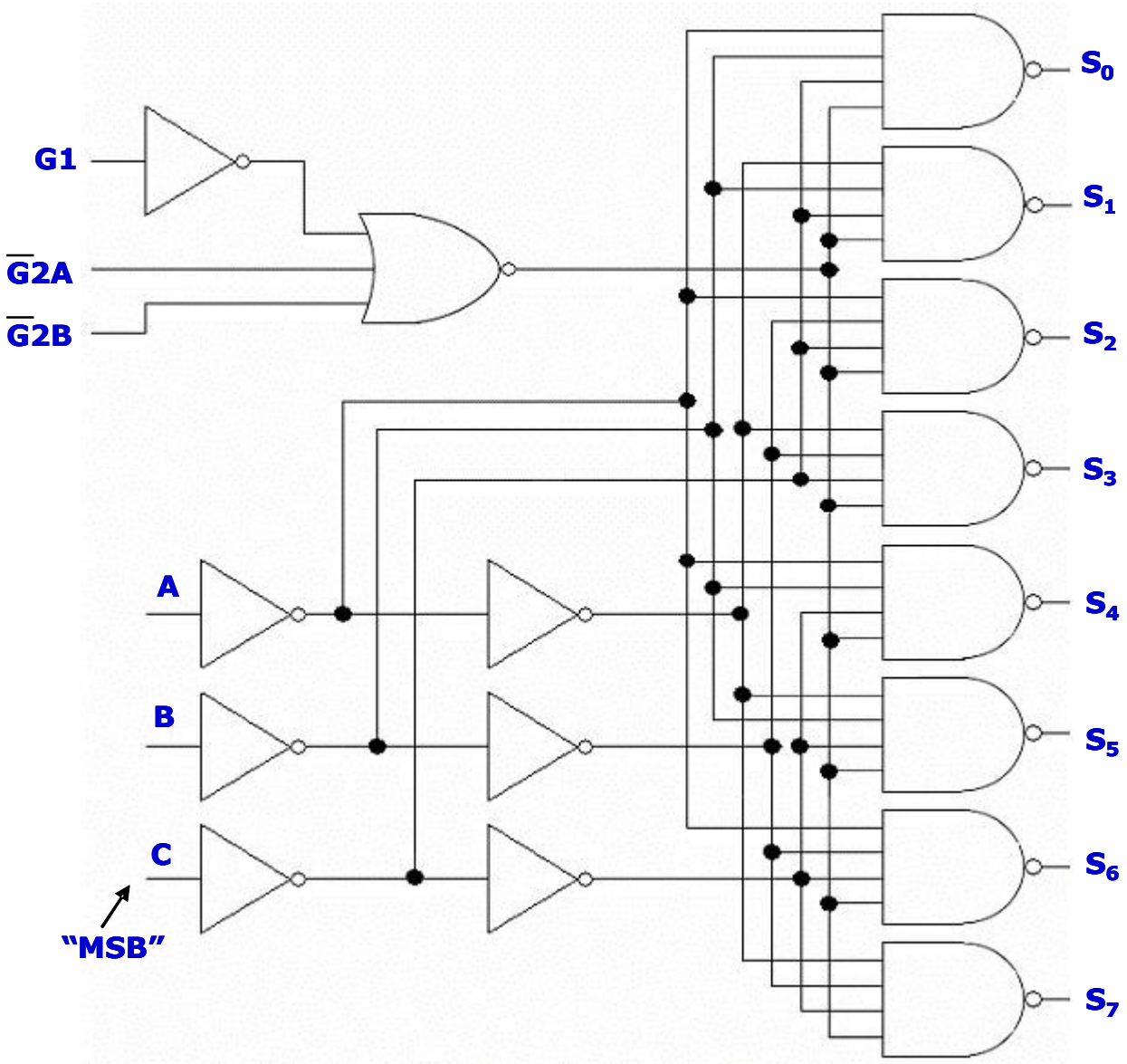


Entradas						Saídas							
"Enable"			Seleção										
G1	$\bar{G}$2A	$\bar{G}$2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	1	0	X	X	X	1	1	1	1	1	1	1	1
X	0	1	X	X	X	1	1	1	1	1	1	1	1
X	1	1	X	X	X	1	1	1	1	1	1	1	1
0	X	X	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	0	0	1	1	1	1	0	1	1	1
1	0	0	1	0	1	1	1	1	1	1	0	1	1
1	0	0	1	1	0	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
6	4	5				15							7

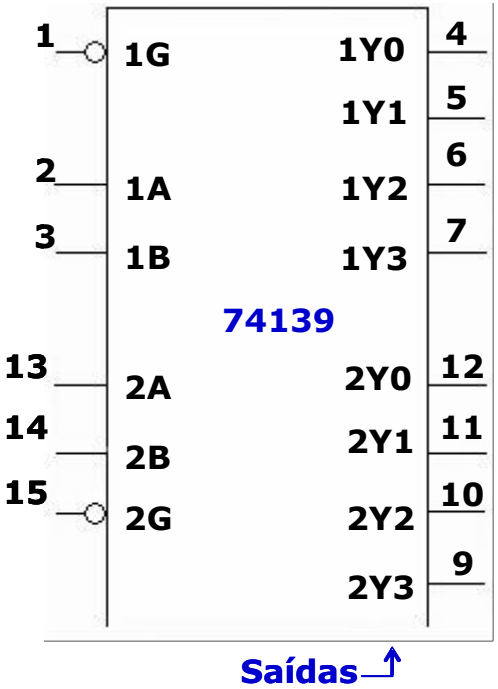
Bloqueado

Liberado

Pinos

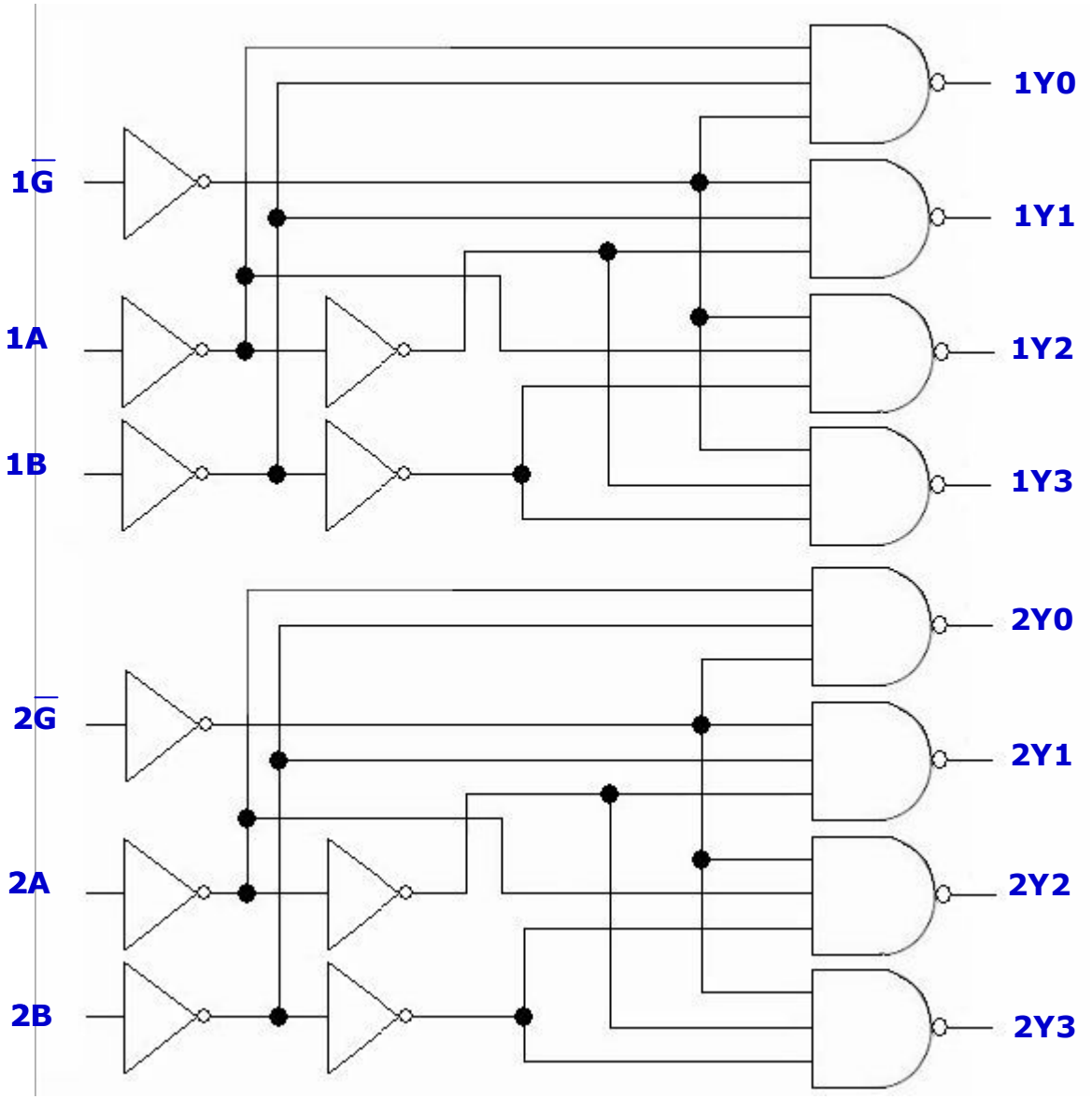

G1
$\overline{G2A}$
$\overline{G2B}$
A
B
C
"MSB"
S_0
S_1
S_2
S_3
S_4
S_5
S_6
S_7

Circuito Integrado 74139, 74LS139, 74HC139



"n" é igual a 1 ou 2

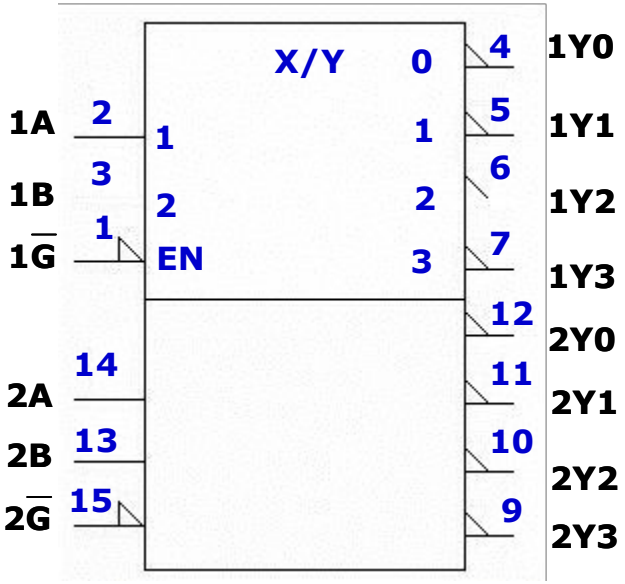
Entradas			Saídas			
nG'	nB	nA	nY0	nY1	nY2	nY3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0
1	3	2	4	←	Pinos	



74139

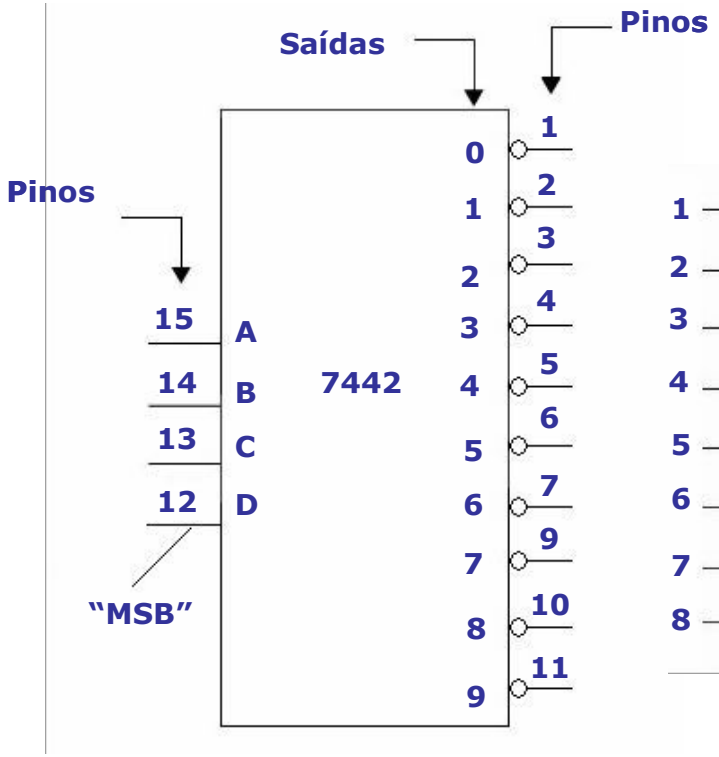

1
1G
Vcc
16
2
1A
2G
15
3
1B
2A
14
4
1Y0
2B
13
5
1Y1
2Y0
12
6
1Y2
2Y1
11
7
1Y3
2Y2
10
8
GND
2Y3
9

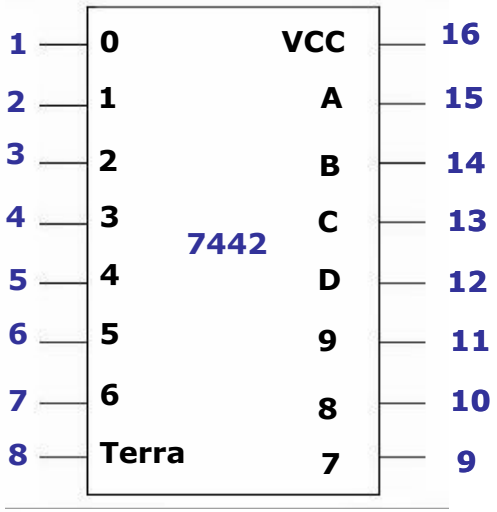
74139

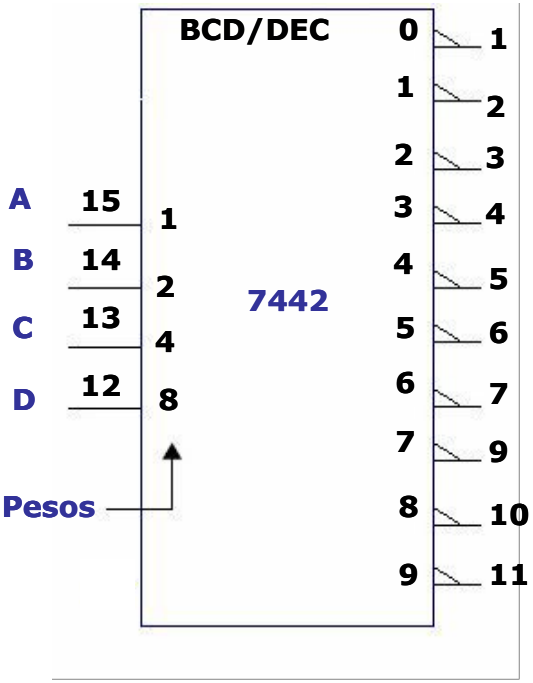

X/Y
0
1
2
3
EN
1A
2
1B
3
1G
1
2A
14
2B
13
2G
15
4
5
6
7
12
11
10
9
1Y0
1Y1
1Y2
1Y3
2Y0
2Y1
2Y2
2Y3

74139

Decodificador Decimal
Circuito Integrado 7442, 74XX42

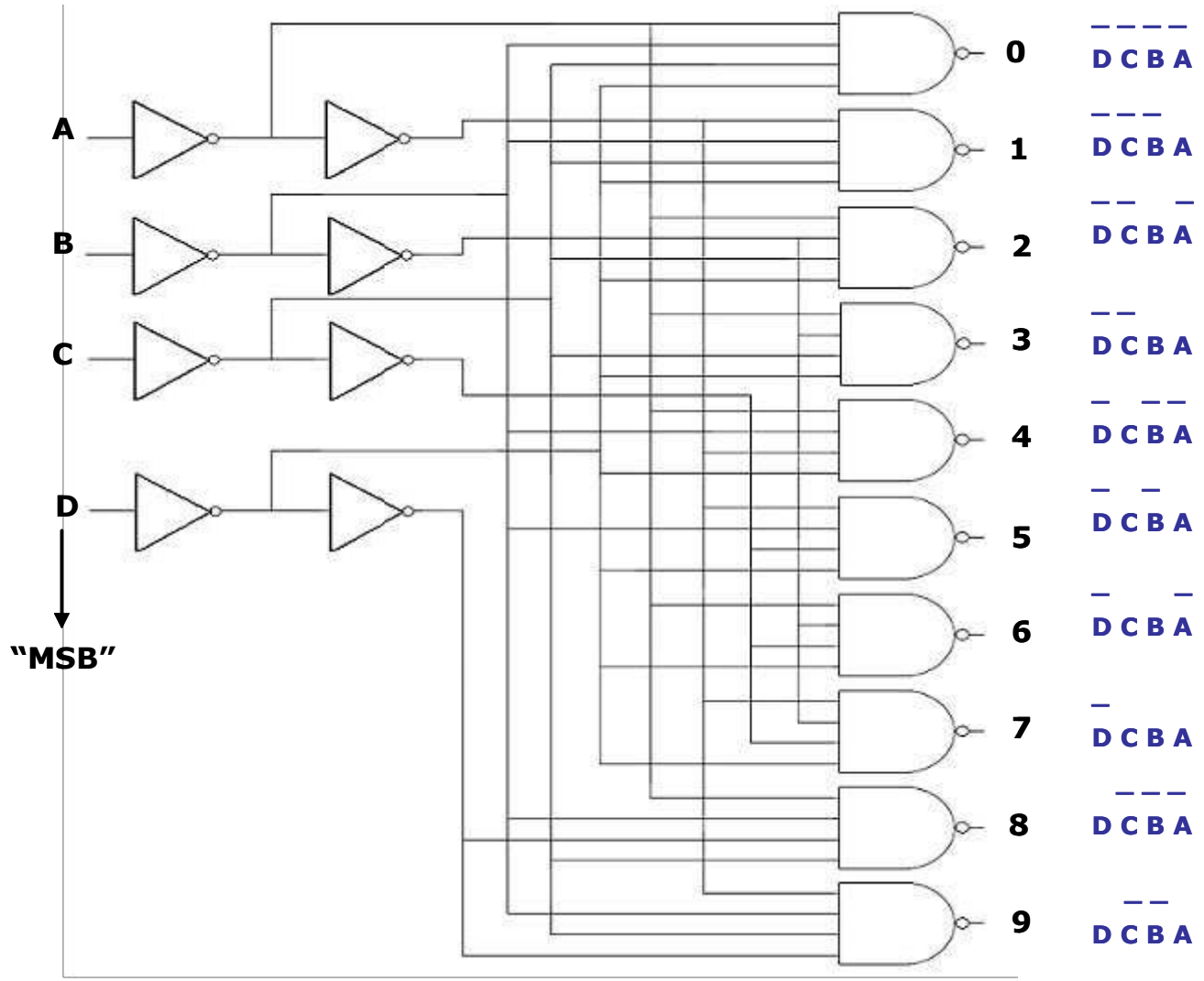


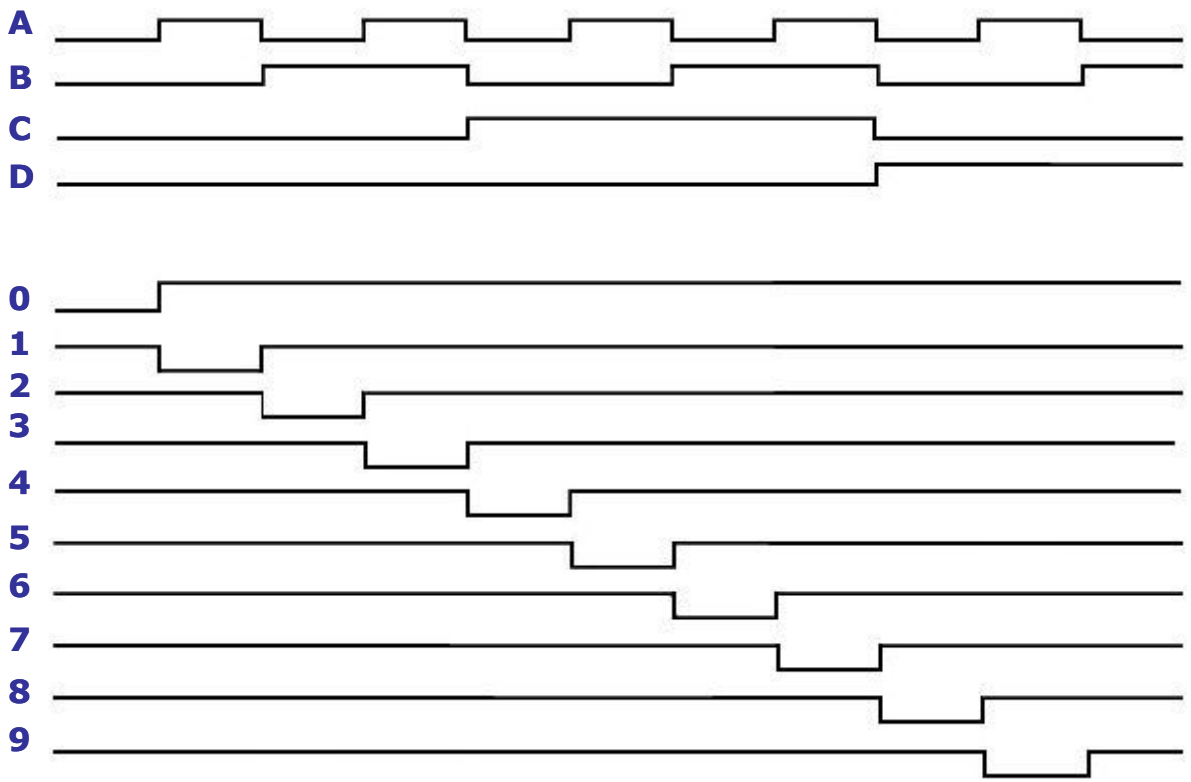




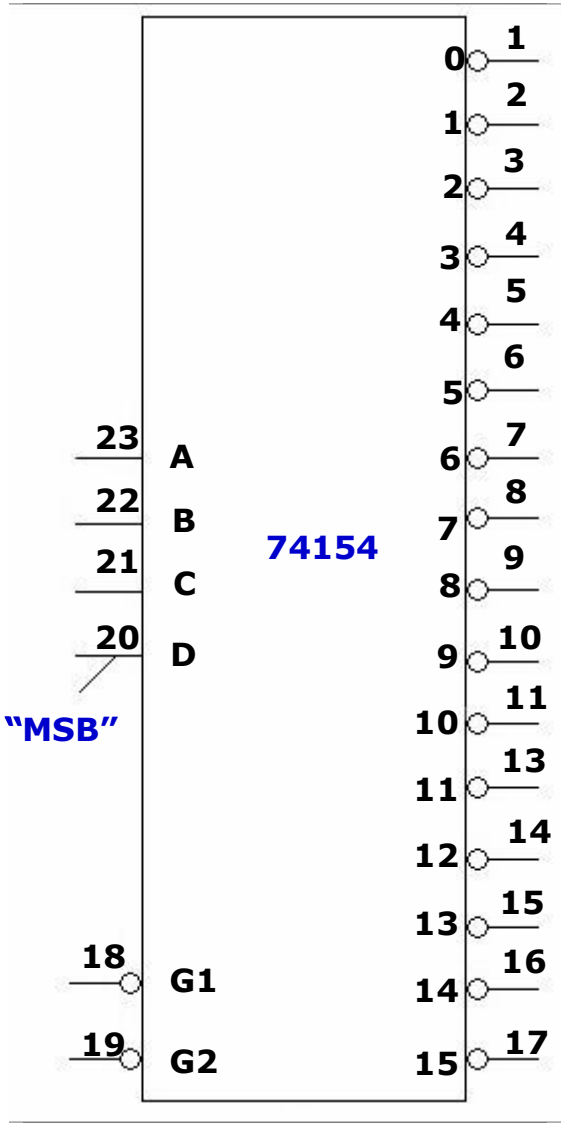
Entradas	Saídas									
DCBA	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
0000	0	1	1	1	1	1	1	1	1	1
0001	1	0	1	1	1	1	1	1	1	1
0010	1	1	0	1	1	1	1	1	1	1
0011	1	1	1	0	1	1	1	1	1	1
0100	1	1	1	1	0	1	1	1	1	1
0101	1	1	1	1	1	0	1	1	1	1
0110	1	1	1	1	1	1	0	1	1	1
0111	1	1	1	1	1	1	1	0	1	1
1000	1	1	1	1	1	1	1	1	0	1
1001	1	1	1	1	1	1	1	1	1	0
1010	1	1	1	1	1	1	1	1	1	1
1011	1	1	1	1	1	1	1	1	1	1
1100	1	1	1	1	1	1	1	1	1	1
1101	1	1	1	1	1	1	1	1	1	1
1110	1	1	1	1	1	1	1	1	1	1
1111	1	1	1	1	1	1	1	1	1	1

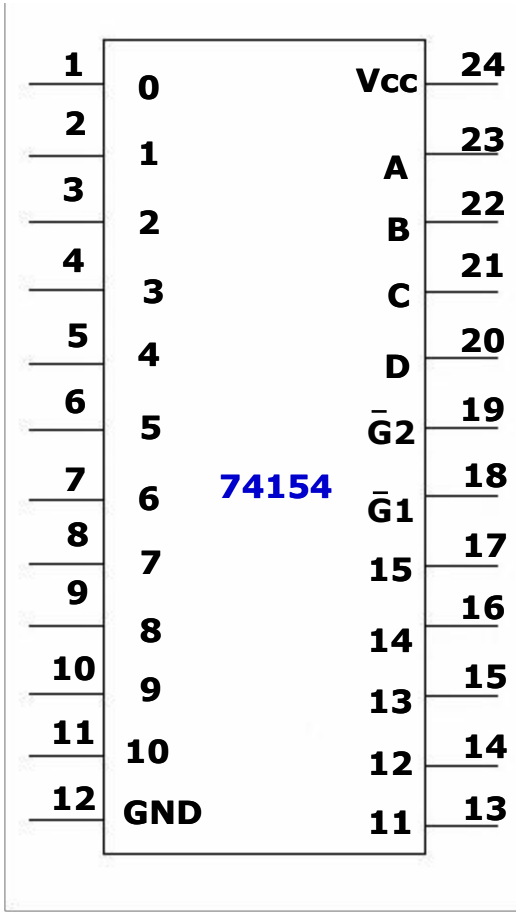
$0 = \overline{D}\,\overline{C}\,\overline{B}\,\overline{A}$	$1 = \overline{D}\,\overline{C}\,\overline{B}\,A$
$2 = \overline{D}\,\overline{C}\,B\,\overline{A}$	$3 = \overline{D}\,\overline{C}\,B\,A$
$4 = \overline{D}\,C\,\overline{B}\,\overline{A}$	$5 = \overline{D}\,C\,\overline{B}\,A$
$6 = \overline{D}\,C\,B\,\overline{A}$	$7 = \overline{D}\,C\,B\,A$
$8 = D\,\overline{C}\,\overline{B}\,\overline{A}$	$9 = D\,\overline{C}\,\overline{B}\,A$

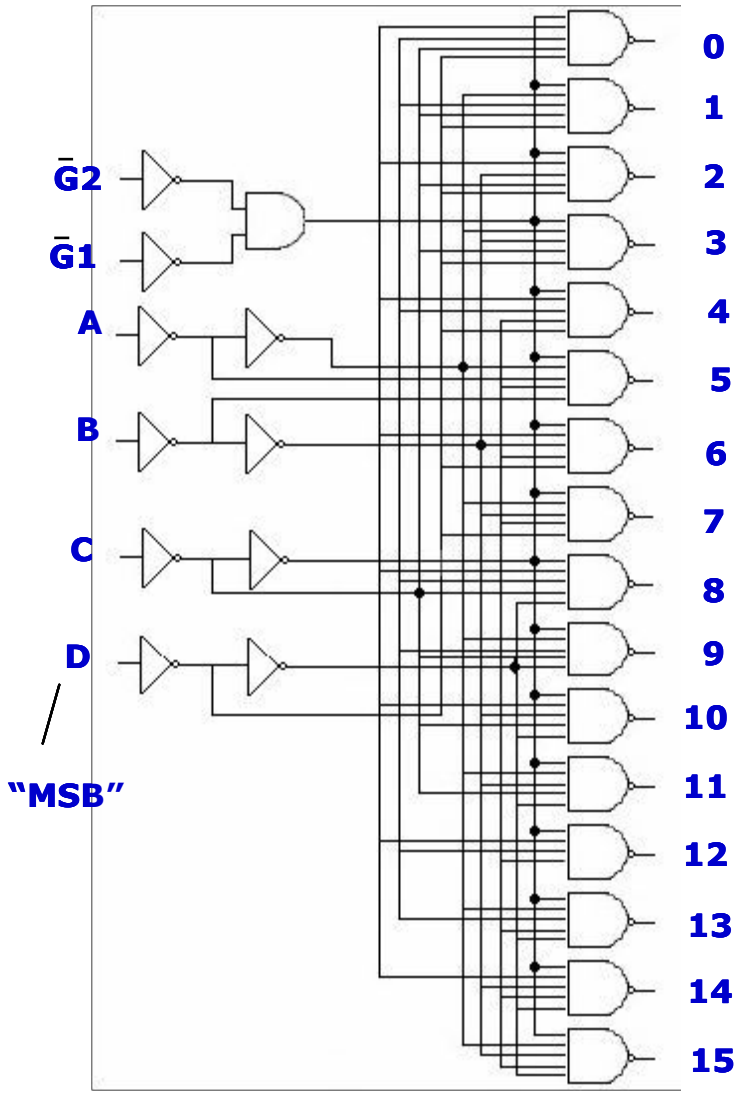

A
B
C
D
"MSB"
0
1
2
3
4
5
6
7
8
9
D C B A
D C B A
D C B A
D C B A
D C B A
D C B A
D C B A
D C B A
D C B A
D C B A


A
B
C
D
0
1
2
3
4
5
6
7
8
9

Decodificador Hexadecimal
Circuito Integrado 74154, 74LS154, 74HC154





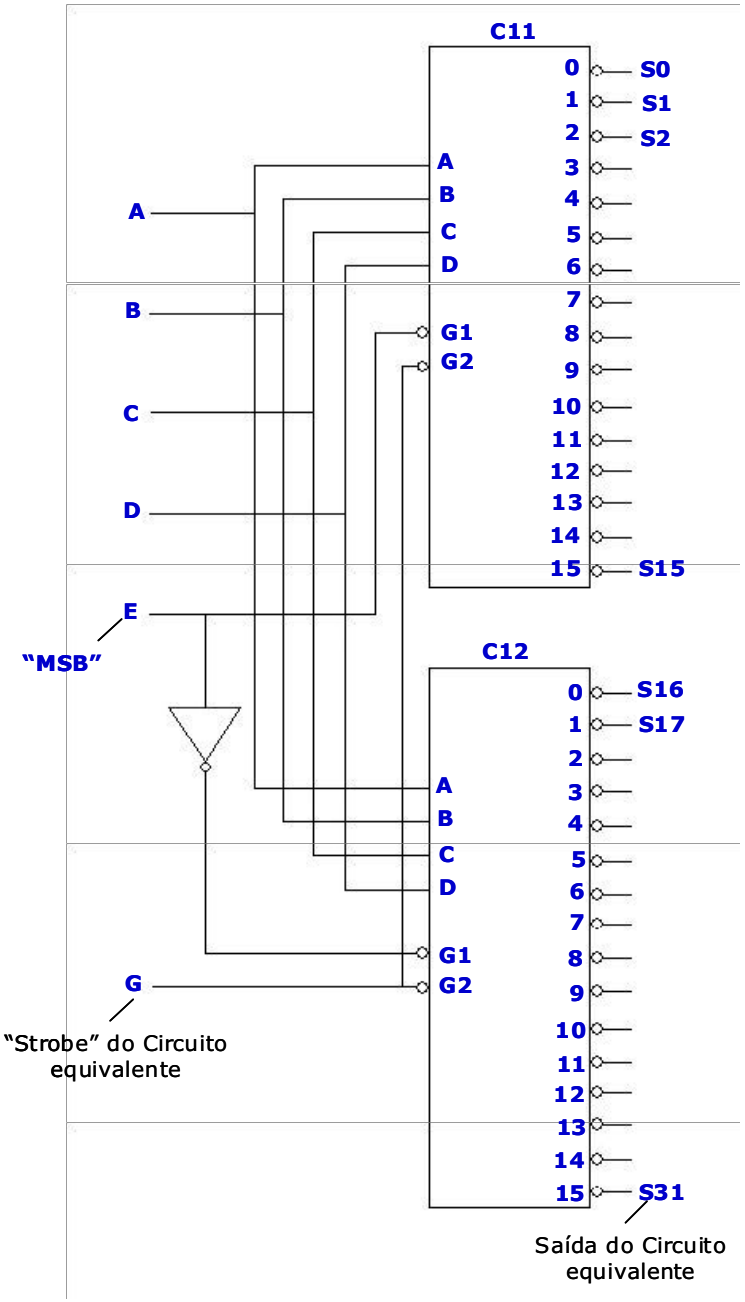

$\bar{G}2$
$\bar{G}1$
A
B
C
D
"MSB"
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

Entradas			Saídas														
$\bar{G}1$	$\bar{G}2$	DCBA	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0000	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0001	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0010	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0011	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0100	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	0101	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	0	0110	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0	0	0111	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
0	0	1000	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
0	0	1001	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
0	0	1010	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
0	0	1011	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
0	0	1100	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
0	0	1101	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	1110	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	0	1111	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0	1	XXXX	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	XXXX	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	XXXX	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
18	19		1	2	←	Pinos												

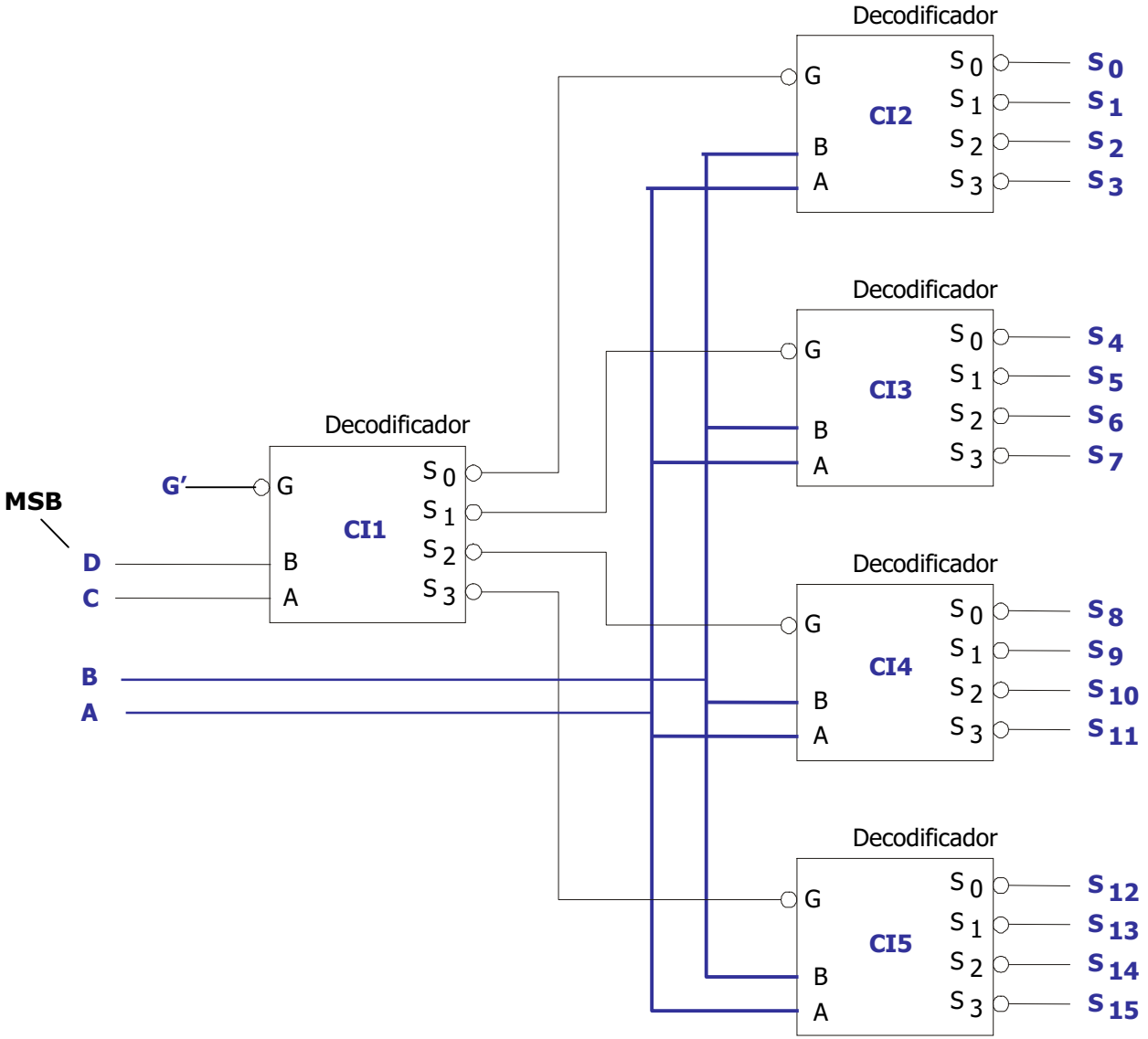
LIBERADO

Bloqueio

Associação de Decodificadores

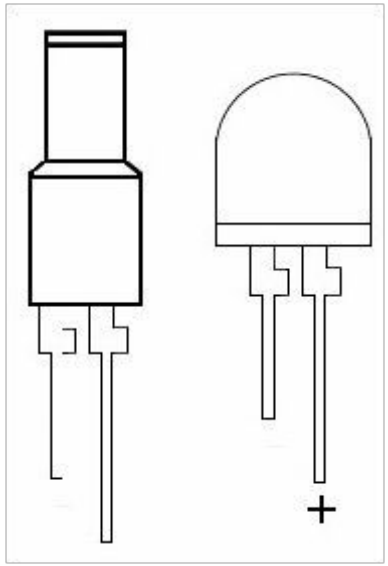


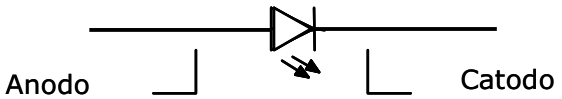
Entradas					Saídas	Comentário
E	**D**	**C**	**B**	**A**	**Nível 0**	**Habilidade**
0	0	0	0	0	S0	C11
	0	0	0	1	S1	
	0	0	1	0	S2	
	...	...	...	...	...	
	...	...	...	...	...	
	...	...	...	...	...	
	...	...	...	...	...	
	1	1	1	1	S15	
1	0	0	0	0	S16	C12
	0	0	0	1	S17	
	0	0	1	0	S18	
	...	...	...	...	...	
	...	...	...	...	...	
	...	...	...	...	...	
	...	...	...	...	...	
	1	1	1	1	S31	

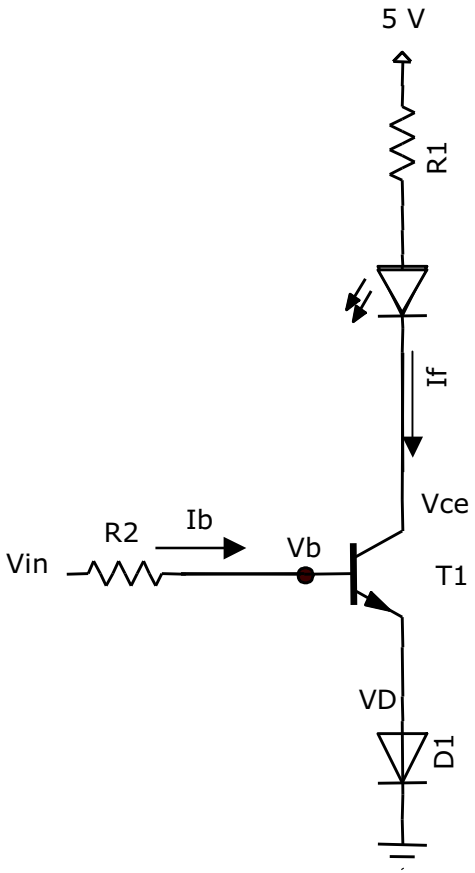

Decodificador
CI1
G
B
A
S 0
S 1
S 2
S 3
G'
MSB
D
C
B
A
Decodificador
CI2
G
B
A
S 0
S 1
S 2
S 3
S 0
S 1
S 2
S 3
Decodificador
CI3
G
B
A
S 0
S 1
S 2
S 3
S 4
S 5
S 6
S 7
Decodificador
CI4
G
B
A
S 0
S 1
S 2
S 3
S 8
S 9
S 10
S 11
Decodificador
CI5
G
B
A
S 0
S 1
S 2
S 3
S 12
S 13
S 14
S 15

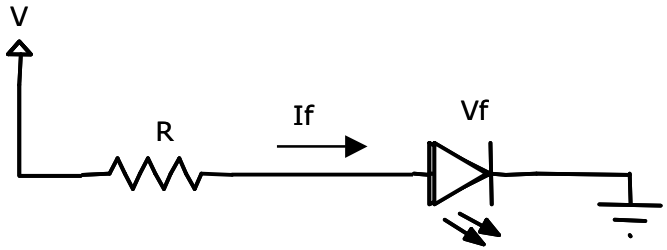
“LEDS” E “DISPLAYS”

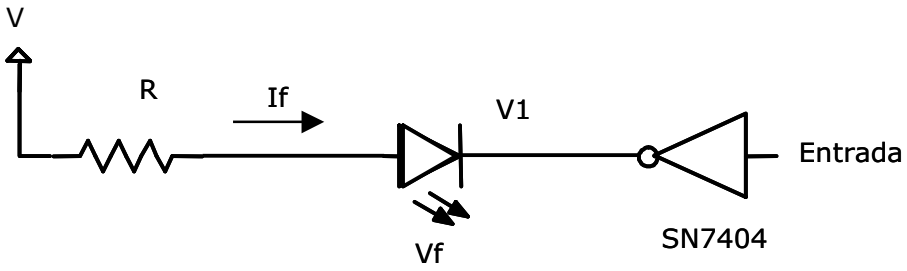
Diodo Emissor de Luz (“Light emitting diode”)



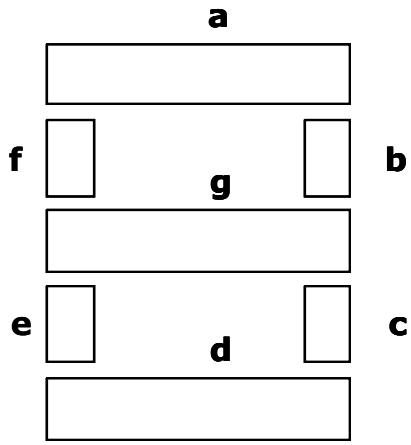


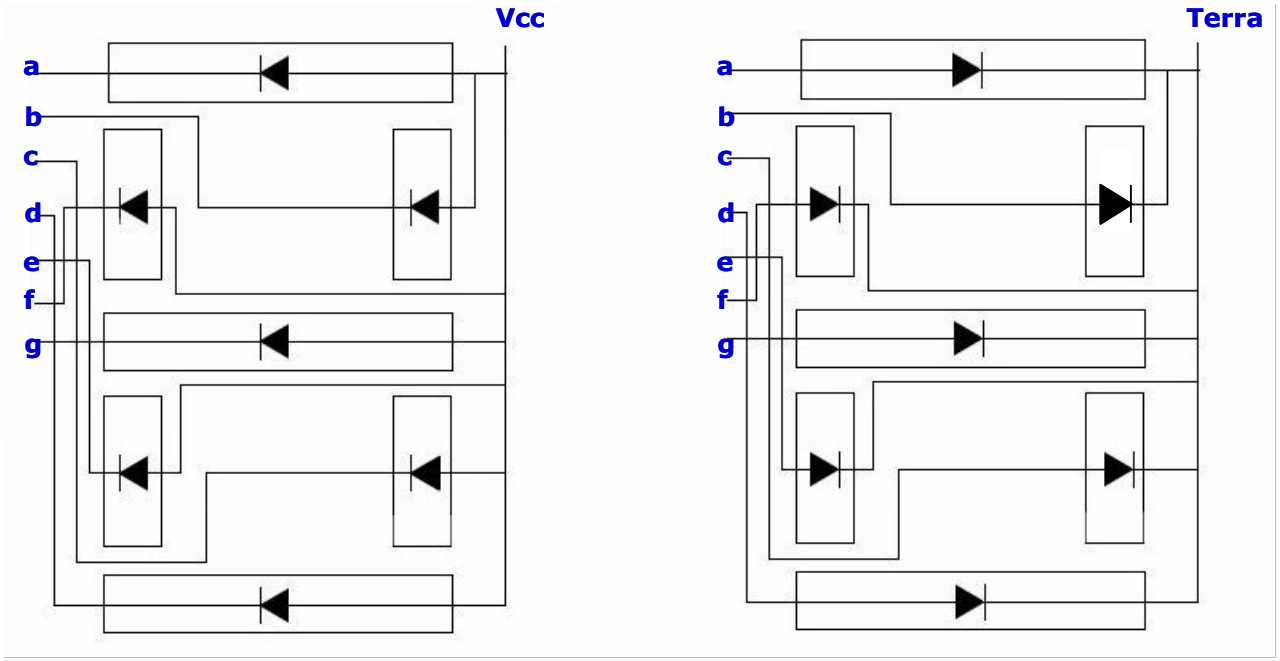

5 V
R1
If
Vce
R2
Ib
Vb
Vin
T1
VD
D1

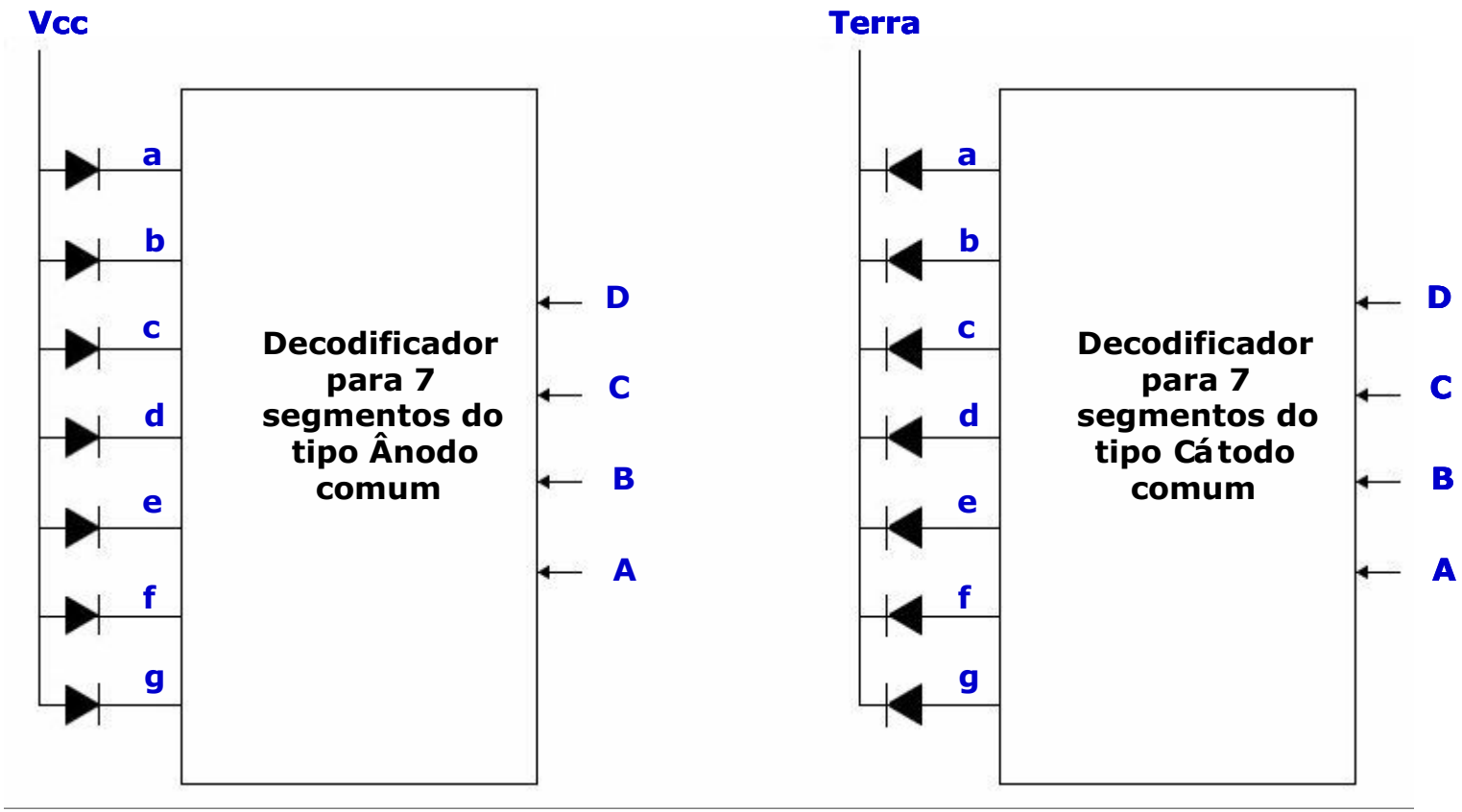

V
R
If
Vf

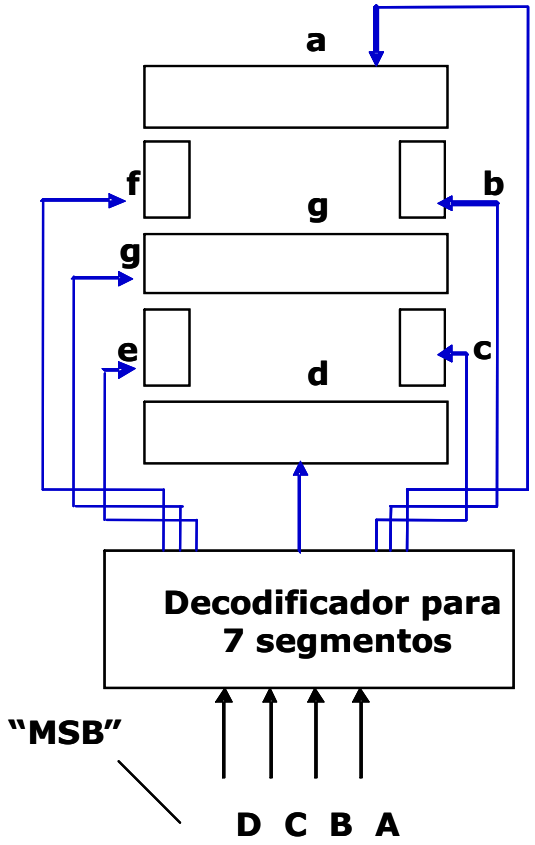

V
R
If
V1
Entrada
Vf
SN7404

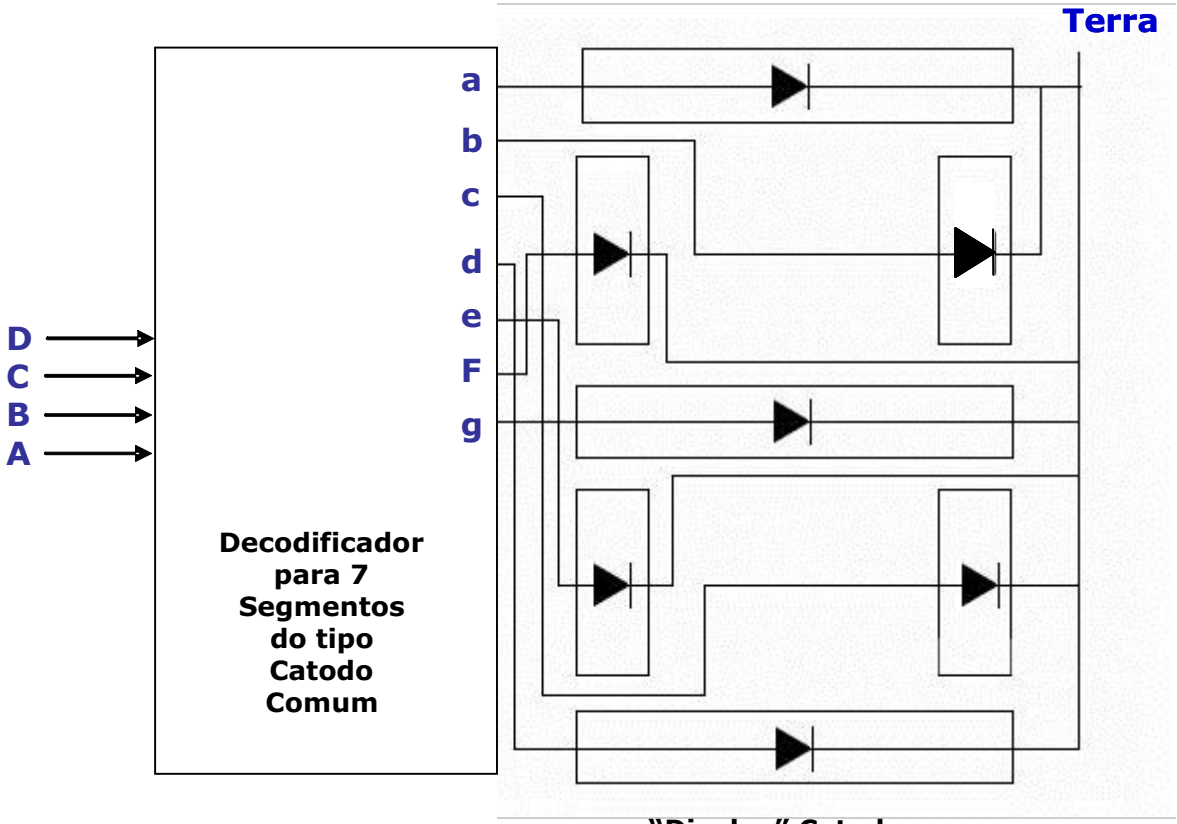
“Display”

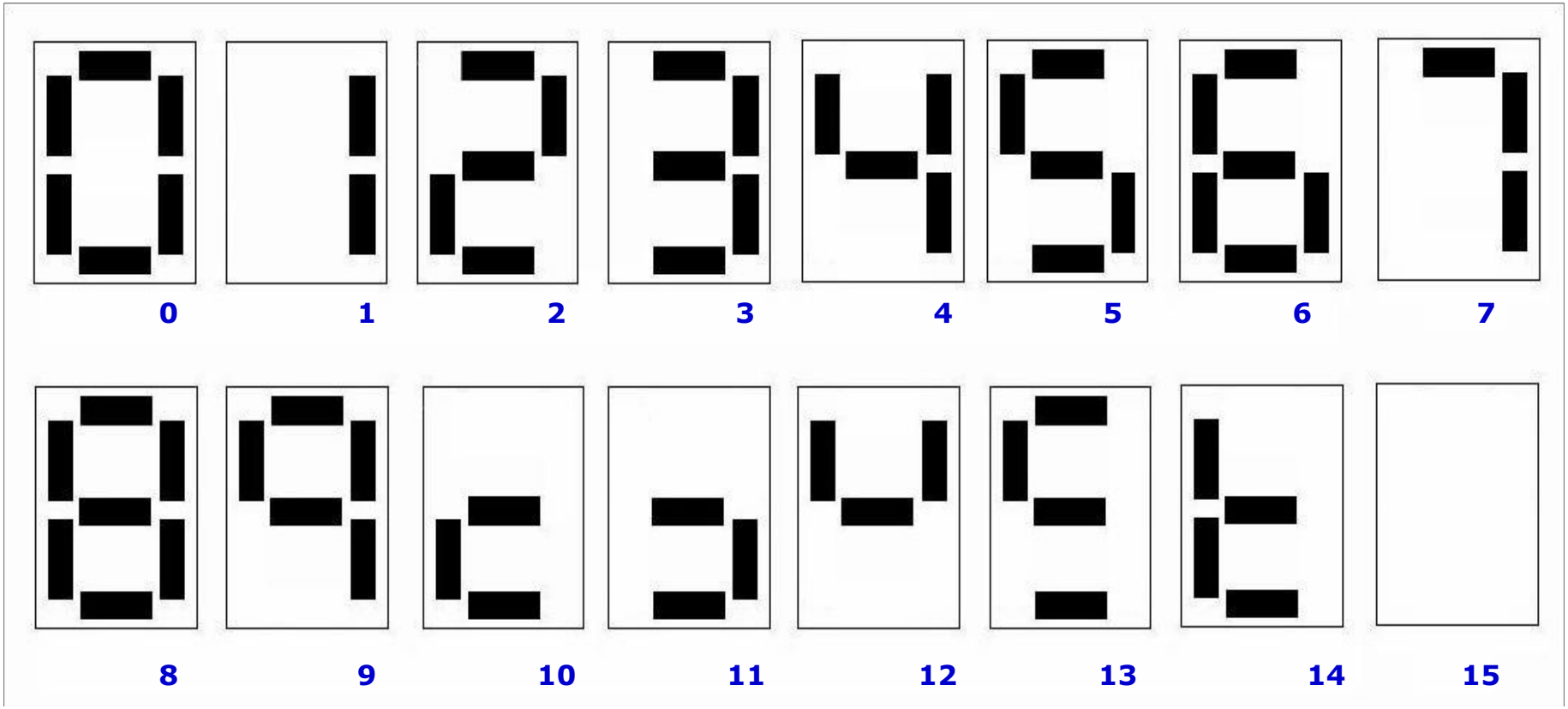


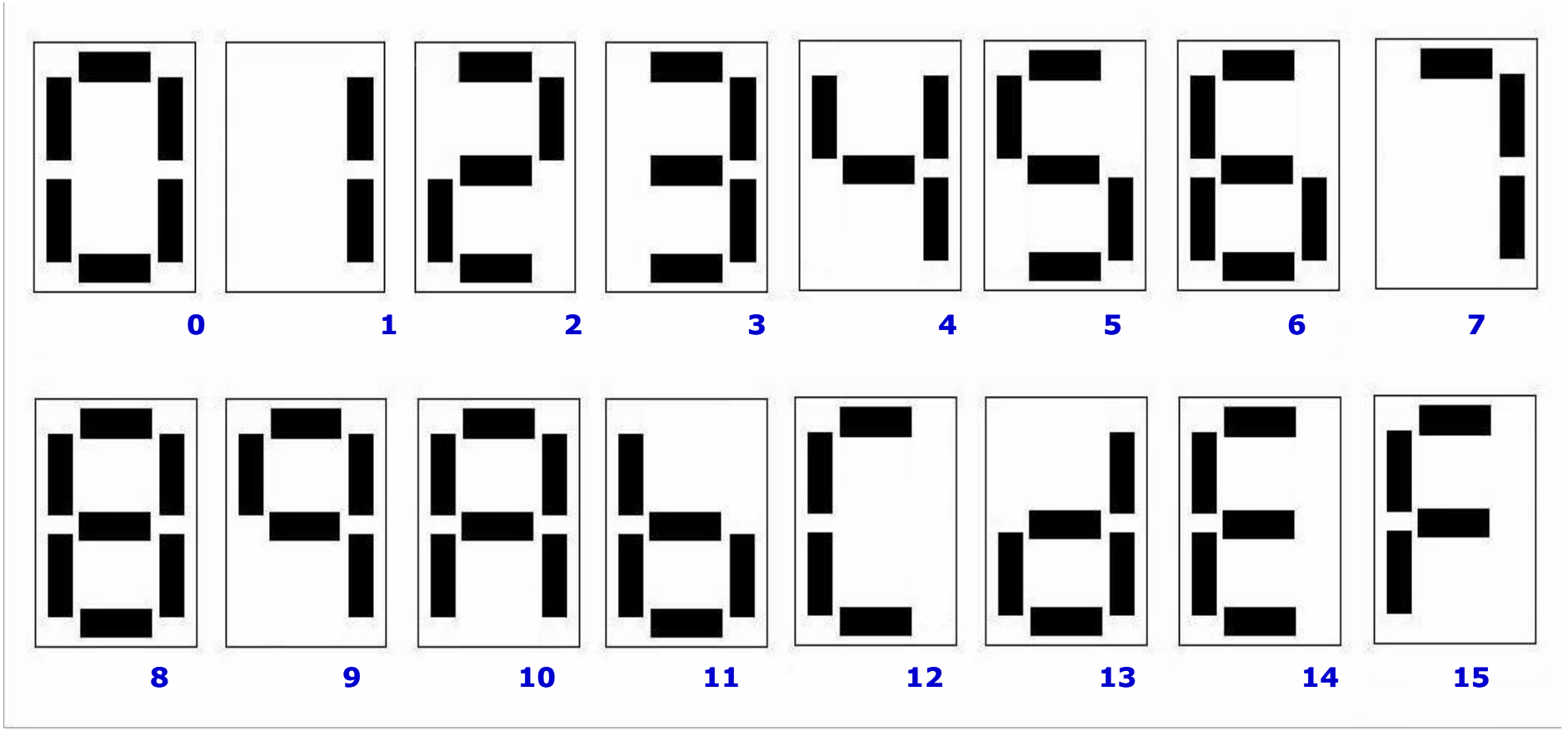



Vcc
a
b
c
d
e
f
g
Decodificador para 7 segmentos do tipo Ânodo comum
D
C
B
A
Terra
a
b
c
d
e
f
g
Decodificador para 7 segmentos do tipo Cátodo comum
D
C
B
A

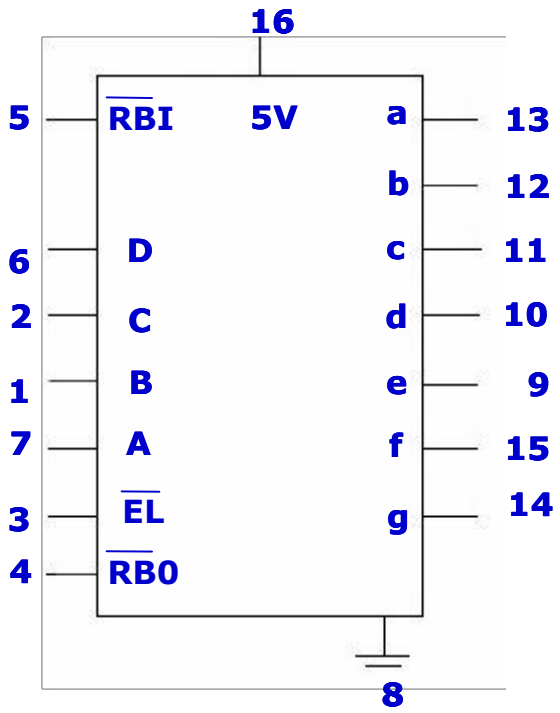

a
f
b
g
g
e
c
d
Decodificador para
7 segmentos
"MSB"
D C B A

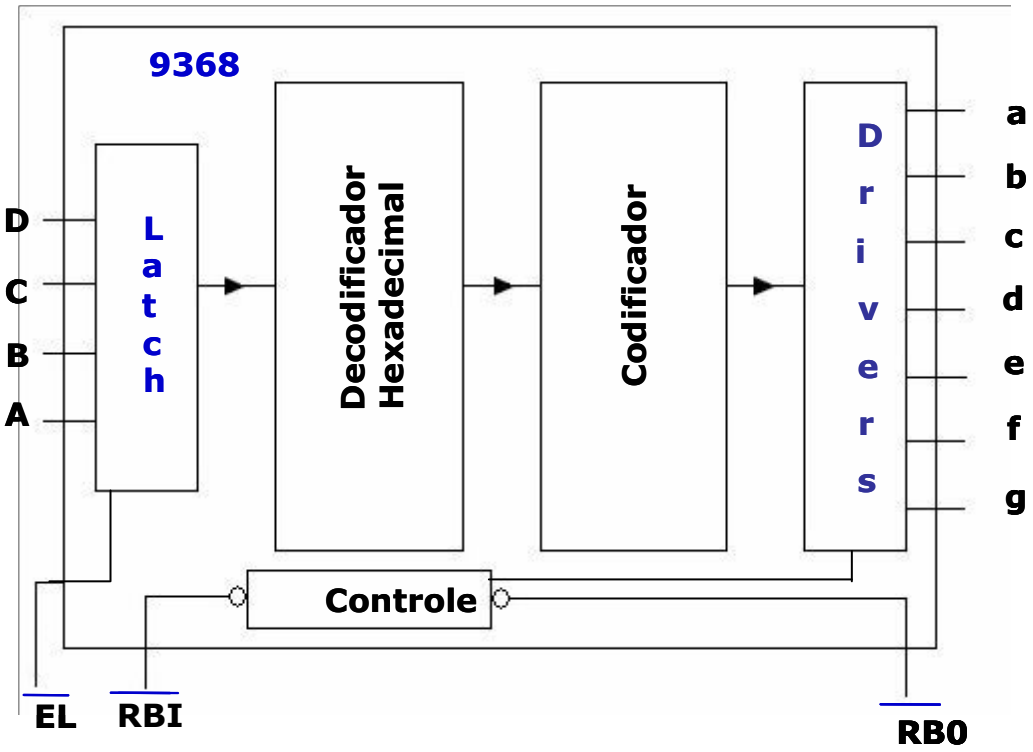

Terra
a
b
c
d
e
F
g
D
C
B
A
Decodificador para 7 Segmentos do tipo Catodo Comum
"Display" Catodo Comum


0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15


0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

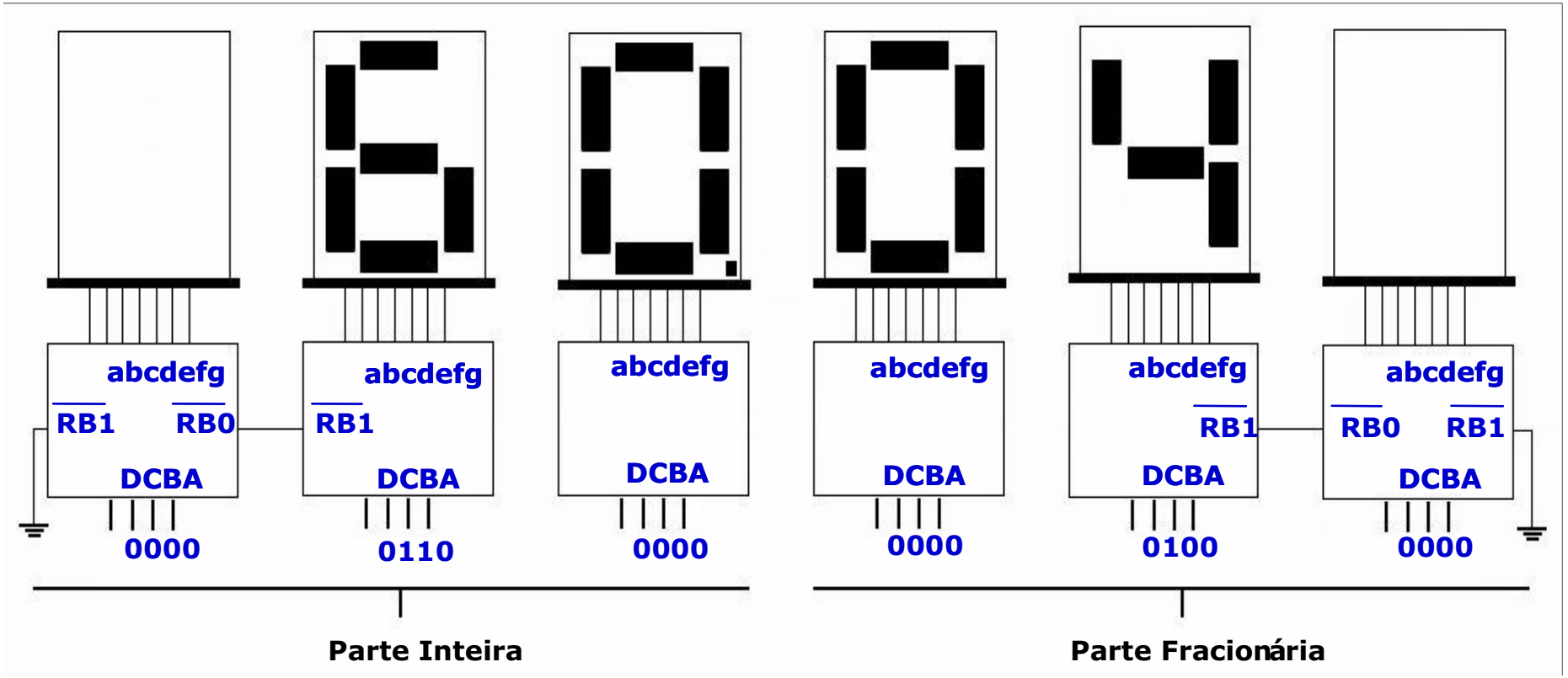
Decodificadores para Sete Segmentos

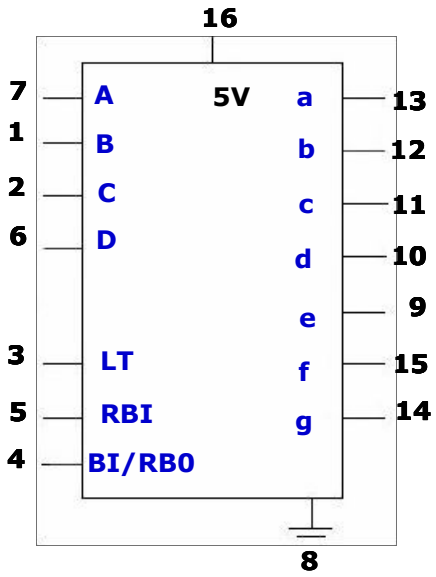


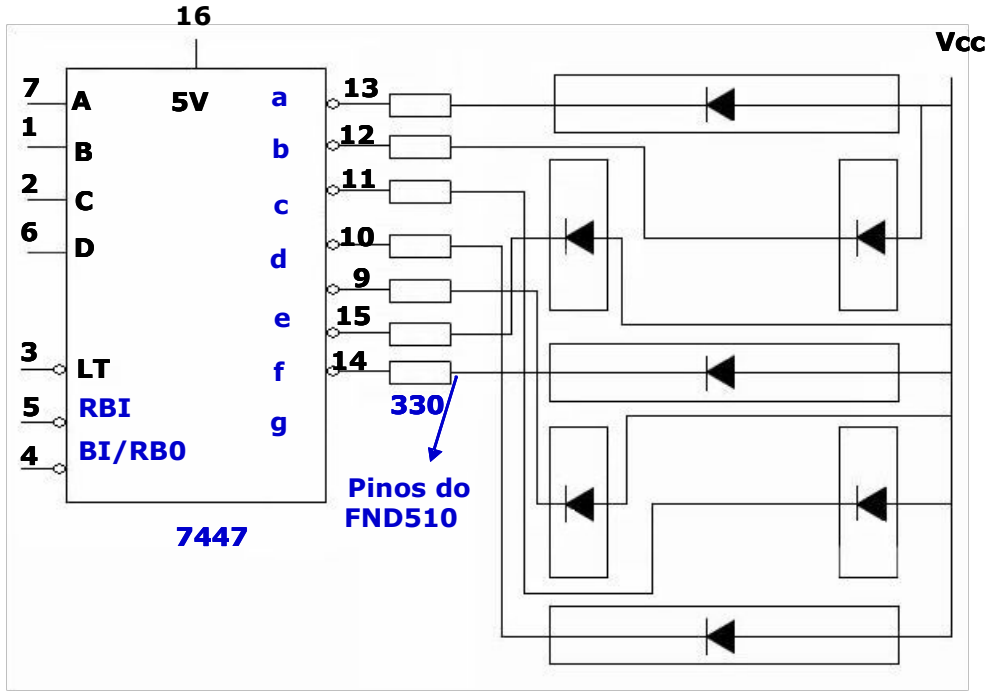


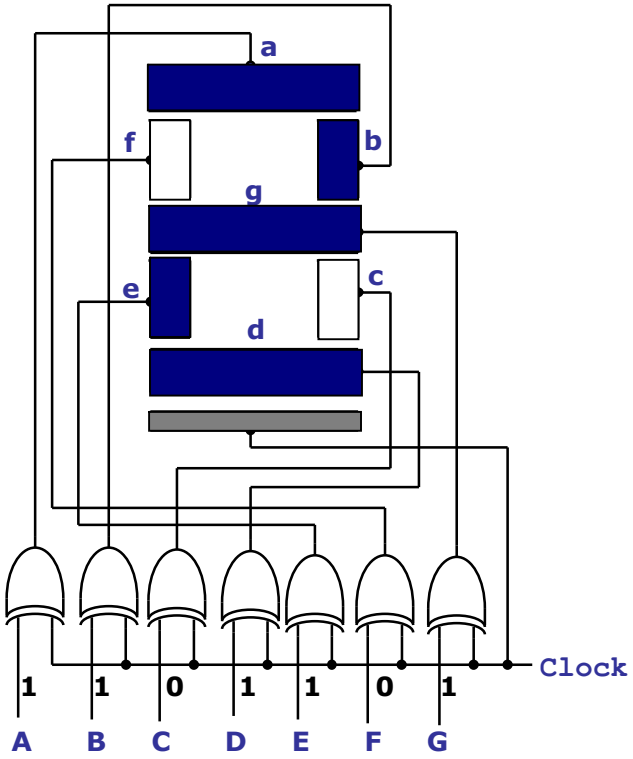
ENTRADAS				SAÍDAS		
$\overline{EL}$	$\overline{RBI}$	DCBA	Equivalente decimal	abcdefg	Visualização	$\overline{RB0}$
0	1	0000	0	1111110	0	1
0	X	0001	1	0110000	1	1
0	X	0010	2	1101101	2	1
0	X	0011	3	1111001	3	1
0	X	0100	4	0110011	4	1
0	X	0101	5	1011011	5	1
0	X	0110	6	1011111	6	1
0	X	0111	7	1110000	7	1
0	X	1000	8	1111111	8	1
0	X	1001	9	1110011	9	1
0	X	1010	10	1110111	A	1
0	X	1011	11	0011111	B	1
0	X	1100	12	1001110	C	1
0	X	1101	13	0111101	D	1
0	X	1110	14	1001111	E	1
0	X	1111	15	1000111	F	1
1	X	XXXX	-	Estável	Estável	1
0	0	0000	0	0000000	Apaga	NC
X	X	XXXX	X	0000000	Apaga	0

NC = Nenhuma conexão


abcdefg
RB1
RB0
DCBA
0000
abcdefg
RB1
DCBA
0110
abcdefg
DCBA
0000
Parte Inteira
abcdefg
DCBA
0000
abcdefg
RB1
DCBA
0100
abcdefg
RB0
RB1
DCBA
0000
Parte Fracionária


16
7
1
2
6
3
5
4
A
B
C
D
LT
RBI
BI/RB0
5V
a
b
c
d
e
f
g
13
12
11
10
9
15
14
8


16
7
1
2
6
3
5
4
A
B
C
D
LT
RBI
BI/RB0
5V
a
b
c
d
e
f
g
13
12
11
10
9
15
14
330
Pinos do
FND510
7447
Vcc


a
f
b
g
e
c
d
Clock
1
1
0
1
1
0
1
A
B
C
D
E
F
G