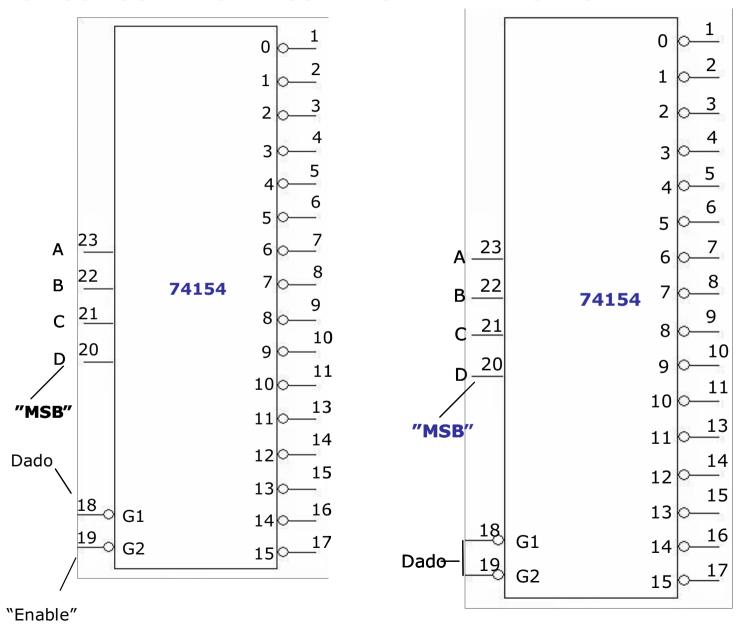
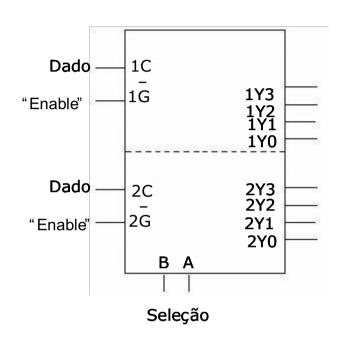


Ent	rac	las		Decimal	
S0 S	53	S2	S1	Equivalente	Destino
0	0	0	0	0	C0
0	0	0	1	1	C1
0	0	1	0	2	C2
	· · · · ·			•••••	
1	1	1	1	2 <sup>M</sup>	C(N-1)

## **CIRCUITOS INTEGRADOS DEMULTIPLEXADORES**



## Circuito Integrado 74155: Duplo Demultiplexador com Quatro Canais



1	1C		Vcc	16
2	1Ğ		2C	15
3	В		- 2G	14
4	1Y3			13
5			A 23/2	12
6	1Y2		2Y3	11
7	1Y1		2Y2	10
85 53	1Y0		2Y1	
_8_	GND	74155	2Y0	9
9				

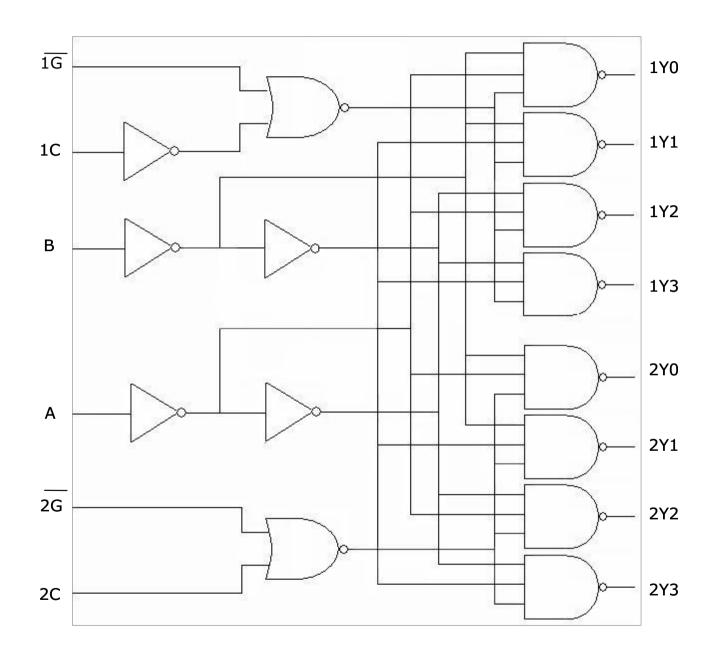
		ENTRADAS	SAÍDAS					
Sel	eção	"Enable"	Dado					
В	A	2G	2C	2Y0	2Y1	2Y2	2Y3	
Х	Х	1	Х	1	1	1	1	
0	0	0	0	0	1	1	1	
0	1	0	0	1	0	1	1	
1	0	0	0	1	1	0	1	
1	1	0	0	1	1	1	0	
Х	Х	Х	1	1	1	1	1	

		ENTRADAS	SAÍDAS					
Sel	eção	"Enable"	Dado	,				
В	A	1G	1C	1Y0	1Y1	1Y2	1Y3	
Х	Х	1	Х	1	1	1	1	
0	0	0	1	0	1	1	1	
0	1	0	1	1	0	1	1	
1	0	0	1	1	1	0	1	
1	1	0	1	1	1	1	0	
Х	Х	Х	0	1	1	1	1	

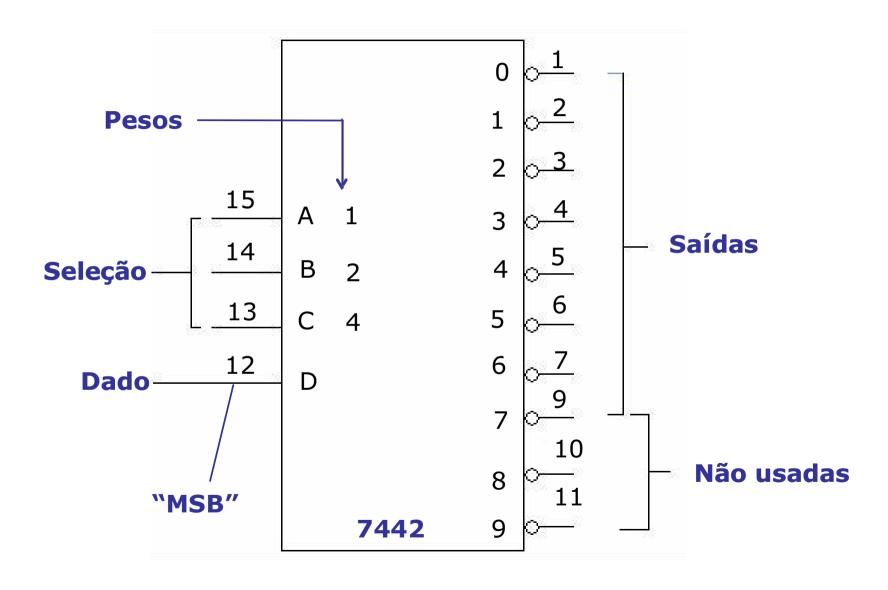
		ENTRADAS	SAÍDAS					
Sel	eção	"Enable"	Da	ido				
В	A	1G 2G	<b>1</b> C	2C	nY0	nY1	nY2	nY3
X	Х	1	Х	Х	1	1	1	1
0	0	0	1	0	0	1	1	1
0	1	0	1	0	1	0	1	1
1	0	0	1	0	1	1	0	1
1	1	0	1	0	1	1	1	0
X	X	X	0	1	1	1	1	1

Onde n=1 ou 2

Para n=1 Para n=2



## **Uso do Decodificador como Demultiplexador**



D	С	В	Α	L0	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0	1
1	0	1	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1