Spring 2022-ECGR-5146/4146-Introduction to VHDL
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LAB 3a

Multiplexer

Objective:

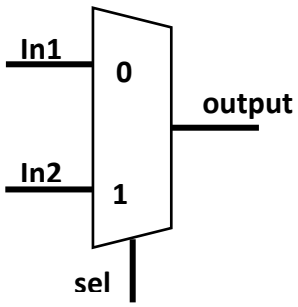
In this lab exercise you will write the design file and test bench for a 2:1 MUX.

2:1 MUX

The multiplexer or MUX is a digital switch, also called as data selector. It is a Combinational Logic Circuit with more than one input line, one output line and more than one select line. It accepts the binary information from several input lines or sources and depending on the set of select lines, a particular input line is routed onto a single output line. It consists of n input lines, m selection lines and one output line. If there are m selection lines, then the number of possible input lines is 2^m. Alternatively, we can say that if the number of input lines is equal to 2^m, then m selection lines are required to select one of n (consider $2^m = n$) input lines.

A 2-to-1 multiplexer consists of two inputs **In1** and **In2**, one select input **sel** and one output **output**. Depending on the select signal, the output is connected to either of the inputs. Since there are two input signals, only two ways are possible to connect the inputs to the outputs, so one select is needed to do these operations.

If the select line is low, then the output will be switched to **In1** input, whereas if select line is high, then the output will be switched to **In2** input. The figure below shows the block diagram of a 2-to-1 multiplexer which connects two 1-bit inputs to a common destination.



Truth Table

sel	output
0	In1
1	In2

VHDL Design

The following is the entity of a 2:1 MUX. Construct the architecture and complete the design.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.numeric_std.all;

entity mux_2x1 is
    Port ( in1 : in STD_LOGIC;
           in2 : in STD_LOGIC;
           sel : in STD_LOGIC;
           output : out STD_LOGIC);
end mux_2x1;
```

Deliverable:

PDF that includes VHDL code, Testbench and the simulation waveform of 2:1 Mux.