Spring 2022-ECGR-5146/4146-Introduction to VHDL
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LAB 4

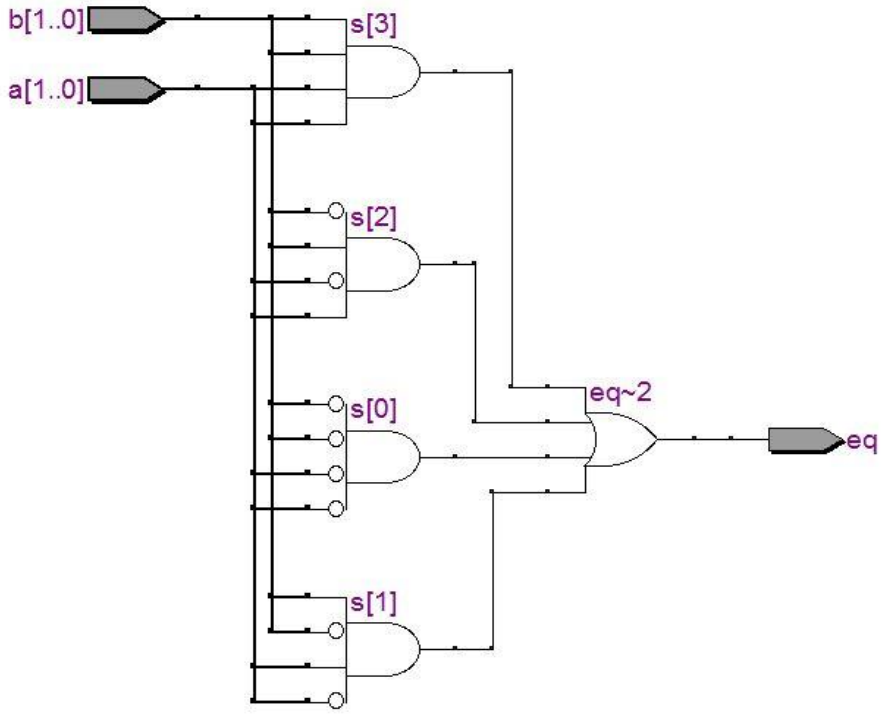
2-bit Comparator

Objective:

In this lab exercise you will write the design file and test bench for a 2-bit comparator using dataflow, structural and behavioral modeling.

2-bit Comparator

A magnitude digital Comparator is a combinational circuit that compares two digital or binary numbers to find out whether one binary number is equal, less than or greater than the other binary number. A comparator that is used to compare two binary numbers each of two bits is called a 2-bit Magnitude comparator. It consists of four inputs and three outputs to generate less than, equal to and greater than between two binary numbers. In this lab the 2-bit comparator is designed with different styles, which generates the output '1' if the numbers are equal, otherwise output is set to '0'. The circuit implementation is given below with inputs: **a [1,0], b[1,0]** and output :**eq .**



2-bit Comparator

Truth table for 2-bit comparator

a[1]	a[0]	b[1]	b[0]	eq
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

VHDL Design

The following is the entity of a 2-bit comparator. Construct the architecture using all the three different models.

(i) Dataflow Model
(ii) Behavioral Model
(iii) Structural Model

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity comparator2Bit is
        port( a, b : in std_logic_vector(1 downto 0);
                eq : out std_logic
        );
end comparator2Bit;
```

i. Dataflow modeling

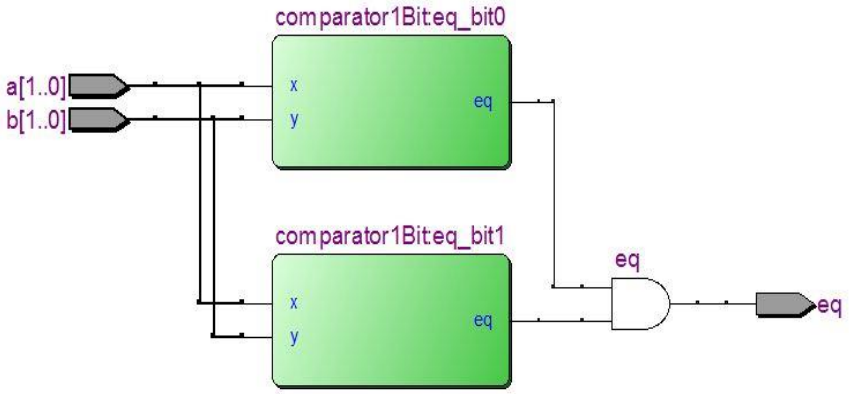
In this modeling style, the relation between input and outputs are defined using signal assignments. Signals: **s0,s1,s2 and s3** can be used to construct the architecture for the dataflow model.

ii. Behavioral modeling

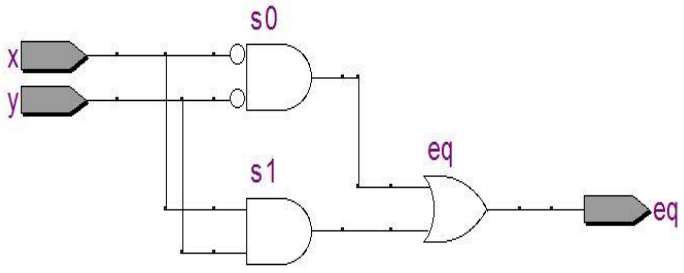
In behavioral modeling, the **'process'** keyword is used and all the statements inside the process statement executes sequentially and is known as "sequential statements". Various conditional and loop statements can be used inside the process block such as **if, while** etc.

iii. Structural modeling

In structural modeling pre-defined designs are used to create the new designs. Implementation of a module as a composition of subsystems with component instantiation is done in this model. To design the 2-bit comparator using structural modeling make use of the 1-bit comparator provided below.
The simplified 2-bit comparator circuit for structural modeling uses two 1-bit comparator is:



1-bit Comparator VHDL code:



x	y	eq
0	0	1
0	1	0
1	0	0
1	1	1

```
library ieee;
use ieee.std_logic_1164.all;
entity comparator1Bit is
        port( x, y : in std_logic;
        eq : out std_logic );
end comparator1Bit;
architecture dataflow1Bit of comparator1Bit is
signal s0, s1: std_logic;
begin
        s0 <= (not x) and (not y);
        s1 <= x and y;
        eq <= s0 or s1;
end dataflow1Bit;
```

Deliverable:

PDF that includes:

VHDL code and Testbench with the simulation waveform for:

(i) Dataflow Model
(ii) Behavioral Model
(iii) Structural Model