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ECGR 4146: Introduction to VHDL
Lab 4: 2-Bit Comparator

Note: (I had an issue trying to run the design sources within the same project, so I created three separate project folders. For some reason, it would not work well if I tried to change the architecture name to something other than Behavioral)

VHDL Code for Dataflow Model:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity comparator2bitDataflow is
    Port ( a : in STD_LOGIC_VECTOR(1 downto 0);
           b : in STD_LOGIC_VECTOR(1 downto 0);
           eq : out STD_LOGIC);
end comparator2bitDataflow;
architecture Behavioral of comparator2bitDataflow is
  signal s0, s1, s2, s3: std_logic;
begin
  s0 <= (not a(1)) and (not a(0)) and (not b(1)) and (not b(0));
  s1 <= (not a(1)) and a(0) and (not b(1)) and b(0);
  s2 <= a(1) and (not a(0)) and b(1) and (not b(0));
  s3 <= a(1) and a(0) and b(1) and b(0);
  eq <= s0 or s1 or s2 or s3;
end Behavioral;
```

VHDL Testbench Code for Dataflow Model:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity comparator2bitDataflowsim is
-- Port( );
end comparator2bitDataflowsim;
architecture Behavioral of comparator2bitDataflowsim is
signal a : std_logic_vector(1 downto 0);
 signal b : std_logic_vector(1 downto 0);
 signal eq : std_logic;
begin
p0:entity work.comparator2bitDataflow(Behavioral) port map(a=>a,b=>b,eq=>eq);
process
begin
    A <= "00";
    B <= "00";
    wait for 20ns;
    A <= "00";
    B <= "01";
    wait for 20ns;
    A <= "00";
    B <= "10";
    wait for 20ns;
```

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```
    A <= "00";
    B <= "11";
    wait for 20ns;

    A <= "01";
    B <= "00";
    wait for 20ns;
    A <= "01";
    B <= "01";
    wait for 20ns;
    A <= "01";
    B <= "10";
    wait for 20ns;
    A <= "01";
    B <= "11";
    wait for 20ns;

    A <= "10";
    B <= "00";
    wait for 20ns;
    A <= "10";
    B <= "01";
    wait for 20ns;
    A <= "10";
    B <= "10";
    wait for 20ns;
    A <= "10";
    B <= "11";
    wait for 20ns;

    A <= "11";
    B <= "00";
    wait for 20ns;
    A <= "11";
    B <= "01";
    wait for 20ns;
    A <= "11";
    B <= "10";
    wait for 20ns;
    A <= "11";
    B <= "11";
    wait for 20ns;
  end process;
end Behavioral;
```

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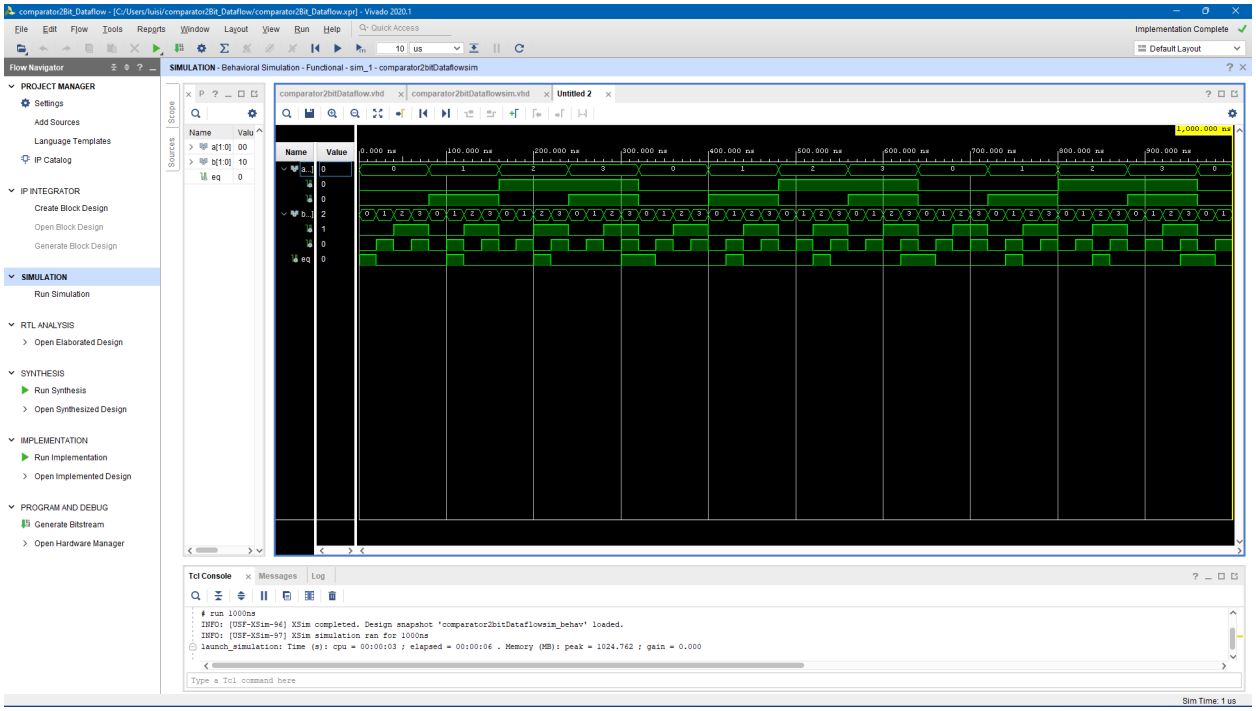
Simulation Waveform of Dataflow Model



VHDL Code for Behavioral Model:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity comparator2bitBehavorial is
    Port ( a : in STD_LOGIC_VECTOR(1 downto 0);
           b : in STD_LOGIC_VECTOR(1 downto 0);
           eq : out STD_LOGIC);
end comparator2bitBehavorial;
architecture Behavioral of comparator2bitBehavorial is
begin
process(a,b)
  begin
    if (a(0)=b(0)) and (a(1)=b(1)) then
      eq <= '1';
    else
      eq<='0';
    end if;
  end process;
end Behavioral;
```

VHDL Testbench Code for Behavioral Model:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity comparator2bitBehavorialsim is
```

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```
-- Port ( );
end comparator2bitBehavorialsim;
architecture Behavioral of comparator2bitBehavorialsim is
 signal a : std_logic_vector(1 downto 0);
 signal b : std_logic_vector(1 downto 0);
 signal eq : std_logic;
begin
p0:entity work.comparator2bitBehavorial(Behavioral) port map(a=>a,b=>b,eq=>eq);
process
begin
    A <= "00";
    B <= "00";
    wait for 20ns;
    A <= "00";
    B <= "01";
    wait for 20ns;
    A <= "00";
    B <= "10";
    wait for 20ns;
    A <= "00";
    B <= "11";
    wait for 20ns;

    A <= "01";
    B <= "00";
    wait for 20ns;
    A <= "01";
    B <= "01";
    wait for 20ns;
    A <= "01";
    B <= "10";
    wait for 20ns;
    A <= "01";
    B <= "11";
    wait for 20ns;

    A <= "10";
    B <= "00";
    wait for 20ns;
    A <= "10";
    B <= "01";
    wait for 20ns;
    A <= "10";
    B <= "10";
    wait for 20ns;
    A <= "10";
    B <= "11";
    wait for 20ns;

    A <= "11";
    B <= "00";
    wait for 20ns;
    A <= "11";
    B <= "01";
    wait for 20ns;
    A <= "11";
    B <= "10";
    wait for 20ns;
```

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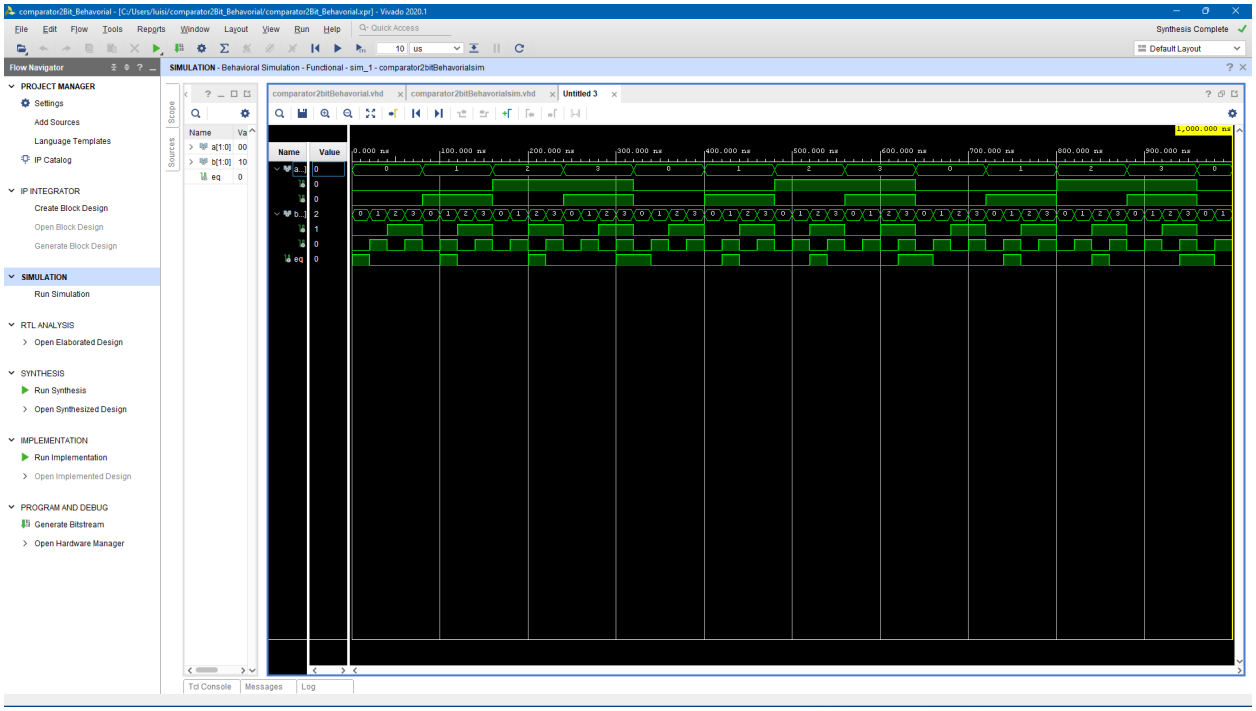
```
    A <= "11";
    B <= "11";
    wait for 20ns;
  end process;
end Behavioral;
```

Simulation Waveform of Behavioral Model



VHDL Code for Structural Model

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity comparator2BitStructural is
    Port ( a : in STD_LOGIC_VECTOR(1 downto 0);
           b : in STD_LOGIC_VECTOR(1 downto 0);
           eq : out STD_LOGIC);
end comparator2BitStructural;
architecture Behavioral of comparator2BitStructural is
 signal s0, s1: std_logic;
begin
  eq_bit0: entity work.comparator1Bit
    port map (a=>a(0), b=>b(0), eq=>s0);
  eq_bit1: entity work.comparator1Bit
    port map (a=>a(1), b=>b(1), eq=>s1);
  eq <= s0 and s1;
end Behavioral;
```

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VHDL Testbench Code for Structural Model

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity comparator2BitStructuralsim is
-- Port ( );
end comparator2BitStructuralsim;
architecture Behavioral of comparator2BitStructuralsim is
signal a : std_logic_vector(1 downto 0);
 signal b : std_logic_vector(1 downto 0);
 signal eq : std_logic;
begin
p0:entity work.comparator2bitStructural(Behavioral) port map(a=>a,b=>b,eq=>eq);
process
begin
    A <= "00";
    B <= "00";
    wait for 20ns;
    A <= "00";
    B <= "01";
    wait for 20ns;
    A <= "00";
    B <= "10";
    wait for 20ns;
    A <= "00";
    B <= "11";
    wait for 20ns;

    A <= "01";
    B <= "00";
    wait for 20ns;
    A <= "01";
    B <= "01";
    wait for 20ns;
    A <= "01";
    B <= "10";
    wait for 20ns;
    A <= "01";
    B <= "11";
    wait for 20ns;

    A <= "10";
    B <= "00";
    wait for 20ns;
    A <= "10";
    B <= "01";
    wait for 20ns;
    A <= "10";
    B <= "10";
    wait for 20ns;
    A <= "10";
    B <= "11";
    wait for 20ns;

    A <= "11";
    B <= "00";
    wait for 20ns;
    A <= "11";
```

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```
    B <= "01";
    wait for 20ns;
    A <= "11";
    B <= "10";
    wait for 20ns;
    A <= "11";
    B <= "11";
    wait for 20ns;
  end process;
end Behavioral;
```

Simulation Waveform of Structural Model