Spring 2022-ECGR-5146/4146-Introduction to VHDL
Dr. Fareena Saqib

LAB 5

Ripple Carry Adder

Objective:

In this lab you will design an adder of two 8-bit numbers, that outputs the sum and carry by using structural modeling.

To construct the adder using structural modeling, first you need to:

1. Design a Half Adder

2. Design a 1-bit Full Adder using 2 Half Adders

3. Design an 8-bit Ripple Carry Adder using 1-bit Half adder and 1-bit Full adders.

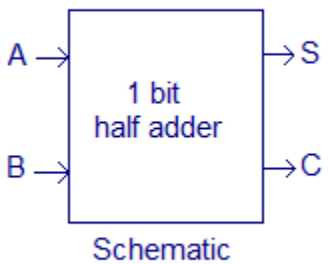
4. Write the Test Bench for Half adder, Full Adder and 8-bit adder.

Half Adder:

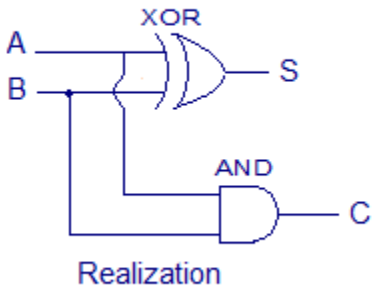
Half adder is a combinational arithmetic circuit that adds two numbers (A and B) and produces a sum bit (S) and carry bit (C) as the output. The truth table, schematic representation and XOR//AND realization of a half adder is given below.

Inputs		Outputs	
A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

Truth table



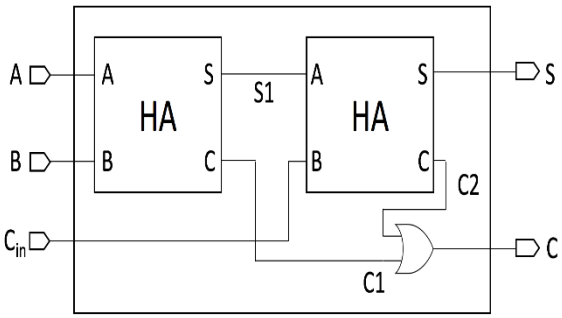
Schematic



Realization

Full Adder:

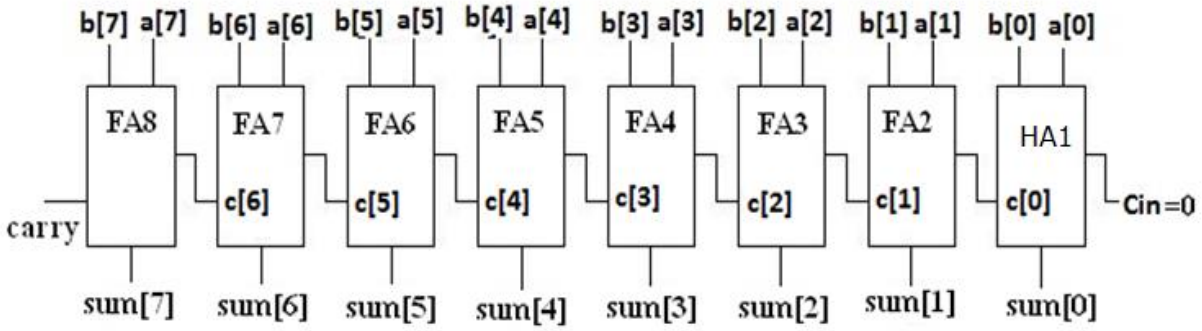
The 1 bit full-adder circuit adds three one-bit binary numbers (A, B, Cin) and outputs two one-bit binary numbers, a sum (S) and a carry (Cout). The Truth Table for full adder is given below and it can be constructed with 2 half adder Port mapping into full adder.



Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Ripple Carry Adder:

Ripple Carry Adder is a combinational logic circuit that is used for adding two n-bit binary numbers. An 8-bit ripple carry adder can be implemented using one half adder and seven one-bit full adders. The block diagram and truth table of the 8-bit ripple carry adder is given below.



VHDL Design

The following is the entity of an 8-bit ripple carry adder. Construct the architecture and complete the design using structural modeling. Make use of the generic and generate statements to build the design.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity R_Adder is
generic (WIDTH: positive:=7);
Port ( a : in STD_LOGIC_VECTOR (WIDTH downto 0);
       b : in STD_LOGIC_VECTOR (WIDTH downto 0);
       cin: in STD_LOGIC;
        s : out STD_LOGIC_VECTOR (WIDTH downto 0);
       cout : out STD_LOGIC);
end R_Adder;
```

Deliverables:

PDF that includes VHDL codes, Testbench and the simulation waveforms of:

i. Half Adder
ii. Full Adder
iii. Ripple Carry Adder