CHARLOTTE

Spring 2022-ECGR-5146/4146-Introduction to VHDL
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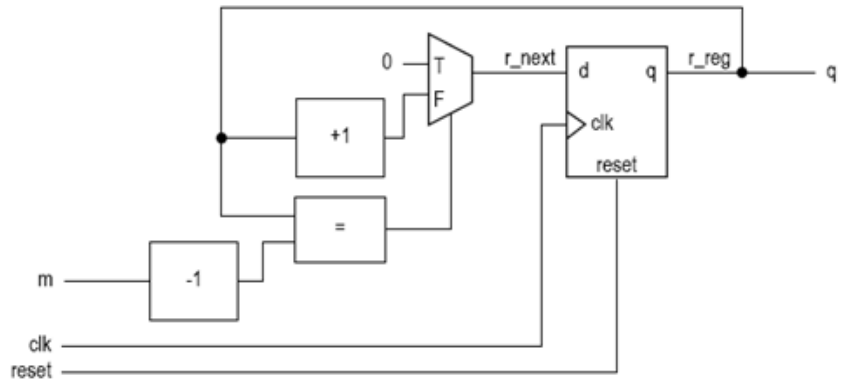
LAB 6

Counter

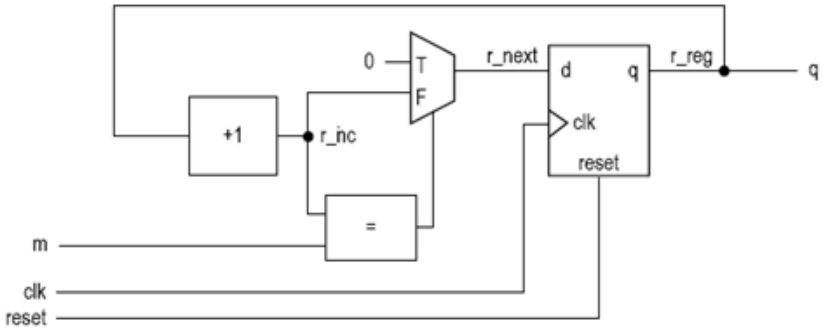
Objective:

In this lab you will design a counter that circulates through a sequence. Instead of using all possible states as discussed in lecture **9-UNCC-VHDL-Lecture6-Sequential Circuits -Free-Running Binary Counter,** which counts from 0-15, sometimes it is required to have a counter to circulate through a subset of the states.

A mod-m counter is a counter in which the value of **m** is specified. For example, a 4-bit mod-m counter is specified by a 4-bit signal(m) which is interpreted as an unsigned number. The maximal number in the counting sequence of a mod-m counter is m-1. Thus, when the counter reaches m-1, the next state should be 0. The block diagram of the mod-m counter is given below.



(a) Block diagram of initial design



(b) Block diagram of more efficient design

In figure a, the next state logic consists of an incrementor, a decrementor and a comparator. Here,

r_reg = (unsigned (m)-1)

This can be further revised by eliminating the decrementor as shown in figure b and r_reg+1 becomes

r_reg+1 = unsigned(m)

and

r_inc <= r_reg+1

With the above example construct a counter in which:

a) A counter whose state circulates from 0 to m-1 and then repeats. Example: 0-12

b) A counter whose state circulates from n to m-1 and then repeats. Example: 6-15

VHDL Design

The following is the entity of a mod-m counter. Construct the architecture and complete the design.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL ;
generic (mod: positive := 3 );
entity m_counter is
port (
        clk, reset: in std-logic;
        m: in std-logic-vector ( mod downto 0) ;
        q : out std-logic-vector (mod downto 0 )
    );
end m_counter ;
```

Deliverables:

PDF that includes VHDL codes, Testbench and the simulation waveforms for the counter implemented for part a and b.