Project 2:

Luis Umana

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Introduction

The purpose of the project is to design analyze, and layout an accumulator. The accumulator required an 8-bit integer input and a 12-bit integer output that would either be twos-complement or unsigned, the design of the project was intended for unsigned integers as well as a clock and reset signal which should be synchronous or asynchronous. VDD must be at 1V, overflow output should have a maximum value of 4095, pins on the layout should be in metal 1, 2, or 3, and the design must be optimized for area, energy, or speed. The final requirements are fairly standard; the function of the design should be edge trigged, and the layout must be DRC and LVS clean.

The report will cover the following sections: design, simulation results, discussion, and the conclusion. The design section will cover the schematics of the components of the accumulator, reasoning of designs, the testbench, and layout. The simulation results will just show the overall results collected from the accumulator as well as measurements. The discussion sections cover the overall challenges and solutions meet throughout the project. Finally, the conclusion section will cover what the project itself has achieved.

Design

The designs shown in figure 1 shows a side-by-side comparison of the example. Since this accumulator is designed for unsigned integers, the two-bit register would be replaced by a one-bit register. The one-bit register eliminates the need for the underflow; however, this will arguably make the accumulator less efficient and accurate compared to a stronger design.

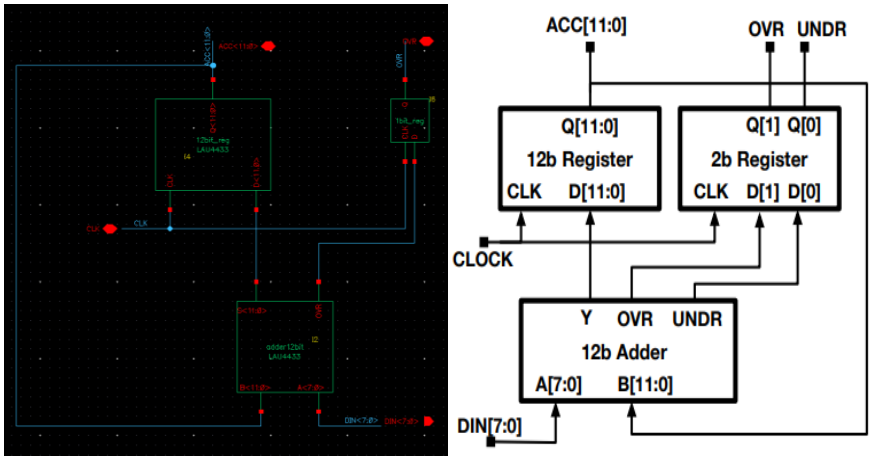

Figure 1: Schematic of the Accumulator vs Example provided

The 12-bit adder was made from 12 full adders, and essentially followed the same design shown in the demo adder videos. Figure 2 shows the entire schematic of the adder, while figure 3 shows the initial set up of the first three adders and figure 4 shows the last three adders of the design. As shown in figure 4, since we are required to have 8 inputs, the last 4 A pins in the 12-bit adder were grounded.

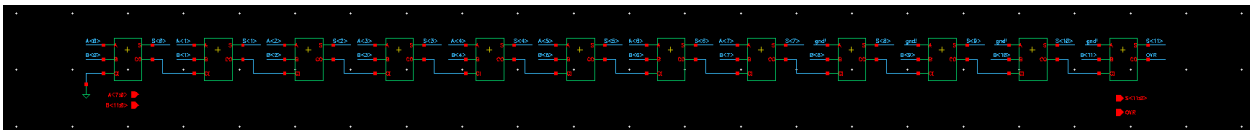

Figure 2: Schematic of the 12-bit Adder

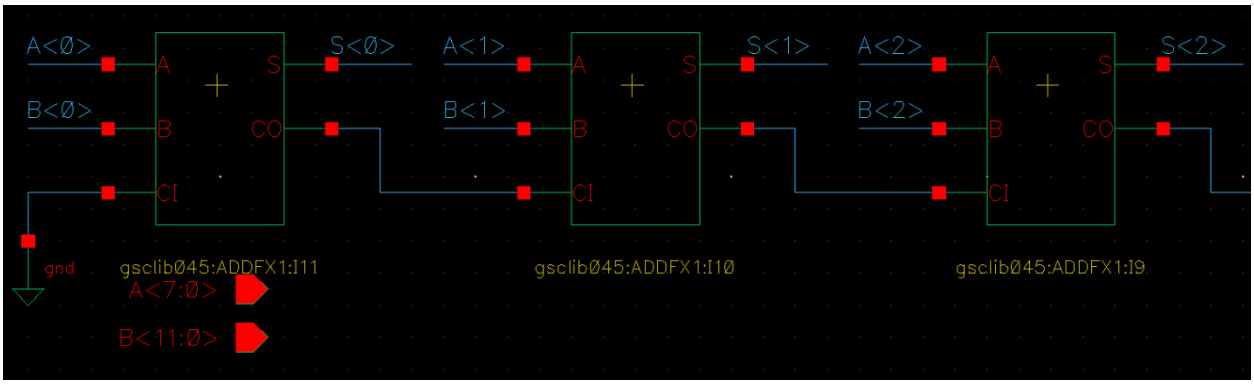

Figure 3: In depth view of the initial 3 Adders

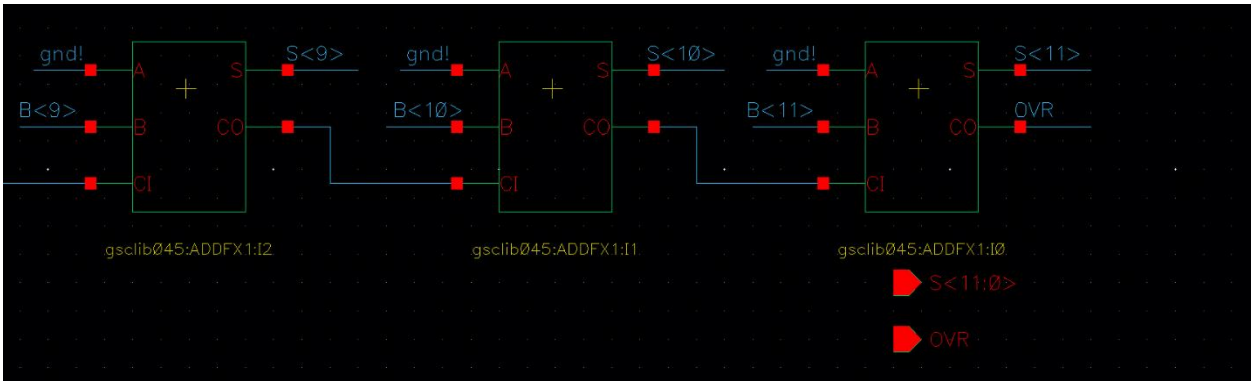

Figure 4: In depth view of the last 3 Adders

Due to a change in the requirements, the registers in figures 5 and 6 were changed to not include a reset in the designs. Both registers will now be unable to reset, which would normally be a poor design choice for efficiency however the focus of the design is geared more towards

functionality for the data. Figure 7 and 8 shows a better view of the first and last 3 registers of the 12-bit schematic.

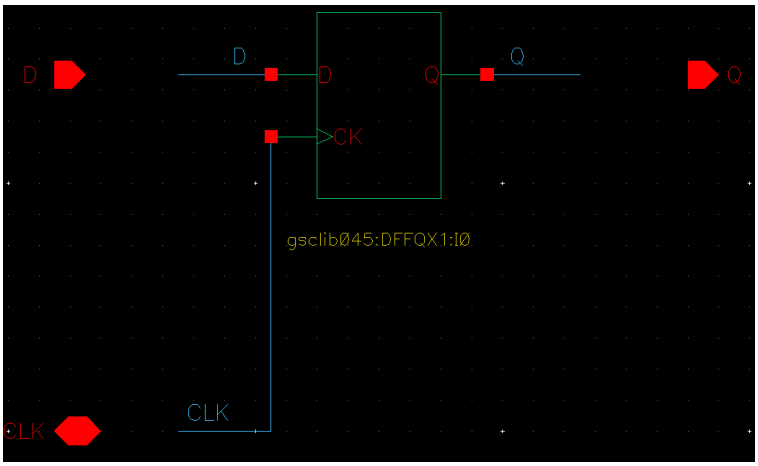

Figure 5: Schematic of 1-bit registers

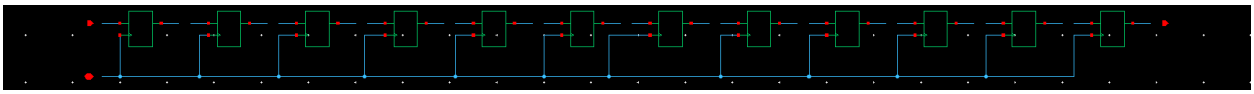

Figure 6: Schematic of 12-bit registers

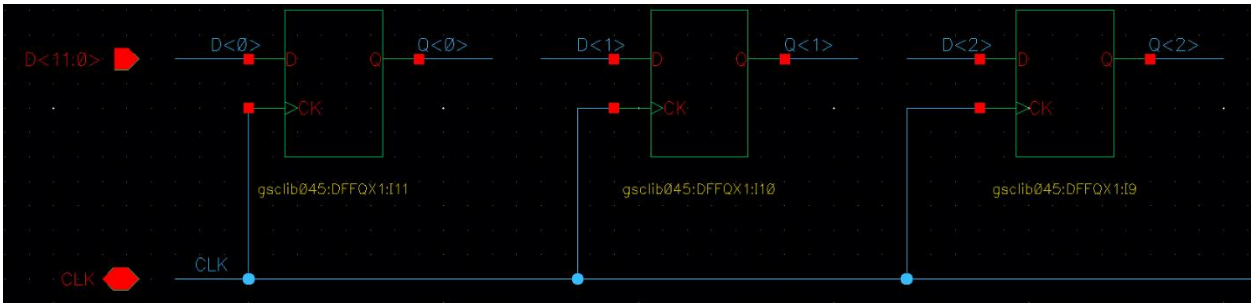

Figure 7: In depth view of the first 3 Registers

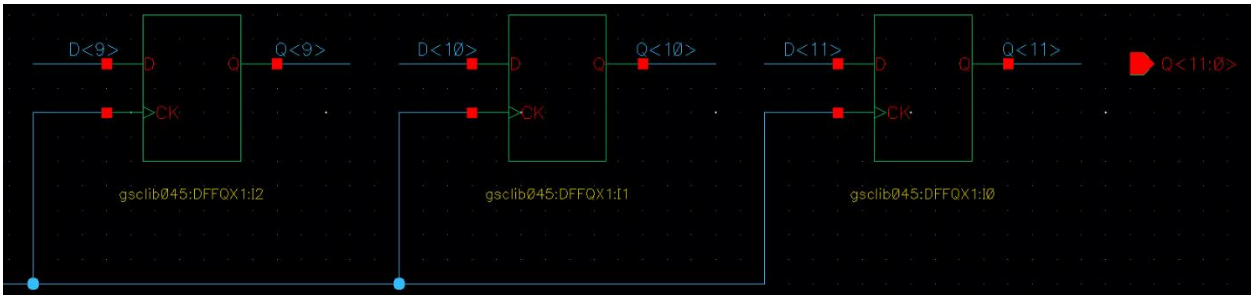

Figure 8: In depth view of the last 3 Registers

Once every component of the accumulator was created, the testbench and layout were created. Figure 9 shows the schematic of the accumulator. Figure 10 and 11 shows the complete layout of the accumulator as well as the clean DRC and LVS.

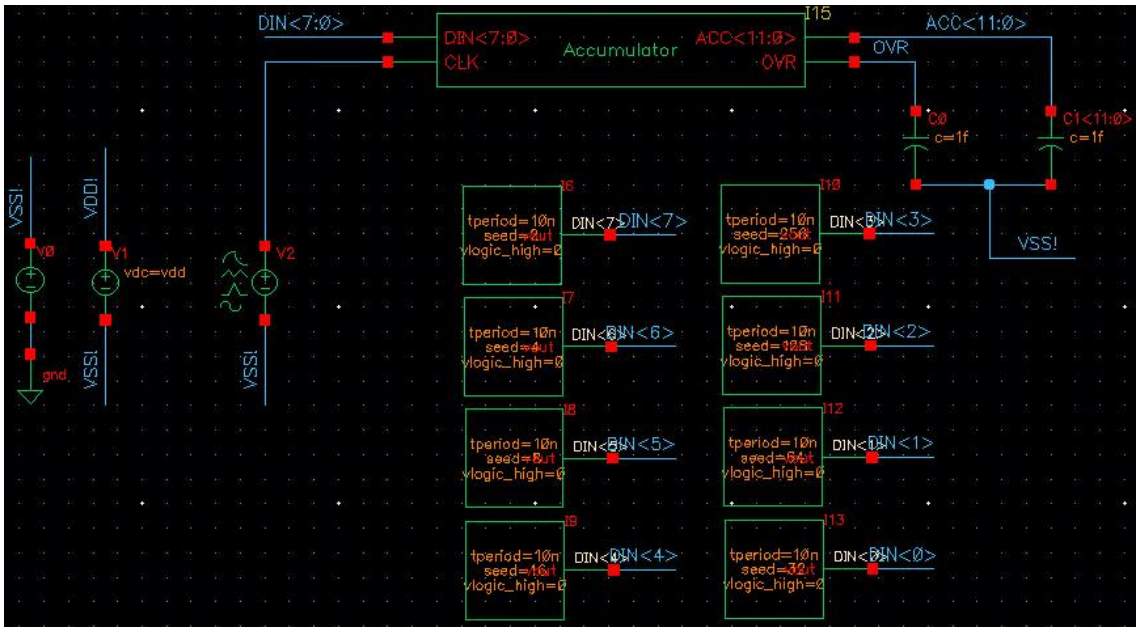

Figure 9: Test bench of the Accumulator

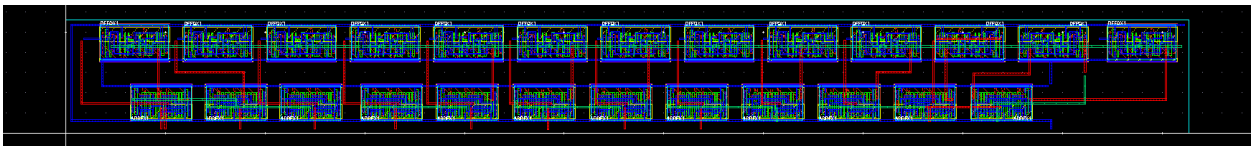

Figure 10: Layout of the Accumulator

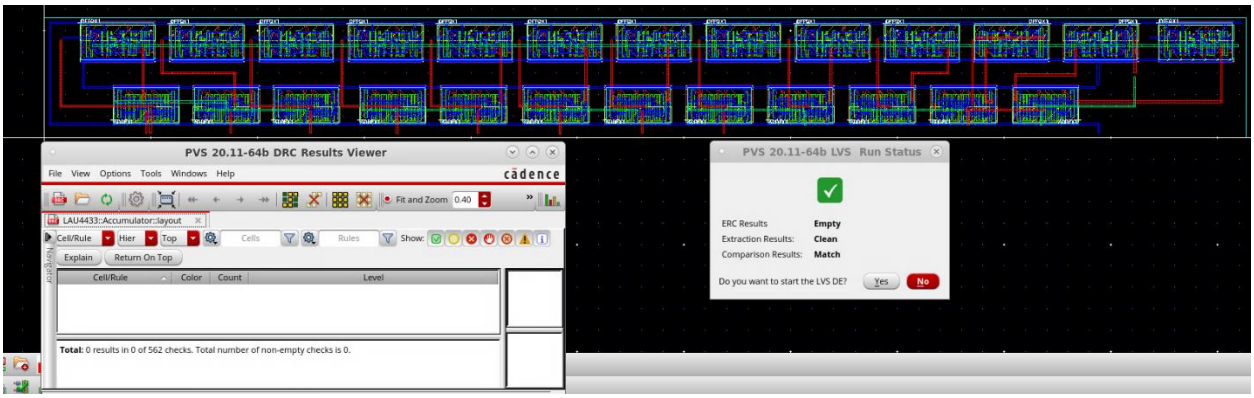

Figure11: Layout with DRC and LVS

Simulation Results

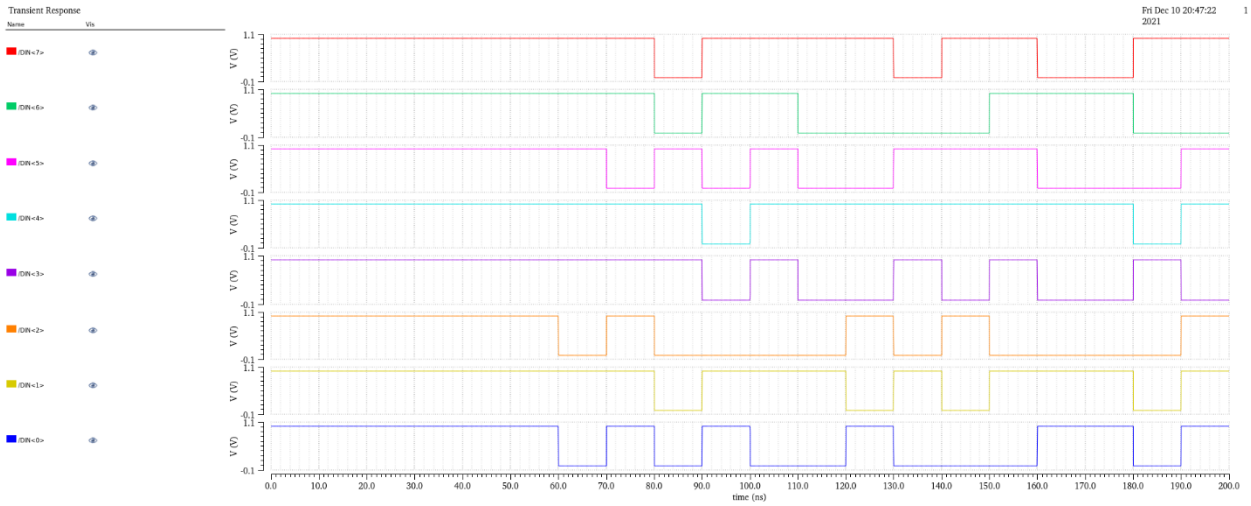

Figure12: Plot of only DIN

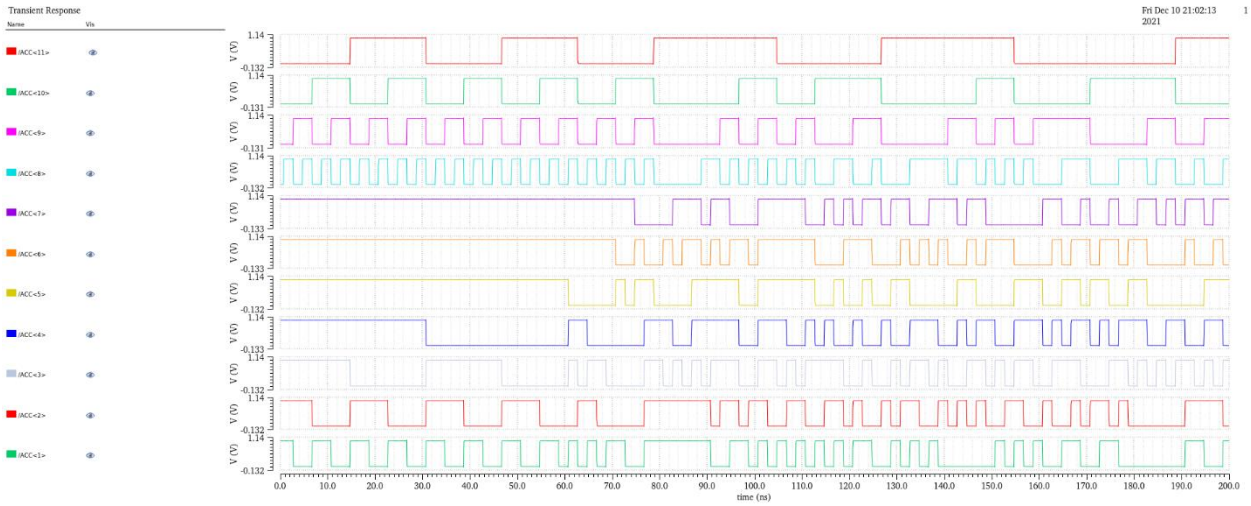

Figure 13: Plot of only ACC

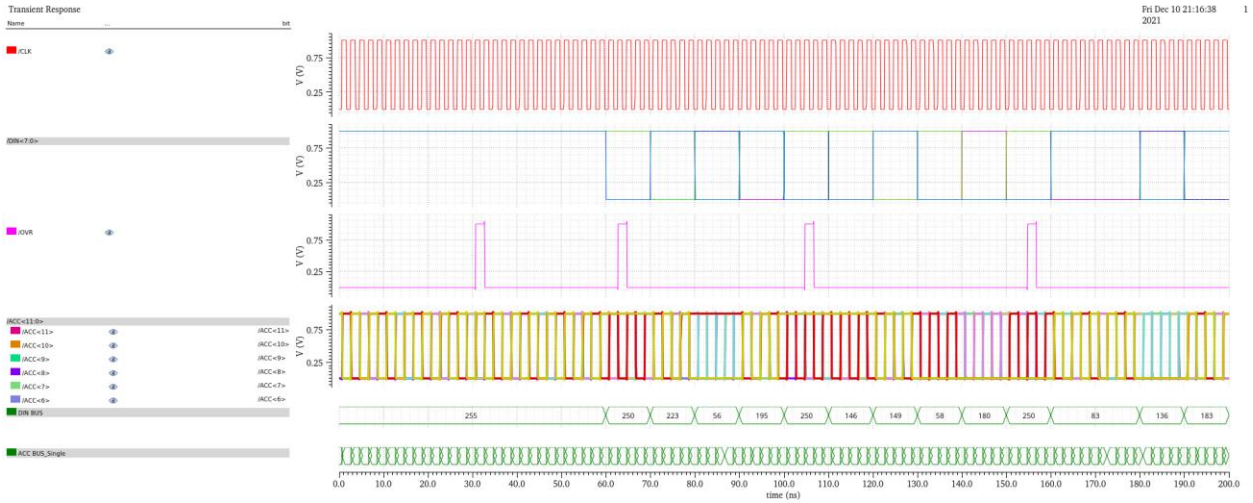

Figure 14: Plot of CLK, OVR, DIN<7:0, AND ACC <11:0>

Maximum Clock Frequency	**100ps**
Energy per Cycle	**6.12 pJ/s**
Supply leakage current	**2.0188 nA**
Dynamic supply current	**163.278uA**
Layout area	**316.03935**

Table 1: Measurements that were required.

Discussion and Troubleshooting

In figure 15, we can see that both the CLK and the output of the accumulator were producing no results. These were caused by two major issues. The first issue was that I had grounded all of the reset pins since the requirements no longer need them, but this would cause the system to constantly be resetting regardless of input. This was fixed by changing the registers to one's that did not include a reset pin. The second issue was a glaring oversight as my TCLK was set to equal 1 instead of 1n. Besides needing to constantly redesign the layout, there were not that many problems needed to be dealt with once those two major issues were resolved.

Figure 15: Plot of CLK, OVR, DIN<7:0, AND ACC <11:0>

Conclusions

The purpose of the project was to design and layout an accumulator with unsigned integers. The results shows that the accumulator is functional, but that the results itself is not perfect due to the design. Looking at the overflow in figure 14, it shows that there is an abnormal spike whenever it starts to rise and fall. It may not be visible in figure 14, but the CLK also seemed slightly rigged whenever I had my plotted my results. A final issue to address is a slightly high energy per cycle and dynamic current where both values seemed a tad bit high. However given that a majority of the plots are acting as expected, we can consider that the accumulator successful works despite a few minor issues.

References

None