ECGR 4433/5133 Project 2: Digital Accumulator

Due Wed. Dec. 8, 2021
Last updated Nov. 26, 2021

In this project you will design, verify, and layout an accumulator, which calculates a running sum of binary numbers delivered to its input.

- Students of ECGR 4433 may work individually or in teams of two and can design the accumultor to operate on either signed twos-complement or unsigned integers.
- Students of ECGR 5133 may perform the project individually and design for unsigned integers, or work in teams of two and design for signed integers.
- You may discuss the concepts with other students, but you should not share designs outside of your group.
- The accumulator should be designed using the Cadence 45 nm Generic PDK used for other class assignments.
- You can use the provided 'gsclib045' standard cell library, which includes many gates. See notes below.

Specifications

Design your accumulator to meet the following specifications.

- $V_{DD} = 1.0\ V$
- Inputs are 8-bit integers, either signed twos-complement or unsigned, as determined above.
- The running sum output is a 12-bit integer, either signed twos-complement or unsigned, as determined above.
- Other inputs include clock and a reset signal, which may be synchronous or asynchronous.
- An overflow (OVR) output should indicate when the 12b accumulator has exceeded its maximum value of 4095/2047 for an unsigned/signed integer. For a signed accumulator, there should be a similar underflow (UNDR) output, indicating that the accumulation register has exceeded its maximally negative value of -2048.
- Operation is edge triggered, though the choice of positive or negative edge is left to your discretion.
- Layout is DRC and LVS clean and area-efficient (empty space between gates should be minimized.
- Pins should be on the periphery of the layout in metal 1, 2, or 3.
- Optimize your design for area, energy (J/cycle), or speed.

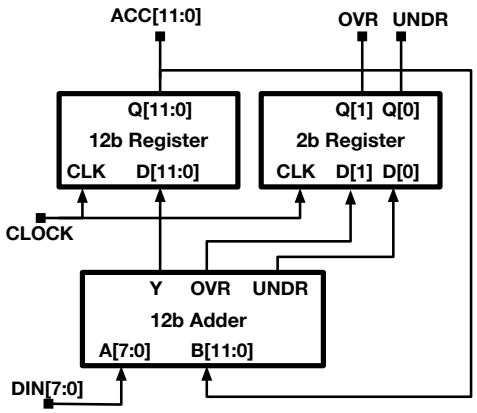

Figure 1: Example block diagram of an accumulator

Notes

Energy Measurement Run the system at a sufficiently high frequency that dynamic power dominates over static power. Measure and averge the supply current over several clock cycles, while running a reasonable representative input pattern. The measurement interval should be an integer multiple of the clock period, since the supply current is not evenly distributed over a clock cycle. The energy, in J/cycle (or equivalently J/operation), is just the power ($I_{DD}V_{DD}$) multiplied by the clock period.

Library Sharing If you are working in a group, or sharing logic gates, you will need a commonly accessible space. You can request a shared folder from Mosaic. The link to create a request is https://engrmosaic.uncc.edu/open-ticket/create-ticket.

Architecture and Operation

Figure 1 shows a block diagram of one way to construct the accumulator. The accumulator keeps a running sum of all the numbers input since it was last reset. The output is fed back into the input of the adder to compute the next sum. The sum of several 8-bit numbers may exceed the range of an 8b integer (e.g. 120+125+99=344 cannot be represented with 8 bits), so the accumulator is 12 bits. Therefor the inputs to the adder are one 8b integer and one 12b integer. The easiest way to deal with this is to construct a 12b adder and connect the upper 4b of DIN to ground, so they are always zero. Alternatively, you may be able to take advantage of this by using half adders in places where a full adder is not needed, thereby saving some power and area. The sum of the current input and the current output is the input to a 12b register (12 DFFs in parallel, with a common clock), which is updated on the rising clock edge.

If an addition exceeds the largest representable 12b integer (4095 for an unsigned number, 2047 for a signed integer), it should trigger an "Overflow" indicator, so the user knows that the accumulator output is not valid. For unsigned arithemetic, this overflow can be detected by looking for a carry-out at the MSB position of the adder. If the accumulator is designed to handle signed integers, there is also the possibility of an "underflow" in the event that two large negative numbers are added and sum to a negative number outside the representable range (e.g. -2000 + -100 sum to -2100, which cannot be represented in 12b). Overflow and underflow detection in signed arithmetic follows the same basic principle, but is slightly more complex. Note that the overflow and underflow outputs are registered, so they indicate whether the current registered accumulator output is valid or not.

Report Contents and Format

Document the design and testing of your accumulator in a report. Figures should be included in the body of the document, not printed separately and stapled to the back. Your report should thoroughly explain your design process.

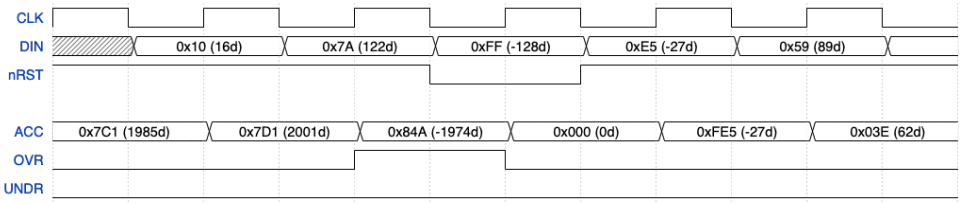

Figure 2: Operation of an 8b-input 12b accumulator with a synchronous active-low reset. Note the overflow after the second rising edge, when the output should have been 2123, but rolled over to -1974 due to the limited range of a 12b signed integer.

The items below represent key parts of the design, but do not constitute an exhaustive list of what your report should explain. The report should include the following sections:

Introduction Describe the purpose of the project, what you intended to accomplish, and inform the reader about the upcoming sections. Two to three paragraphs should be sufficient.

Design and Analysis Discuss your design choices.

- What style of adder did you use. If you considered any other topologies, mention them and explain why you did or did not ultimately choose them. If you added any features beyond baseline, such as an asynchronous reset, discuss these as well.
- Explain how you modified your circuit based on simulation and why. Discuss any particular challenges.
- A table of your gates, listing the logical operation (e.g. NAND, INV, DFF, FADD), delay, area, and person responsible for each gate.
- Discuss the worst case state and input combination in terms of delay. Why is it the worst case pattern?
- Estimate the maximum clock frequency of your accumulator from the propagation delays of your logic gates and setup/hold times of your flip flops. Assume the worst case input pattern.
- Figure 2 shows a hypothetical timing diagram of a 12-bit accumulator, illustrating a reset and an overflow.
- Clean LVS and DRC results for your top-level design.

Simulation Results Include the following simulation results.

- Plot of CLK, DIN, ACC, OVR, UNDR over several cycles showing correct functionality. The plots should show the output changing correctly as new inputs are added; output responding to a reset; and the OVR and UNDR output pins correctly indicating an overflow/underflow, respectively. Use multiple plots here; you do not need to attempt to fit all these behaviors into one plot.
- Include propagation delays (and setup/hold times as appropriate) for all the gates used in your design.
- Simulation measuring the propagation delay from the clock edge, through the register output, through the adder and back to the data input of the register. Use your worst case input pattern.
- A table listing the following parameters:
  - Maximum clock frequency of the accumulator.
  - Energy per cycle.
  - Supply leakage current $I_{DD,Leak}$. Describe the conditions under which this measurement was made.
  - Dynamic supply current specified as µA/MHz (I_{DD}/f_{CLK} measured at a sufficiently high frequency that $I_{DD} \gg I_{DD,Leak}$.
  - Layout area.
- Any other plots or information you feel would be useful in demonstrating the performance or functionality of your circuit.

Discussion If there are any odd behaviors in your simulations attempt to explain them. What might be the cause? What did you do to investigate the cause? Include any simulation plots that might aid your explanation here. What difficulties were encountered? What would you have done differently?

Conclusion Briefly summarize your results. What did you learn?

References If you used information from any papers, applications notes, or other textbooks, cite those works here. You do not need to cite class notes or the Weste and Harris textbook.

1 Grading

The criteria and weights listed in Table 1 will be used in calculating project grades.

Table 1: Grading

Criteria	Weight
Functionality	30%
Performance	20%
Design Procedure	20%
Report Clarity	30%

Resources

You may find some of the following resources helpful.

- There are several web calculators that can convert between decimal and two's complement. One is here: https://www.exploringbinary.com/twos-complement-converter/.
- Wavedrom is a useful web tool for drawing timing diagrams: https://wavedrom.com/
- Adders are discussed in section 4.2 of the Weste & Harris textbook.