ECGR 4433 Project 1: Flip-Flop Design and Characterization

Due Friday Nov. 19, 2021

In this project you will design and layout a D-type flip-flop in 45nm CMOS technology.

- Project is to be performed individually. You may discuss the concepts, but you should not share designs.
- The DFF should be designed using the Cadence 45 nm Generic PDK used for other class assignments.

Specifications

Design your DFF to meet the following specifications.

- $V_{DD} = 1.0\ V$
- Rising-edge triggered.
- Layout is DRC and LVS clean.
- Layout is suitable for abutment placing in a larger logic circuit and should have an integer number of wiring tracks.
- Pull-up and pull-down strengths should be approximately equal, defined as output rise- and fall-times being within 20% of equal to each other.

Notes

Input Capacitance To estimate input capacitance, assume transistors have $C_{OX} = 8\text{fF}/\mu m^2$. Then the input capacitance of a given input X is the sum of the areas of all transistor gates connected to that input. For example suppose you have an inverter with the following dimensions.

$$
\begin{aligned}
(W/L)_N &= 500nm/45nm = 0.5\mu m/0.045\mu m \\
(W/L)_P &= 1000nm/45nm = 1.0\mu m/0.045\mu m \\
A_N &= 0.5 \cdot 0.045 = 0.0225\mu m^2 \\
A_N &= 1.0 \cdot 0.045 = 0.045\mu m^2 \\
A_{INV} &= 0.0675\mu m^2 \\
C_{In,INV} &= 0.0675\mu m^2 \cdot 8fF/\mu m^2 = 0.54fF
\end{aligned}
$$

Note that you should not count the gates of *all* transistors in a gate, only the ones connected to the input in question.

Layout The layout should be suitable for use as a standard cell in a larger design.

- VDD and VSS should connect by abutment both horizontally, and (with flipped adjacent rows) vertically.

- The cell should use a "PRboundary" layer to indicate alignment.
- Any electrically conductive layer not connected to VDD or VSS (poly, active/oxide, contacts) should be within PRboundary with sufficient spacing that two adjacent cells will be DRC clean together.
- Other layers, when cells are abutted, should either connect or leave sufficent spacing.
- M1-M2 contacts are all on a grid.
- M2 should be minimized and should only run vertically.
- No layers above M2 should be used in the layout.
- Demonstrate that the layout is tileable by abuting instantiating several copies of the cell, abutted in the manner described in class, and showing that the combined layout passes DRC (you don't need to run LVS on this circuit).

Latch vs Flip-Flop The well-known SR latch, comprising two cross-coupled NAND or NOR gates is a latch, not a flip flop. Be sure to verify that the design you use is *edge-triggered* not *level-triggered*. The two-stage DFF design (built from two latches, each including two inverters and tw switches) discussed in class meets this requirement.

Report Contents and Format

Document the design and testing of your amplifier in a report Figures should be included in the body of the document, not printed separately and stapled to the back. Your report should thoroughly explain your design process. The items below represent key parts of the design, but do not constitute an exhaustive list of what your report should explain. The report should include the following sections:

Introduction Describe the purpose of the project, what you intended to accomplish, and inform the reader about the upcoming sections. Two to three paragraphs should be sufficient.

Design and Analysis Describe your design process.

- Discuss your design choices. If you used the topology we discussed in class, say so and explain why. If you considered any other topologies, mention them and explain why you did or did not ultimately choose them. If you added any features beyond baseline, such as an asynchronous reset, discuss these as well.
- Explain how you modified your circuit based on simulation and why. Discuss any particular challenges.
- Include the schematic of your DFF, the testbench schematic, and a table of all transistor sizes.

Simulation Results Include the following simulation results.

- Plot of CLK, D, Q showing correct functionality. The waveforms should show Q correctly changing on the rising clock edge and should show that Q does not change except on a clock edge (or a reset, if applicable). If you add a reset, it should also show the reset working correctly.
- The simulation results you use to measure setup time, hold time, and CLK-Q delay. Use the method described in section 10.4.2 (*Characterizing Sequencing Element Delays*) of the Weste and Harris book (4th edition) to measure the setup and hold times.
- A table listing the following parameters:
  - Clock-to-Q delay for both a rising and falling output: $t_{C-Q,lh}$, $t_{C-Q,hl}$.
  - Setup time t_{setup}.
  - Hold time t_{hold}.
  - Output rise time and fall time t_r, t_f.
  - Supply leakage current $I_{DD,Leak}$ under four different conditions (CLK=0,1 and Q=0,1).
  - Dynamic supply current specified as µA/MHz (I_{DD}/f_{CLK} measured at a sufficiently high frequency that $I_{DD} \gg I_{DD,Leak}$.
  - Input capacitance at CK and D pins, determined from the supply current of a driving inverter, as described above in the notes section.

  - Layout area, including only the area enclosed by "PRbound."
- Any other plots or information you feel would be useful in demonstrating the performance or functionality of your circuit.

Discussion If there are any odd behaviors in your simulations attempt to explain them. What might be the cause? What did you do to investigate the cause? Include any simulation plots that might aid your explanation here. What difficulties were encountered? What would you have done differently?

Conclusion Briefly summarize your results. What did you learn?

References If you used information from any papers, applications notes, or other textbooks, cite those works here. You do not need to cite class notes or the Weste and Harris textbook.

1 Grading

Table 1: Grading

Criteria	Weight
Meeting Specifications	30%
Design Procedure	40%
Report Clarity	30%