Project 1: Flip Flop Design and Characterization

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Introduction

The purpose of the project is to design and layout a D-type flip flop. The project had five requirements that needed to meet, VDD must be 1 volt, rising edge triggered, Layout is DRC and LVS, and Pull up/down strengths should be withing 20% of each other. Besides those requirements, students were free to design the D-type flip flop as they please.

The report will also cover four brief sections of the process of the project. The first section discusses the design of the schematic and testbench. The second section covers the overall results from the project. The next section discusses the issued dealt with in the project, initial design issues with the schematic and layout. The final section discusses what was learned from the project and highlights results of the project.

Design and Analysis

The design is a two stage D-type flip flop. This was created by using two SR latches which is seen in figure one. Once the schematic was created, it was then used in the testbench schematic along with an inverter shown in figure two. The main reason for choosing this design was because of the simplicity. The latch was already made from a previous assignment, so just by connecting two of them we would get our D-type flip flop. The inverter was added to the test bench to give improved accuracy of the waveforms shown in figure three.

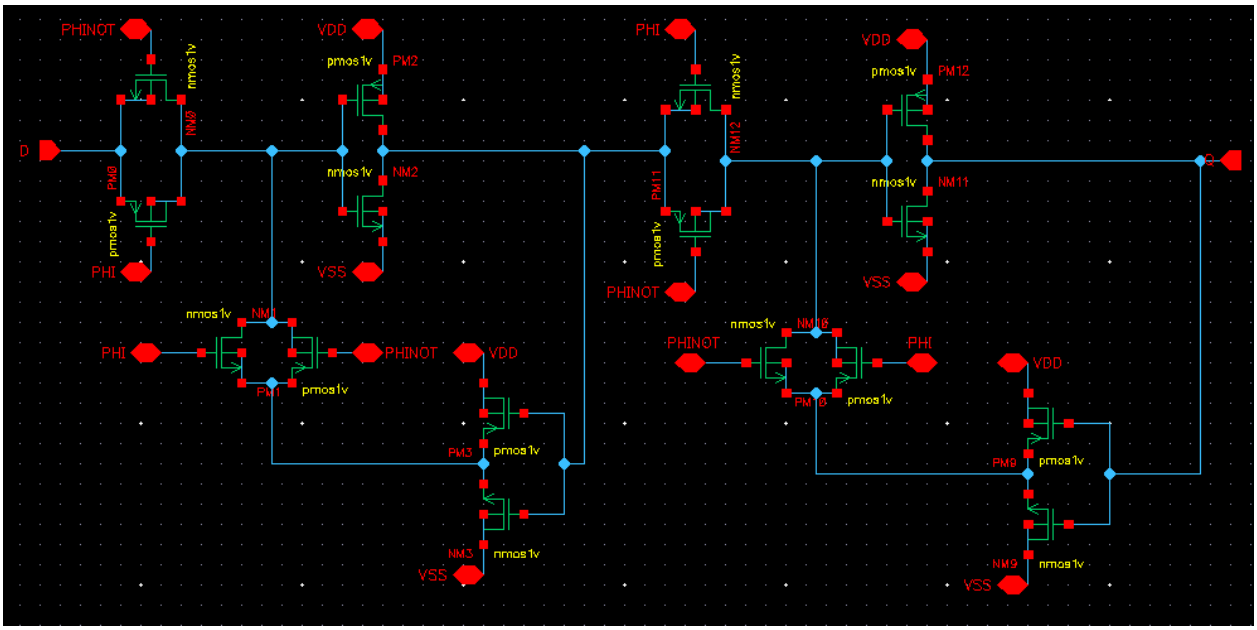

Figure 1: Schematic of the D- type Flip Flop

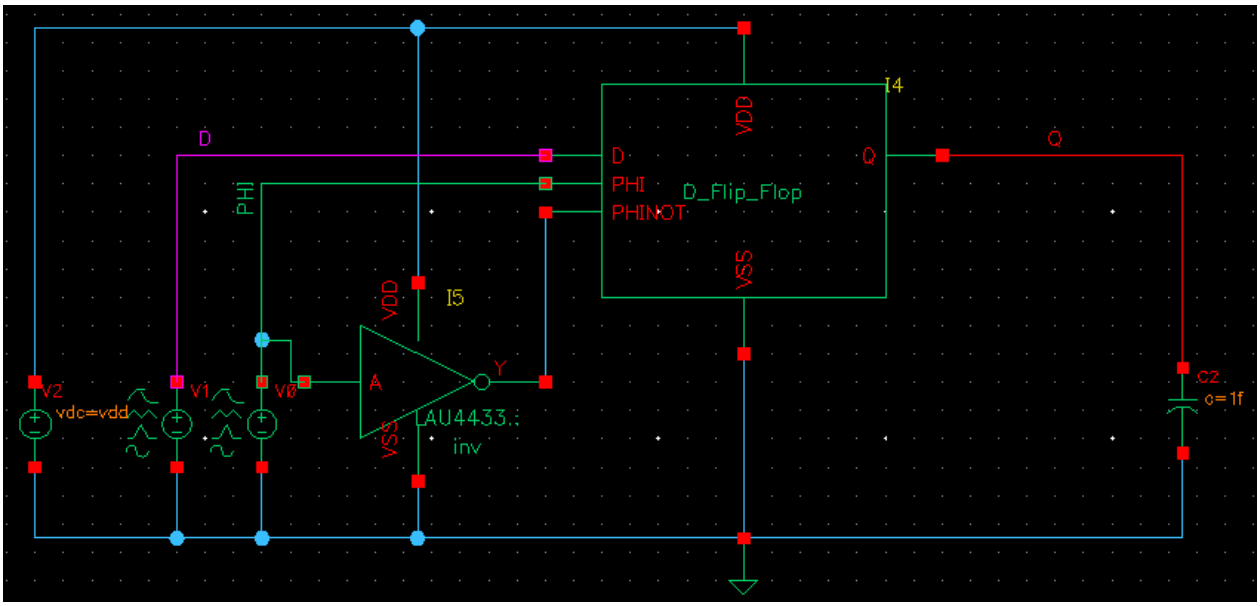

Figure 2: Test bench

Simulation Results

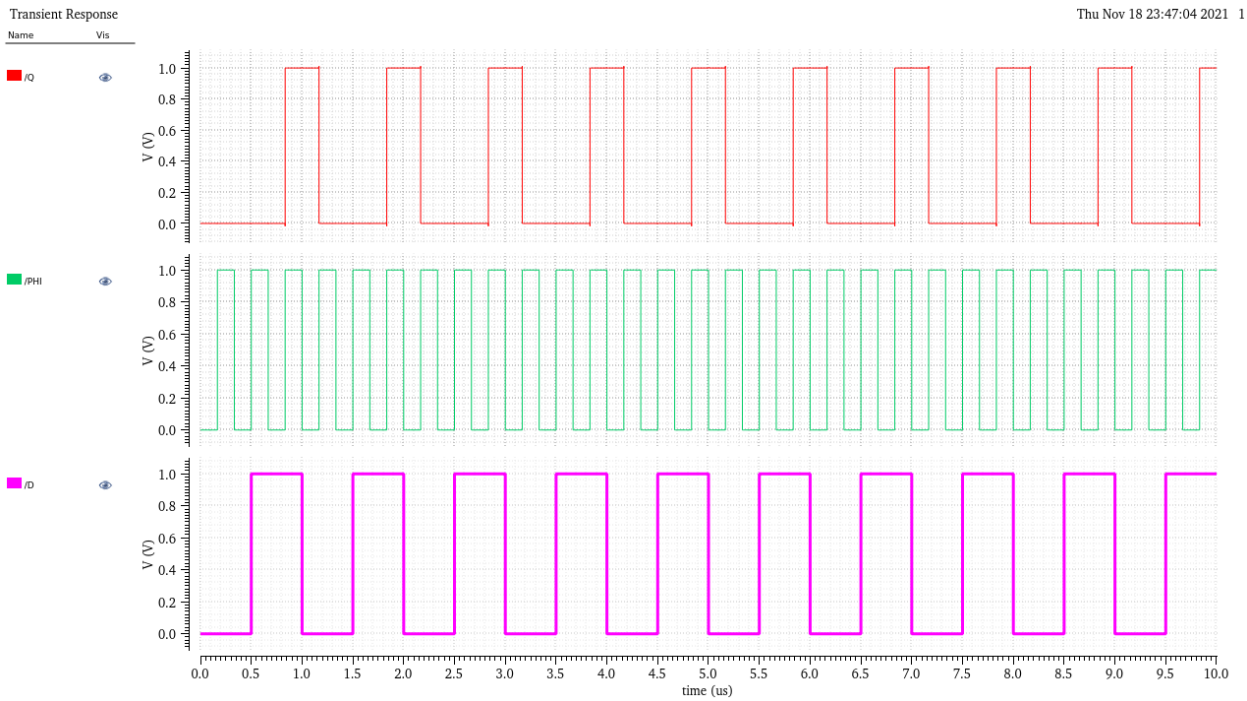

Figure 3: Plot of PHI, D, AND Q.

Clock to Q-delay - Rising	**0.5u**
Clock to Q-delay - Falling	**0.5u**
Setup Time	**0.5u**
Hold Time	**-18p**
Output Rise Time	**74.4025**
Supply Leakage Current: 00	**3.44 pA**
Supply Leakage Current: 01	**-5.01995 ua**
Supply Leakage Current: 10	**11.6956 uA**
Supply Leakage Current: 11	**28.4112 uA**
Dynamic Supply Current	**49.6163 nA**
Input Capacitance	**0.612 fF**

Table 1: Simulation Output

Layout

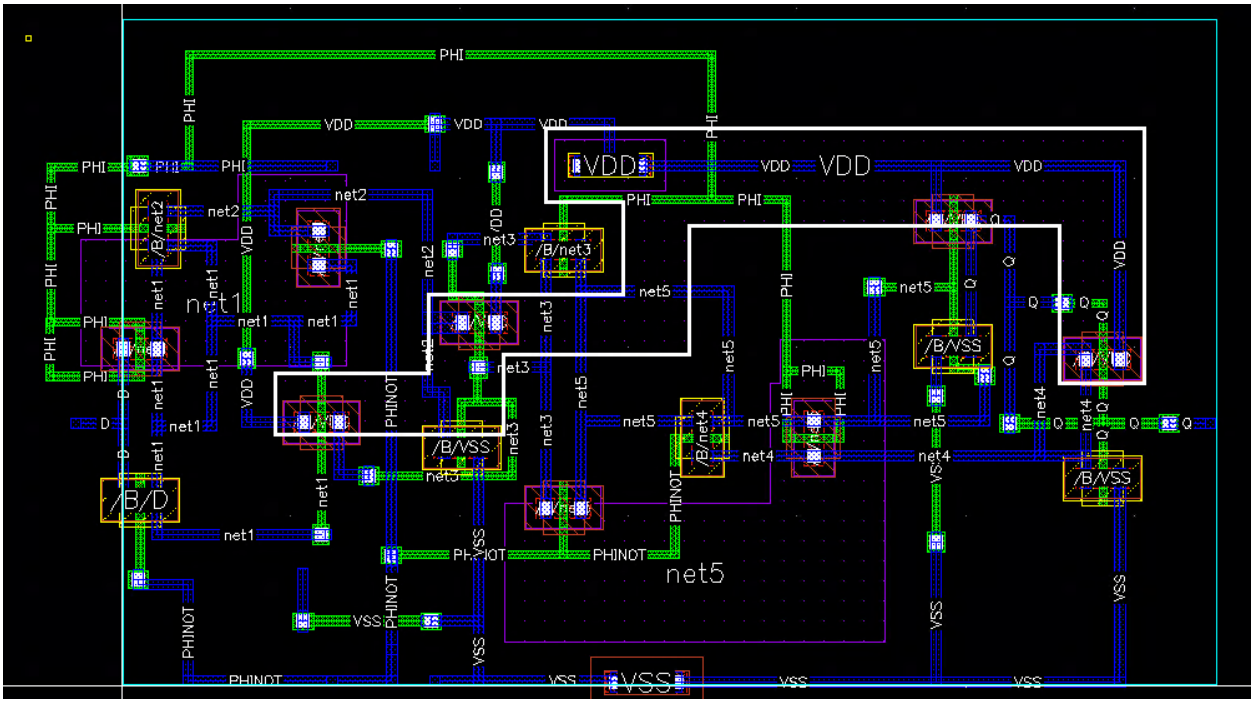

Figure 4: Layout of the D-type Flip Flop

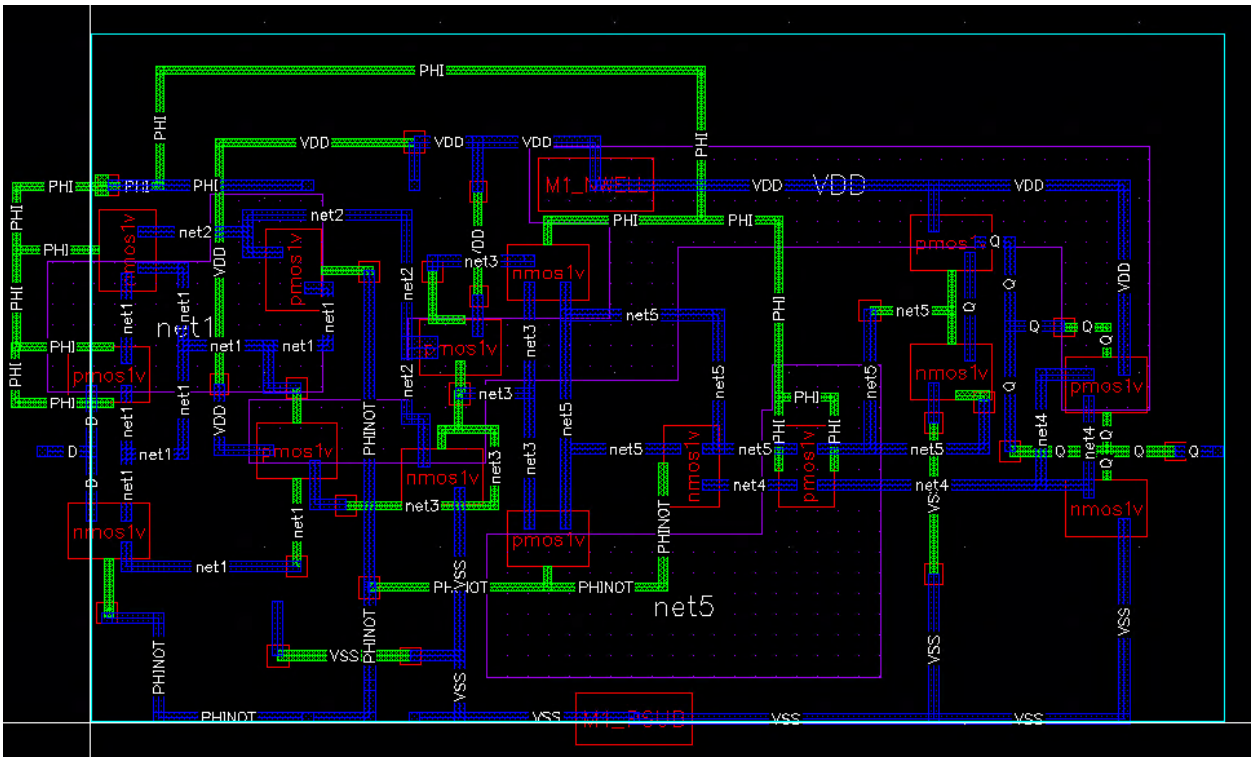

Figure 5: Layout of the D-type Flip Flop (simple view)

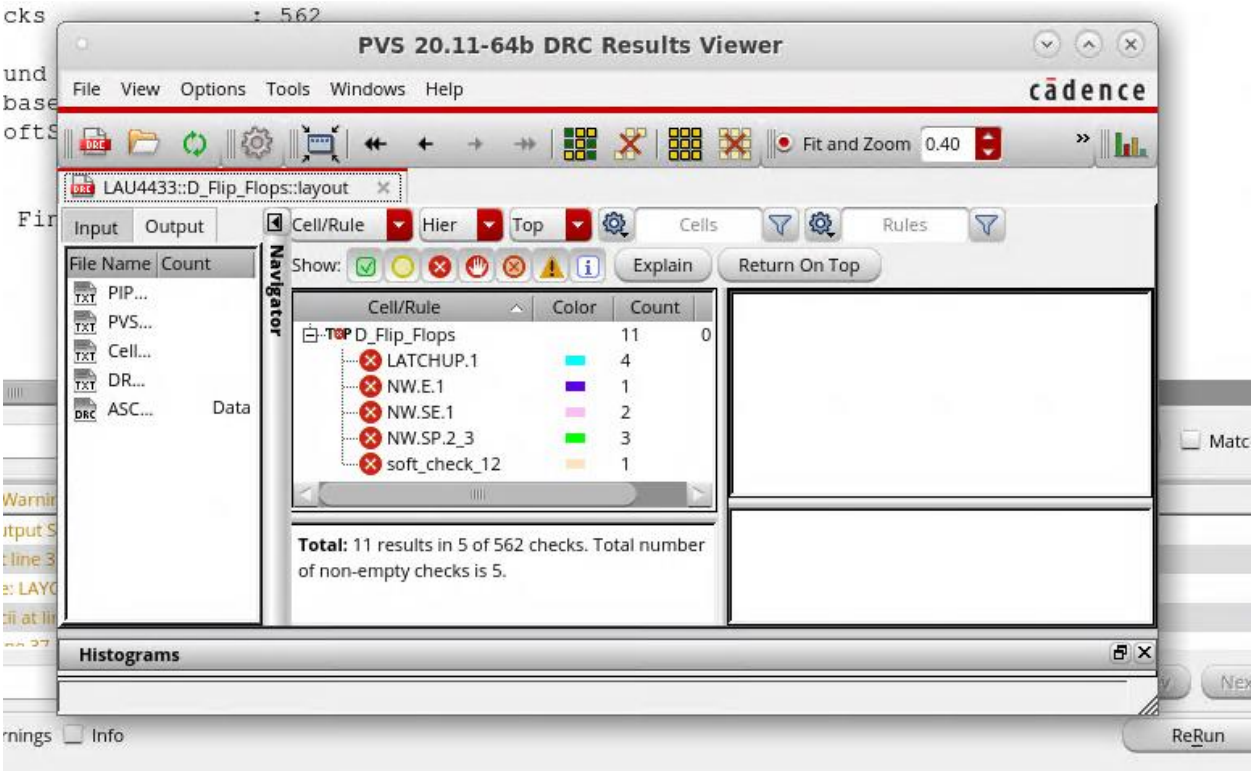

Figure 6: DRC Check

Discussion and Troubleshooting

I would have changed my overall design in figure 1, had I considered how difficult the layout would be to create later. I had to recreate my layout multiple times due to issues such as, files locked out by mosaic anywhere, wiring crossing, and spacing issues. I definitely would have tried reducing, PHI, PHINOT, VDD, and VSS to just a single pin each. The schematic issue would have been very messy, however I felt that it would have just made creating the layout much easier. The schematic shown in figure 1 is my third design of the flip-flop since I had issues producing a functioning waveform.

Conclusions

Due to complicated issues with multiple attempts to create a proper layout, not all of the specification are included in the report. The results that are given shows that the schematic and testbench produced an accurate plot of the PHI, D, and Q. The layout had 11 errors shown in figure 6. This was cause by a strange issue where the N-well net 5 would not register and cause 4 additional latch-up. N-well net 1 also has a similar issue to net 5, however this would strange be solved by including half of a n-mos shown in figure five. The rest of the spacing issues were caused by the n-mos needing to be included in net 1. I felt had I not have so many issues with losing files or restarting layouts multiple times, I may have had more time to fix the issue. I learned that proper spacing and pin placements can make all the difference in designing a schematic and layout.

References

None