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ECGR 4146: Introduction to VHDL
Lab 2: Full Adder

1. Take a screenshot of Vivado screen after you have run synthesis, and the simulation (Include the snapshot of the simulation waveform).

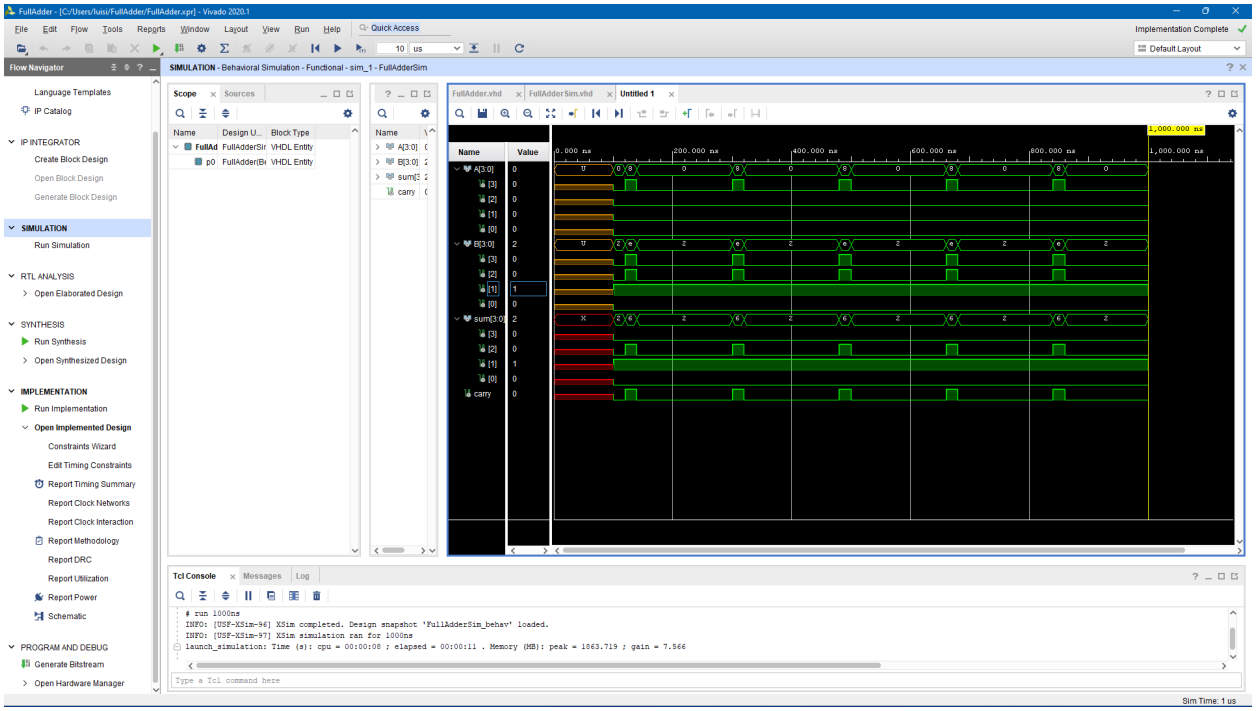

Figure 1: Simulation waveform of the full adder.

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4. Run synthesis, post place, and route and Generate Bitstream successfully. (Note: I wasn't sure if you wanted the screenshot that showed this message in figure 2, or the reports shown in figure 3.

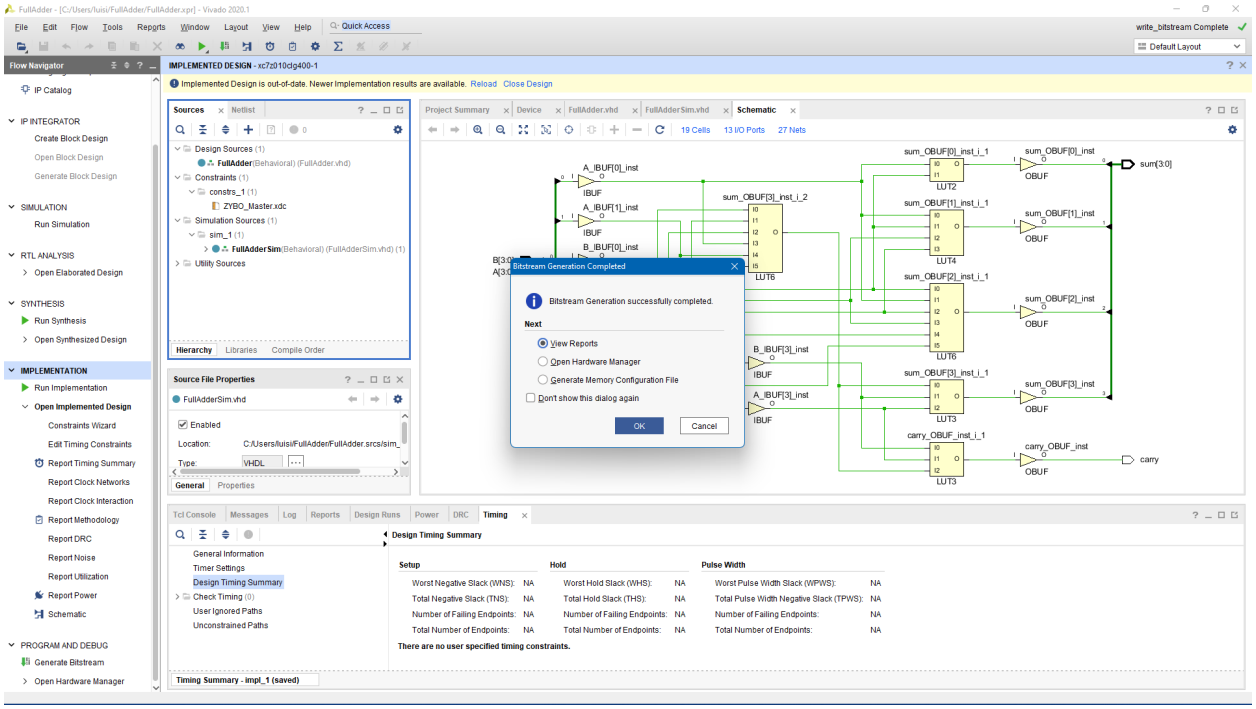

Figure 2: Message displayed after bitstream was generated.

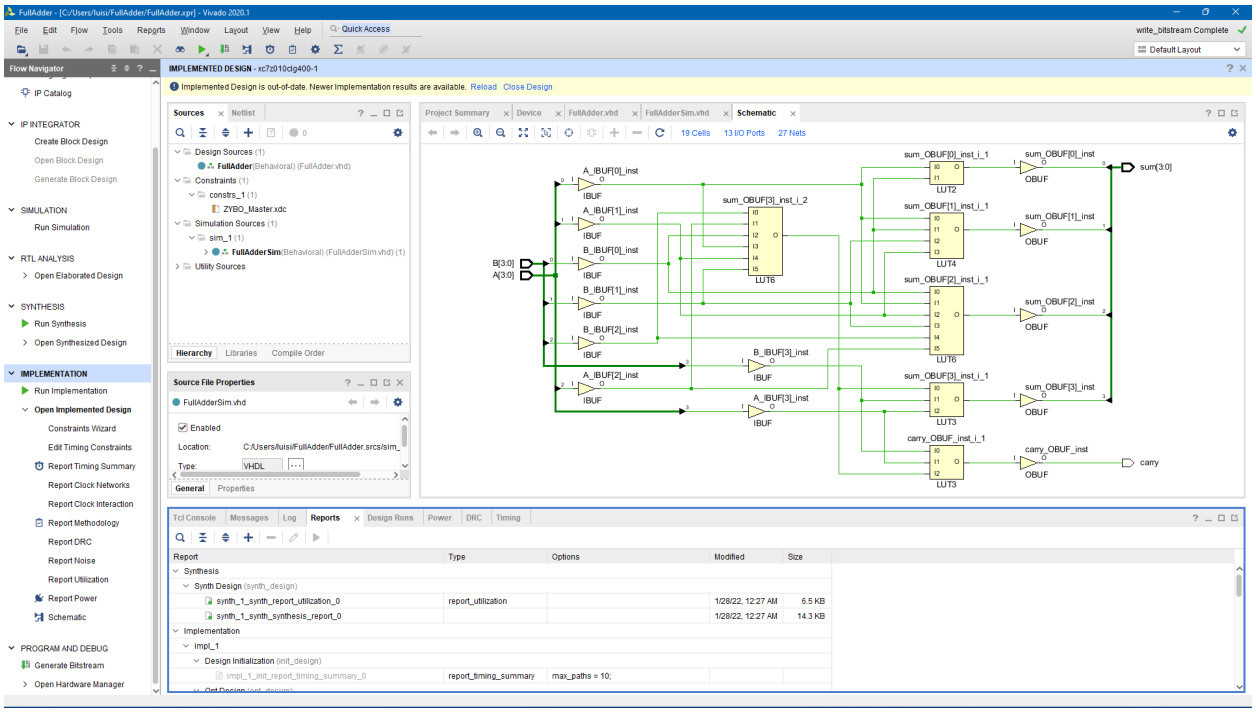

Figure 3: Reports shown after the message was closed.

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