Spring 2022-ECGR-5146/4146-Introduction to VHDL
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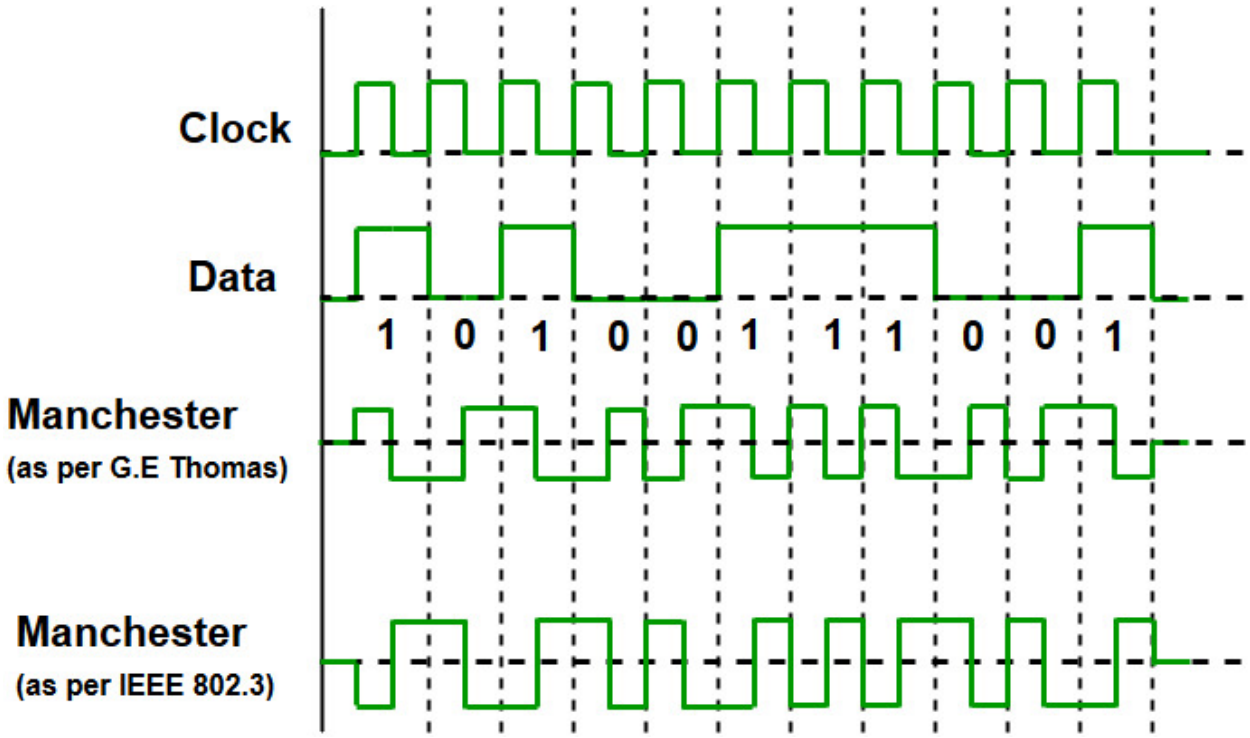
LAB 7

Manchester Encoding

Manchester encoding is a data-modulation technique that can be used in binary data transfer based on analog, RF, optical, high-speed-digital, or long-distance-digital signals. In Manchester encoding each data bit is either low then high, or high then low, for equal time.

It represents a bit in a data stream. There are two conventions for the representation of data:

- As per G. E. Thomas, it specifies that for a 0 bit the signal levels will be low - with a low level in the first half of the clock period, and a high level in the second half. For a 1 bit the signal levels will be high-low.
- As per IEEE 802.3 standards a logic 0 is represented by a high-low signal sequence and a logic 1 is represented by a low-high signal sequence.



The entity of the design is defined as:

```
entity ManchesterEncoder is
port(
        str_input: in std_logic_vector (7 downto 0);
        clk: in std_logic;
        reset: in std_logic;
        str_output: out std_logic
);
end ManchesterEncoder;
```

In this design the input is 8-bit wide consisting of 8 states from s0 to s7.
Two clock cycles are required for each bit as the encoded bit includes a sequence of "01" or "10". When reset = 0 and enable =1 the output goes to s0 state from idle state for the first bit in the input. Considering a glitch free output make use of the look-ahead output buffer to implement the Manchester encoder.

The look-ahead output buffer for a 1-bit input consists of:

```
process (clk , reset )
begin
    if ( reset = ' l ' ) then
        state_reg <= idle ;
        str_output <= '0';
    elsif ( clk ' event and c1k = ' l ' ) then
        state_reg <= state_next ;
        str_output <= str_output_next ;
    end if ;
    end process;
```

--next state logic---

```
Process(state_reg)
Begin
      Case state_reg is
      When idle =>
        state_ next <= idle;
         else
        state_ next <= s0;
```

By referring the above 1-bit implementation pseudocode design an 8-bit Manchester encoder.

Objectives:

Your objective for this lab exercise is to:

- Develop State diagram for an 8-bit Manchester encoder.
- Implement an 8-bit Manchester encoder with output buffer and lookahead logic.

Deliverables:

PDF that includes:

- FSM
- ASM
- VHDL Codes
- Testbench
- Waveform