Diario: Explica el proceso de diseño de Sistemas en Chip utilizando FPGAs. ¿Cómo es el flujo de trabajo con las herramientas de diseño? ¿Cómo crees que el uso de estas herramientas facilita la creación de diseños complejos (mejora lo que se conoce como "design productivity"?

Thanks Felipe:

Well during this course we developed an intuition of the proper workflow one team of engineers must follow in order to improve the design productivity.

One of the key concepts we learned is that Verilog and VHDL are not the center of the design workflow but rather useful tools to automate circuit implementation.

Before even thinking in Verilog code, one must engage in the design process and test different circuit proposals.

Then, we can translate this implementation into Verilog code and compare Verilog's implementation with ours.

The testbenches are often useful for error detection and debugging because they enable us to see the behavior of the circuit´s signals across different timescales and spot desynchronized signals, bad connections, or strange behaviors in edge cases.

Finally, after we know the project works, we can download the project and test it real hardware components such as an fpga.

Now, my friend Arturo will explain all the challenges we had to overcome in throughout the different assignments and the gumnut core´s implementation.