SOMADOR

Projete um circuito capaz de somar dois números de 1 bit

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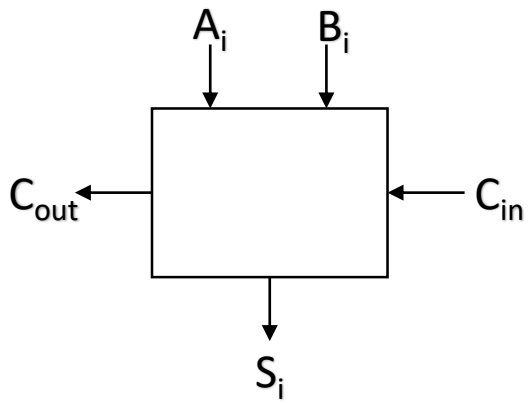

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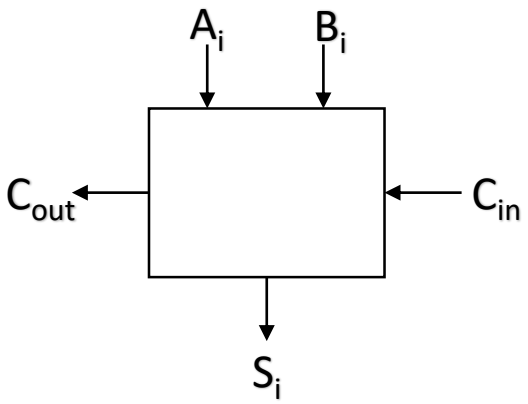

A_i	B_i	C_{in}	C_{OUT}	S_I
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

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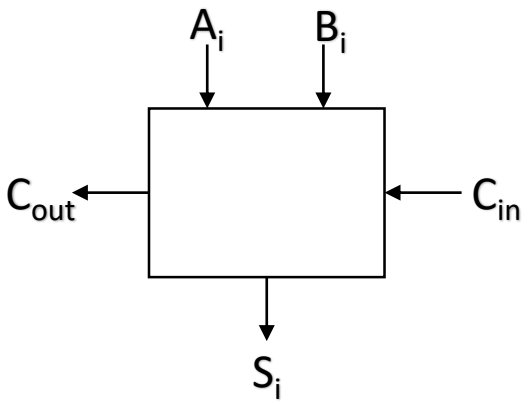
Projete um circuito capaz de somar dois números de 1 bit



A_i	B_i	C_{IN}	C_{OUT}	S_I
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Faça um mapa de Karnaugh para saída S_I e outro para C_{OUT} e encontre as funções minimizadas

A_i	B_i	C_{IN}	C_{OUT}	S_I
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

C_{out}

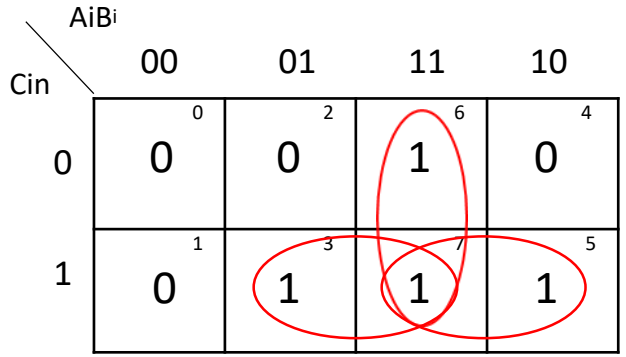
Cin \ AiBi	00	01	11	10
0	0 (0)	0 (2)	1 (6)	0 (4)
1	0 (1)	1 (3)	1 (7)	1 (5)

S_i

Cin \ AiBi	00	01	11	10
0	0 (0)	1 (2)	0 (6)	1 (4)
1	1 (1)	0 (3)	1 (7)	0 (5)

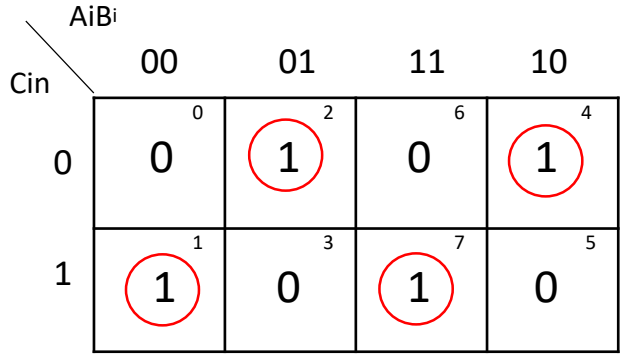
A_i	B_i	C_{IN}	C_{OUT}	S_I
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

C_{out}



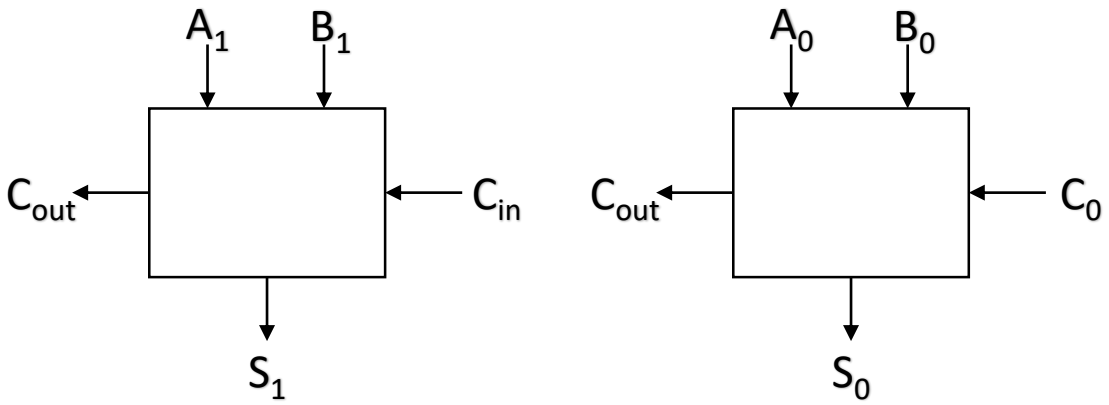
$$C_{out} = B_i.C_i + A_i.C_i + A_i.B_i$$

S_i

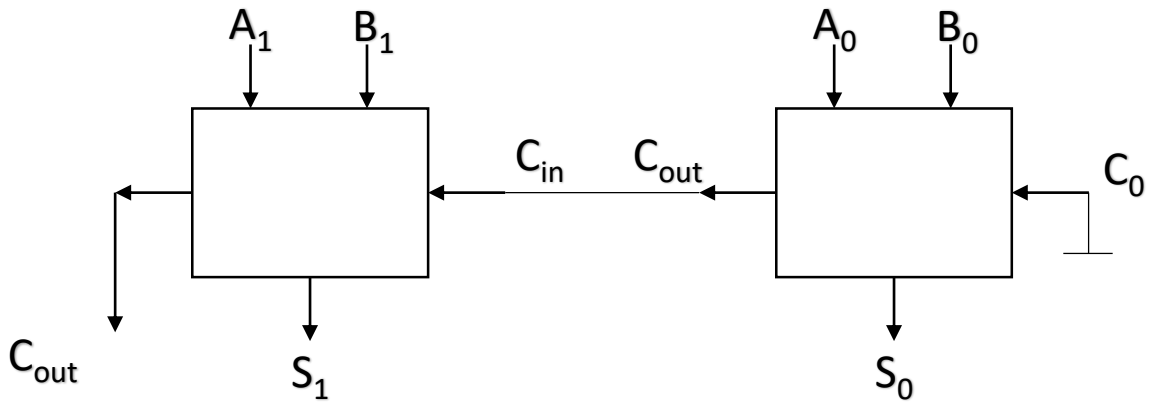


$$S_i = \bar{A}_i.B_i.\bar{C}_i + A_i.\bar{B}_i.\bar{C}_i + \bar{A}_i.\bar{B}_i.C_i + A_i.B_i.\bar{C}_i$$

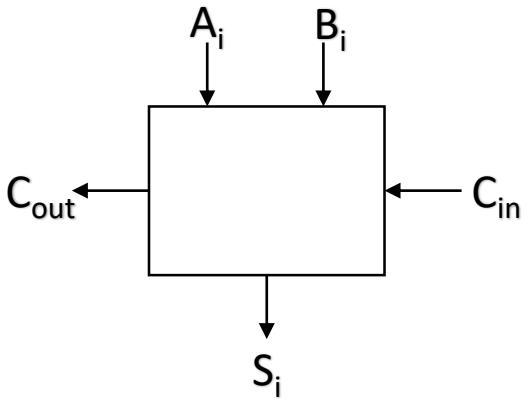
Somador Série de 2 Números de 2 bits



Somador Série de 2 Números de 2 bits



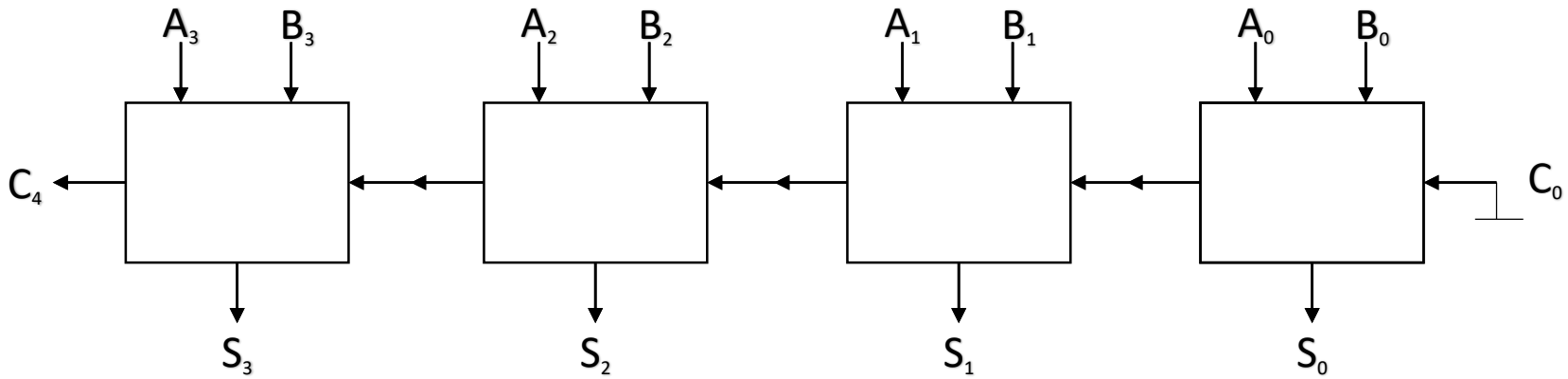
SOMADOR DE 1 BIT



A_i	B_i	C_{in}	C_{OUT}	S_I
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

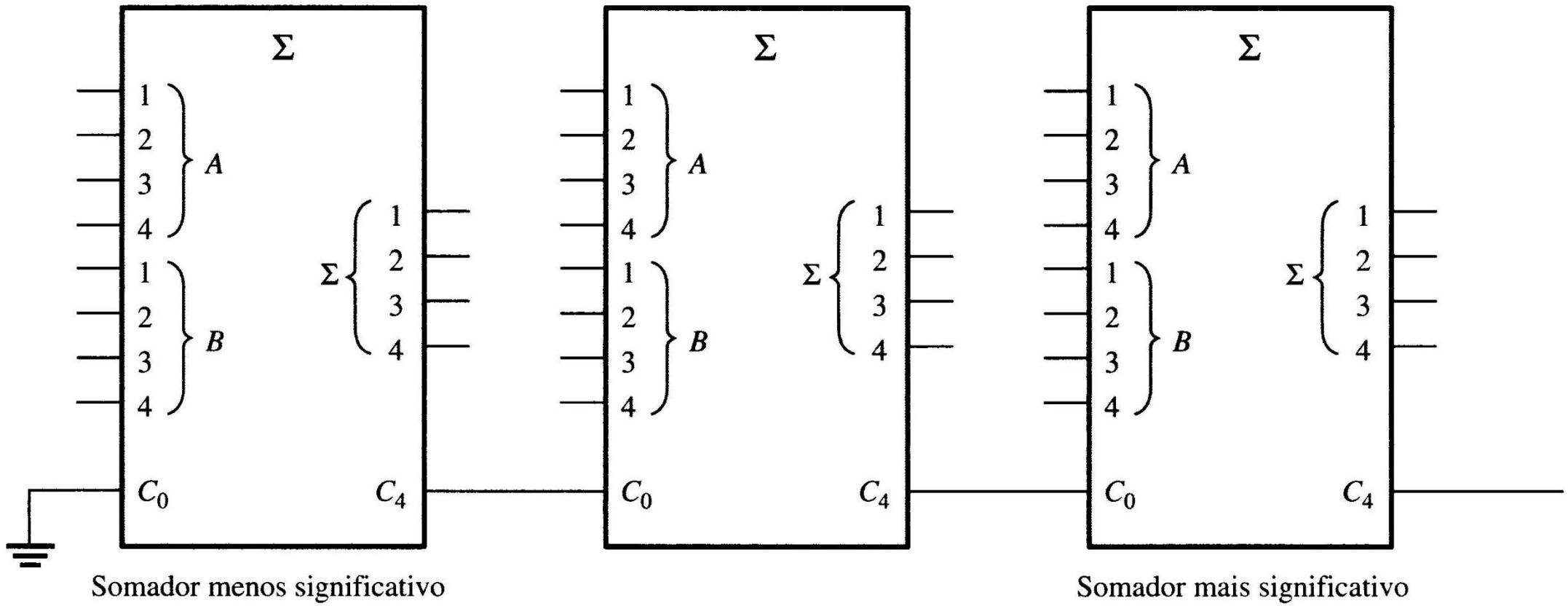
SOMADOR DE 4 BITS

Para implementar um somador de 4 bits, isto é, somar dois números de 4 bits cada, podemos “cascatear” 4 blocos que projetamos conectando o Cout do menos significativo no Cin do mais significativo, como esquematizado abaixo:



Nós vamos utilizar somadores implementados em circuitos integrados de 4 bits (74LS283)

CASCATEAMENTO DE SOMADORES



Comparador de Magnitude de 4 Bits (7485)

Este dispositivo compara a magnitude de dois números binários de 4 bits. Possui entrada que permite cascatear os circuitos possibilitando comparar a magnitude de números de 8, 12, 16 bits...

CASCATEAMENTO DE COMPARADORES