CSCI 221: Logic design

Traffic light system "4 -Ways"

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Tinker cad simulation .....Fifth

DESCRIPTION

❾ *4- way traffic signal using Basic Logic Gates & T flip flop*

Traffic lights (or traffic signals) are lights used to control the movement of traffic. They are placed at road intersections and crossings. The different colors of lights tell drivers what to do.

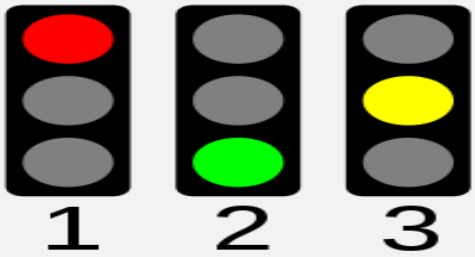
Red light on: This tells drivers to stop.

Green light on: This means the driver can start driving or keep driving.

Yellow light on: This tells drivers to stop when it is safe to as the light is about to turn red.

We used some logic gates to design our 4-ways traffic light as required "or, And, Not. On the other hand, we could used flip-flops to shorten &analyze the design.

Also, we can use clock to simplify the traffics



TRUTH TABLE

Counter state				1st signal			2nd signal			3rd signal			4th signal		
A	B	C	D	R1	Y1	G1	R2	Y2	G2	R3	Y3	G3	R4	Y4	G4
0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	0
0	0	0	1	0	0	1	1	0	0	1	0	0	1	0	0
0	0	1	0	0	0	1	1	0	0	1	0	0	1	0	0
0	0	1	1	0	0	1	1	0	0	1	0	0	1	0	0
0	1	0	0	0	1	0	0	1	0	1	0	0	1	0	0
0	1	0	1	1	0	0	0	0	1	1	0	0	1	0	0
0	1	1	0	1	0	0	0	0	1	1	0	0	1	0	0
0	1	1	1	1	0	0	0	0	1	1	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0	0	1	0	1	0	0

1	0	0	1	1	0	0	1	0	0	0	0	1	1	0	0
1	0	1	0	1	0	0	1	0	0	0	0	1	1	0	0
1	0	1	1	1	0	0	1	0	0	0	0	1	1	0	0
1	1	0	0	1	0	0	1	0	0	0	1	0	0	1	0
1	1	0	1	1	0	0	1	0	0	1	0	0	0	0	1
1	1	1	0	1	0	0	1	0	0	1	0	0	0	0	1
1	1	1	1	1	0	0	1	0	0	1	0	0	0	0	1

K-MAPS AND EQUATIONS

k-map(R1)

00	01	11	10
	1	***1***	***1***
1	***1***	***1***	***1***
1	***1***	***1***	***1***

A+BC+BD

R1= A+B(C+D)

k-map(Y1)

00	**01**	**11**	**10**
1			
1			

A'B'C'D', A'BC'D' : (M0, M4)

Y1= A'C'D'

k-map(G1)

	1	1	1

A'B'CD, A'B'C' : (M1,2,3)
A'B'D+A'B'C
G1= A'B'(C+D)

---

k-map(R2)

1	1	1	1
1	1	1	1
	1	1	1

ABC'D, ABCD, AB'CD', AB'CD: (M0,1,2,3, 9 TO 15)

R2= XNOR (A, B) +A(C+D)

k-map(Y2)

1			
1			

Y2= A'BC'D'+AB'C'D' : (M3,8)

k-map(G2)

	1	1	1

A'BC+A'BD: *(M5,6,7)*

G2= A'B(C+D)

---

k-map(R3)

1	1	1	1
1	1	1	1
	1	1	1

(M0 to M7 , M13,M14,M15)

A'+BC+BD

R3= A'+B(C+D)

k-map(Y3)

1			
1			

AB'C'D', ABC'D' : (M8,M12)

Y3= AC'D'

k-map(G3)

	1	1	1

(M9, M10, M11)
AB'C+AB'D
G3= AB'(C+D)

---

k-map(R4)

	1	1	1
1	1	1	1
1	1	1	1

(M1 to M11)

- *AB'+A'B+A'C+A'D*
- *R4= XOR (A, B)+A'(C+D)*

k-map(Y4)

1			
1			

- *(M0,M12)*
- *A'B'C'D'+ABC'D'*
- *Y4= C'D'. XNOR(A,B)*

k-map(G4)

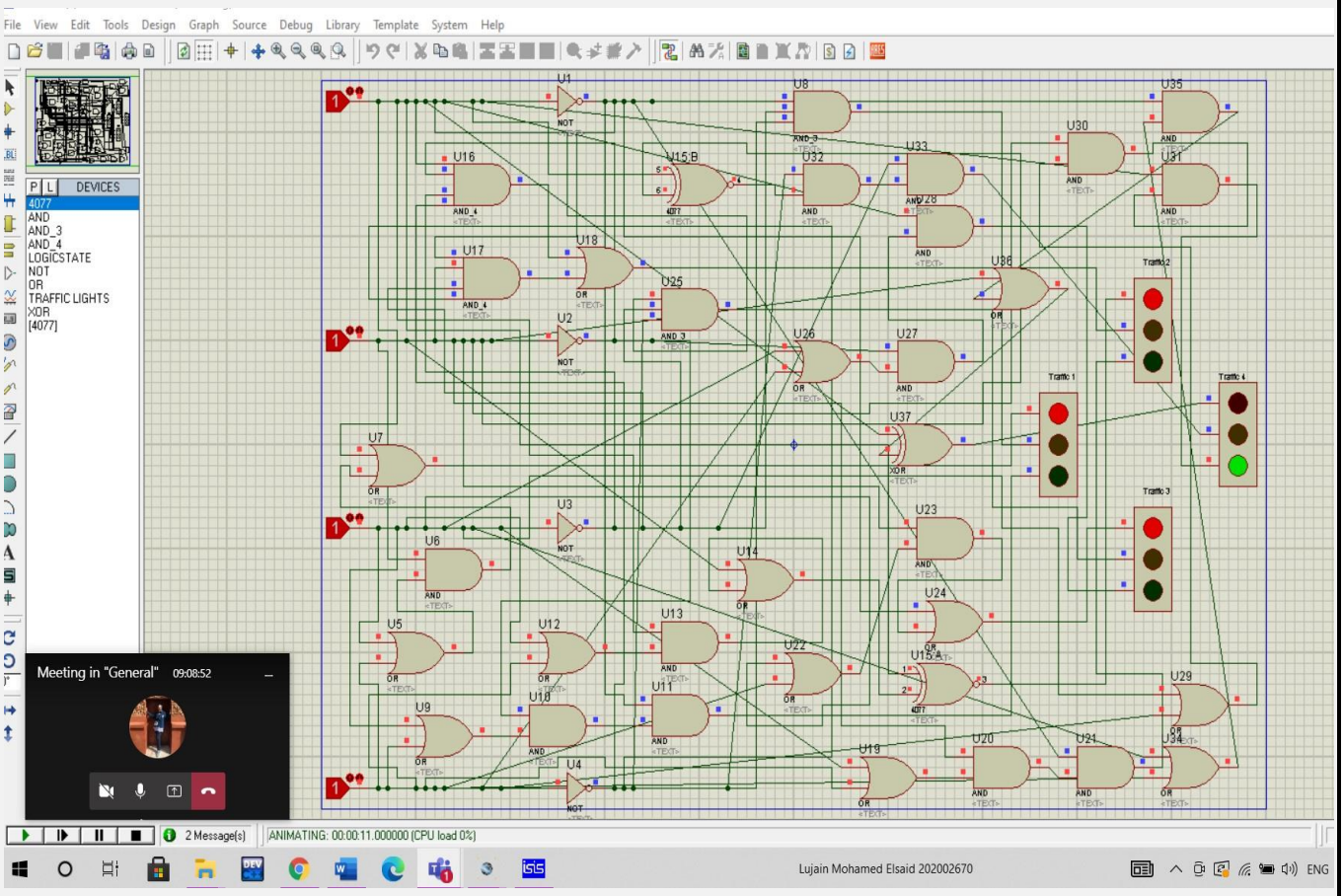
	1	1	1

(M13,M14,M15)

ABC+ABD

G4= AB(C+D)

PROTEUS SIMULATION



GATE WE USE IN PROTUES

IC-4077
AND_3
AND_4
Logic state

AND
NOT
OR
Traffic lights
XOR

TINKER CAD SIMULATION