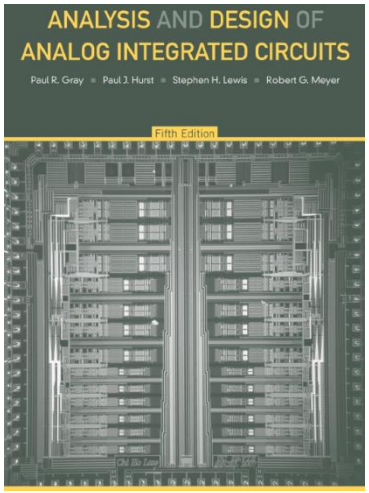
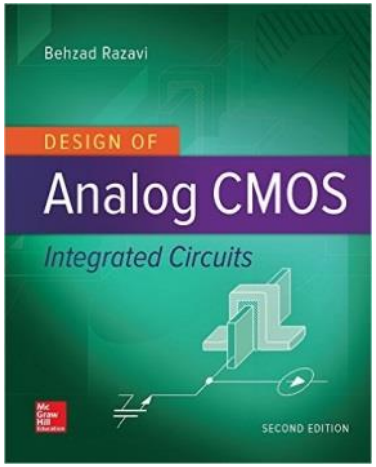
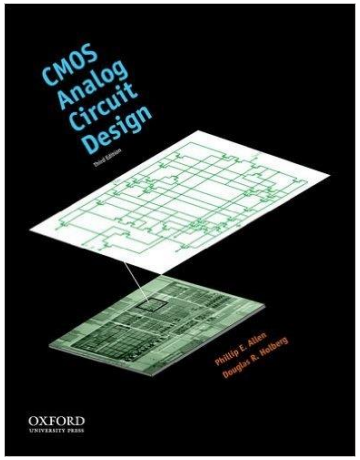
Differential amplifiers



Paul Gray, et. Al..
Analysis and Design of Analog Integrated Circuits



Behzad Razavi:
Design of Analog Integrated Circuit, McGraw-Hill, 2016



Phillip E. Allen, Douglas R. Holberg
CMOS Analog Circuit Design (The Oxford Series in Electrical and Computer Engineering) 3rd Edition

Single–ended and differential operation

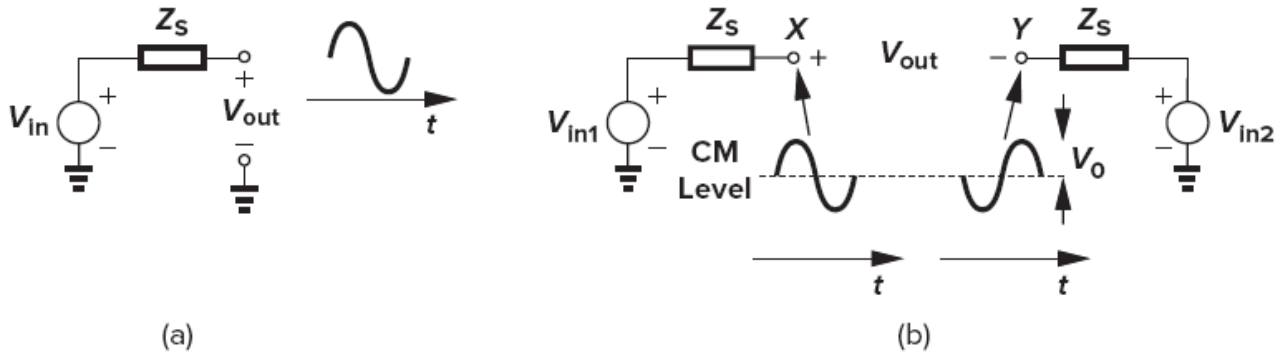


Figure 4.1 (a) Single-ended and (b) differential signals.

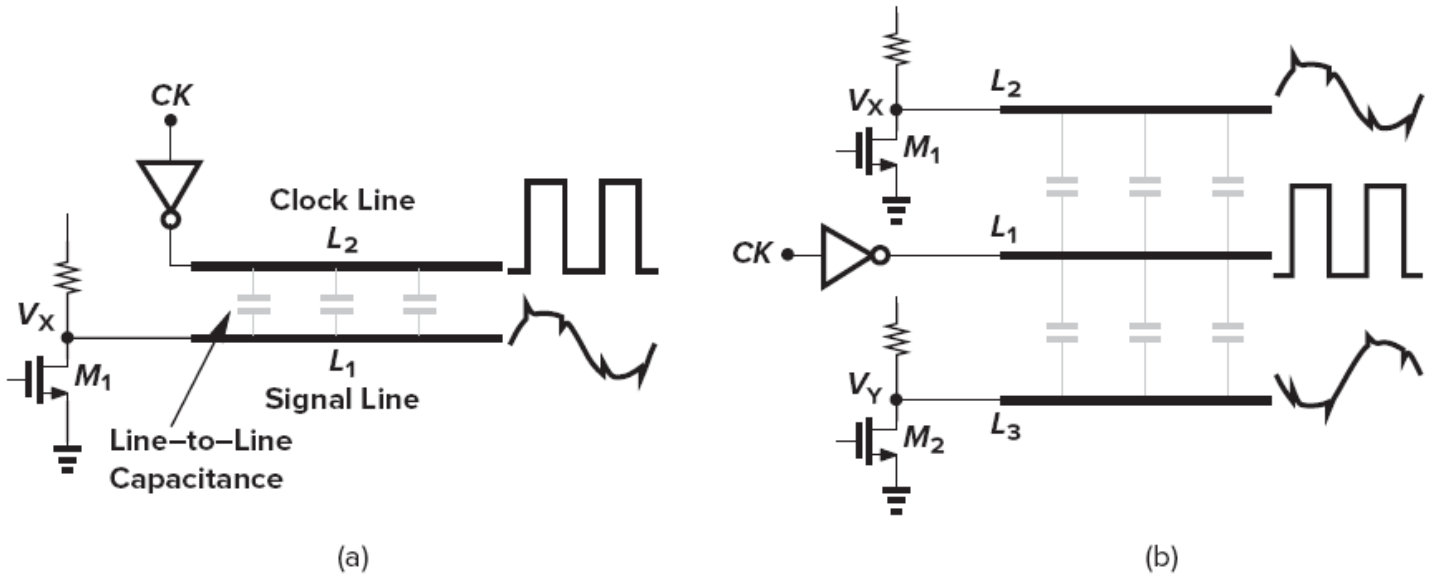


Figure 4.2 (a) Corruption of a signal due to coupling; (b) reduction of coupling by differential operation.

Single–ended and differential operation

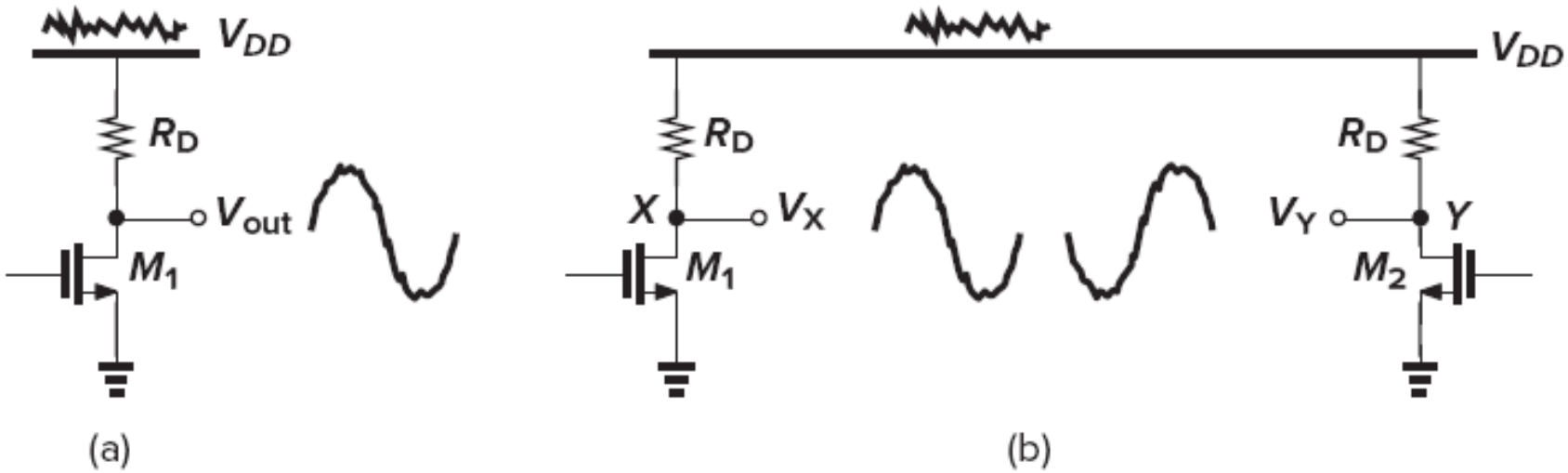
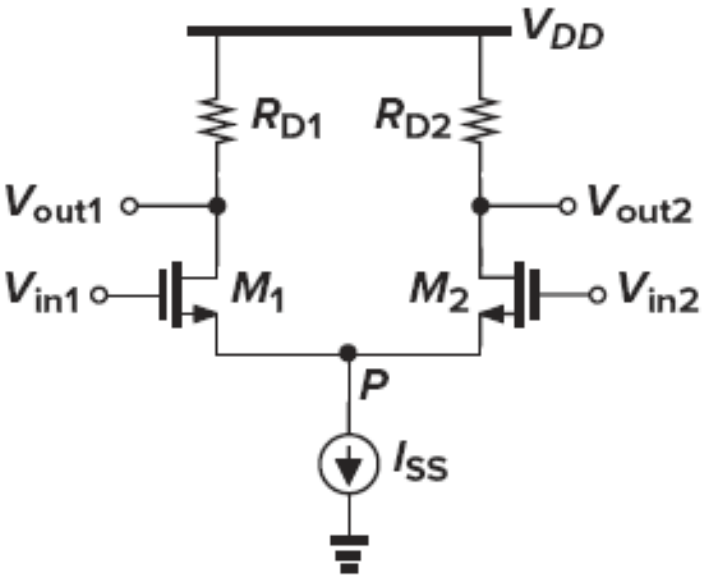


Figure 4.3 Effect of supply noise on (a) a single-ended circuit and (b) a differential circuit.

Differential amplifiers – how it operates



M_1, M_2 are the same
R_{D1}, R_{D2} are the same

Qualitative Analysis

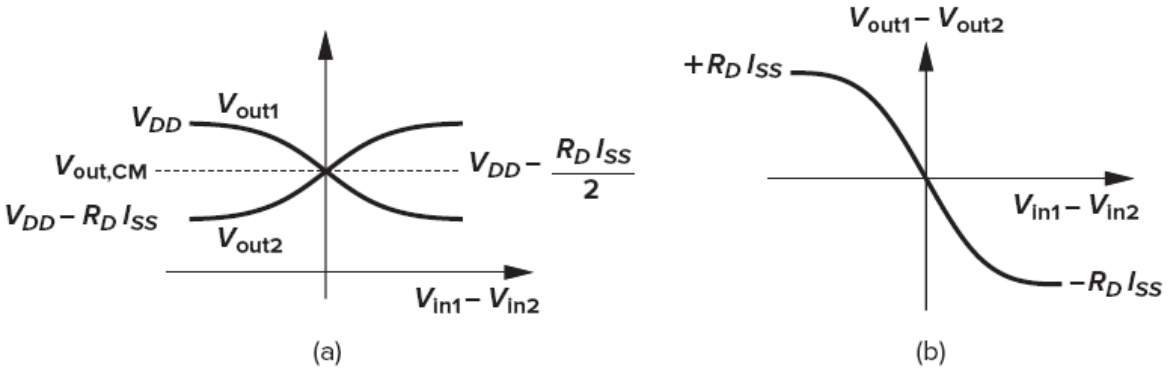


Figure 4.8 Differential input-output characteristics of a differential pair.

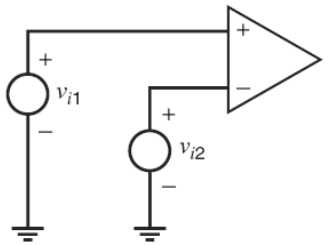
Differential amplifiers – small voltage gain

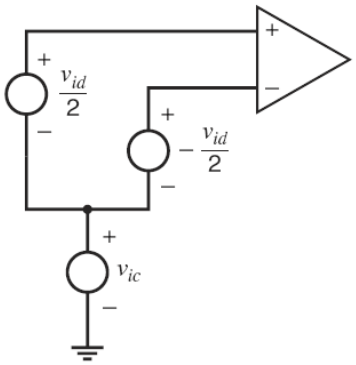
The differential input,

$$v_{id} = v_{i1} - v_{i2}$$

The common-mode or average input,

$$v_{ic} = \frac{v_{i1} + v_{i2}}{2}$$





$$v_{i1} = v_{ic} + \frac{v_{id}}{2}$$

$$v_{i2} = v_{ic} - \frac{v_{id}}{2}$$

New output variables are defined in the same way. The differential output is

$$v_{od} = v_{o1} - v_{o2}$$

The common-mode or average output is

$$v_{oc} = \frac{v_{o1} + v_{o2}}{2}$$

$$v_{o1} = v_{oc} + \frac{v_{od}}{2}$$

$$v_{o2} = v_{oc} - \frac{v_{od}}{2}$$

Differential gain - balanced amplifier

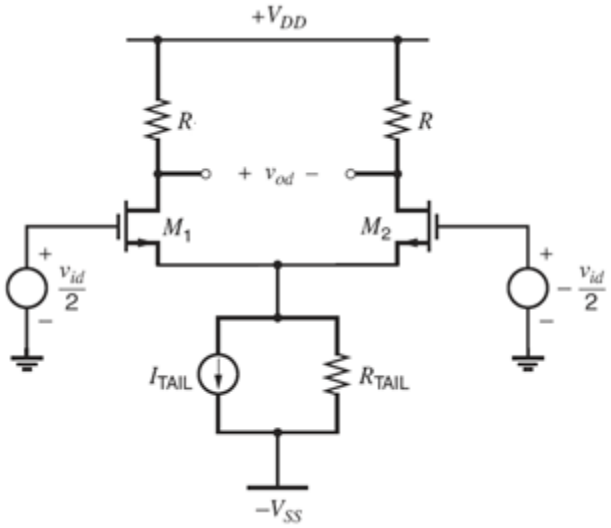


Fig. 3.54

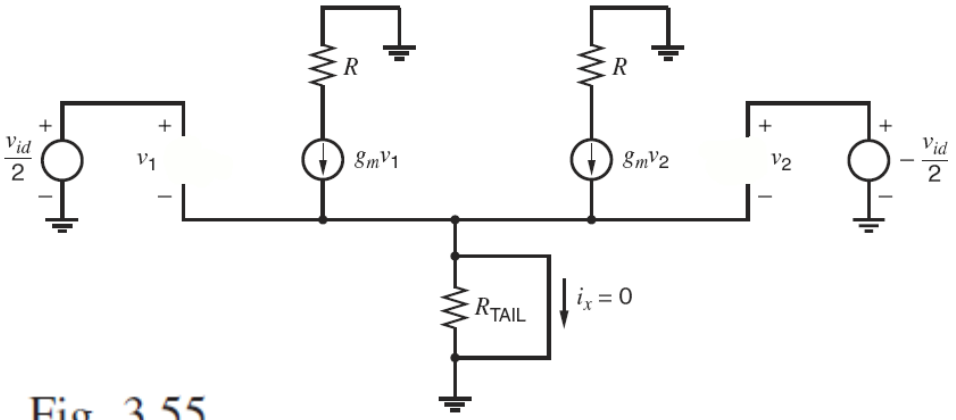
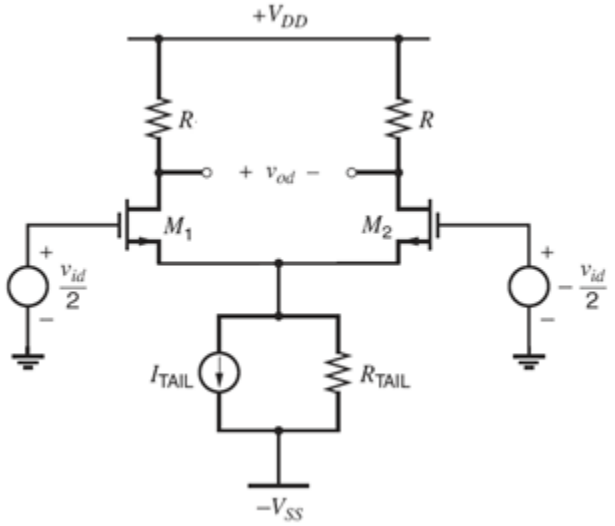


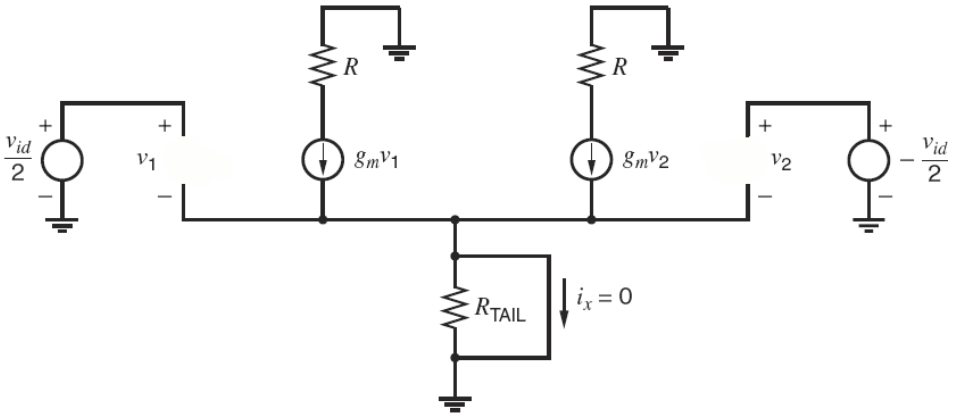
Fig. 3.55

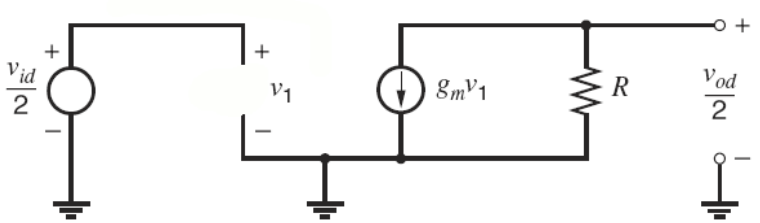
Because the circuit in Fig. 3.54 is perfectly balanced, and because the inputs are driven by equal and opposite voltages, the voltage across R_{TAIL} does not vary at all. Another way to see this result is to view the two lower parts of the circuit as voltage followers. When one side pulls up, the other side pulls down, resulting in a constant voltage across the tail current source by superposition. Since the voltage across R_{TAIL} experiences no variation, the behavior of the small-signal circuit is unaffected by the placement of a short circuit across R_{TAIL}, as shown in Fig. 3.55. After placing this short circuit, we see that the two sides of the circuit are not only identical, but also independent because they are joined at a node that operates as a small-signal ground. Therefore, the response to small-signal differential inputs can be determined by analyzing one side of the original circuit with R_{TAIL} replaced by a short circuit.

Gray, et al.. ed. 3rd

Differential gain - balanced amplifier





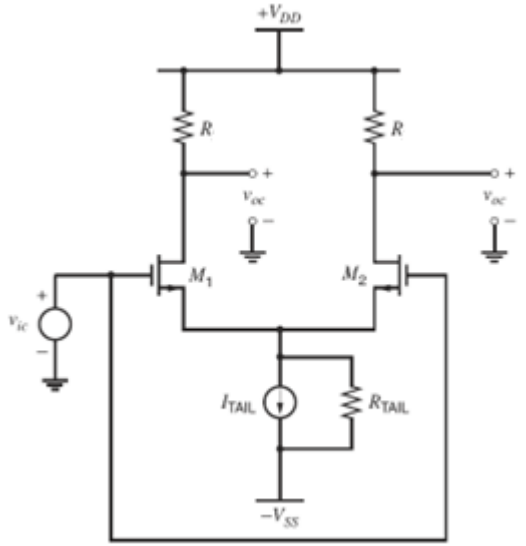


$$\frac{v_{od}}{2} = -g_m R \frac{v_{id}}{2}$$

$$A_{dm} = \left.\frac{v_{od}}{v_{id}}\right|_{v_{ic}=0} = -g_m R$$

Gray, et al.. ed. 3rd

Common mode gain



Gray, et al.. ed. 3rd

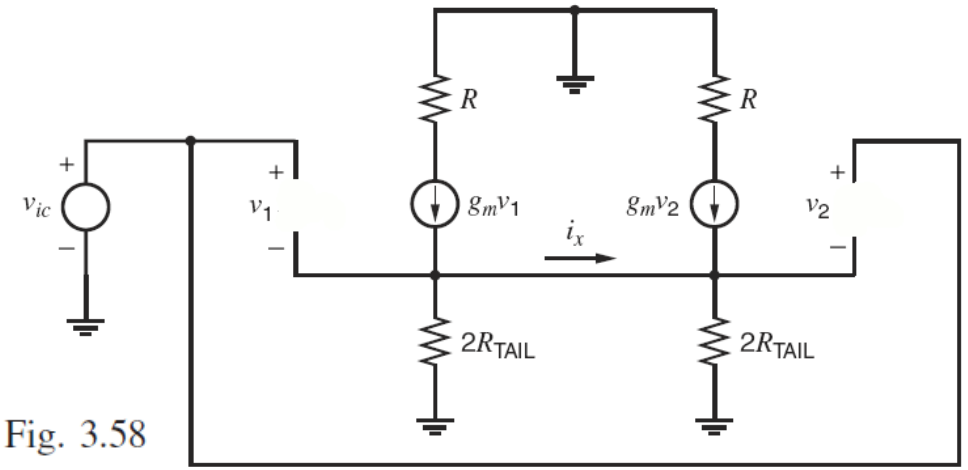
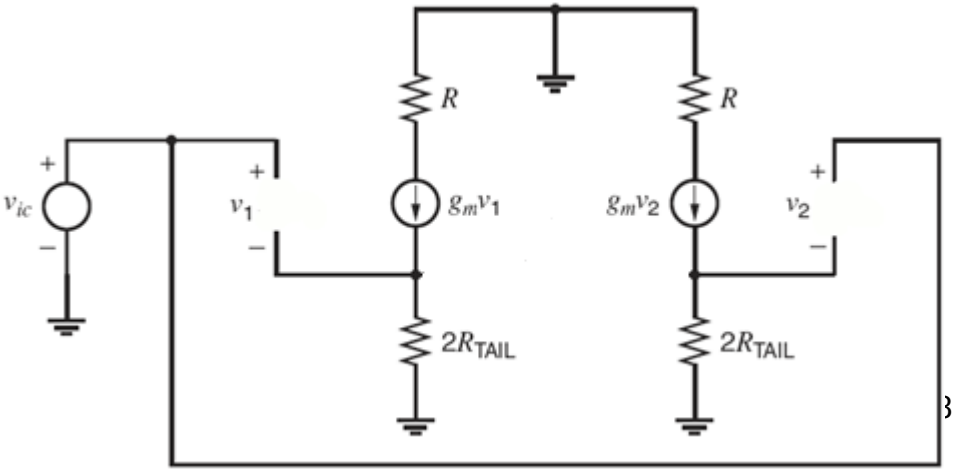
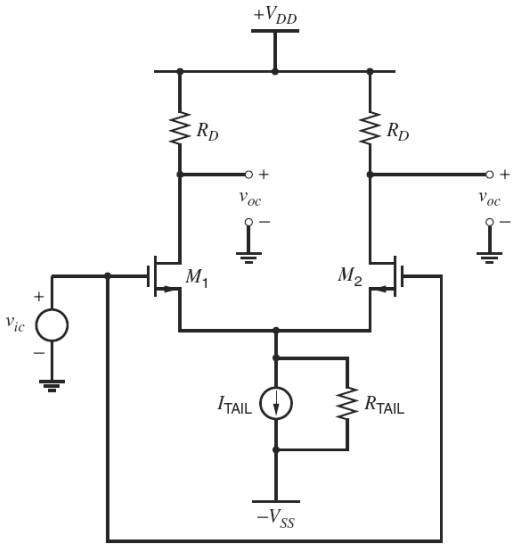


Fig. 3.58

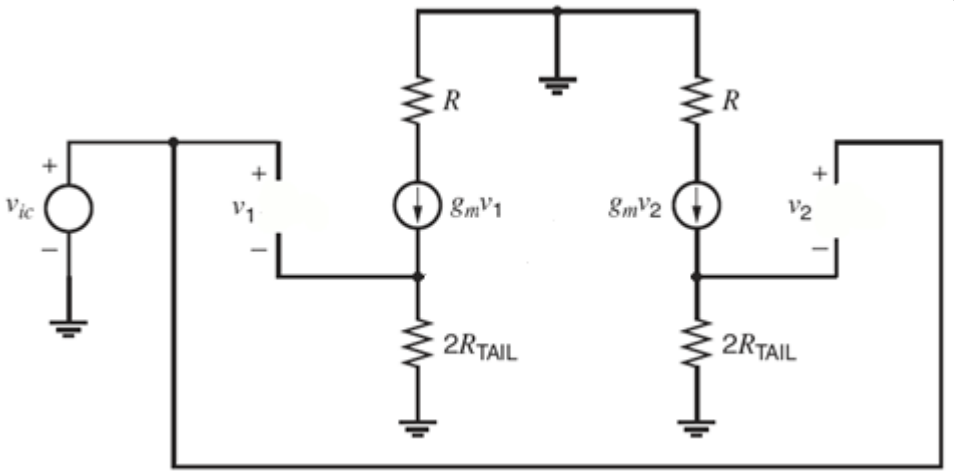
Because the circuit in Fig. 3.58 is divided into two identical halves, and because each half is driven by the same voltage v_{ic}, no current i_x flows in the lead connecting the half circuits. The circuit behavior is thus unchanged when this lead is removed as shown in



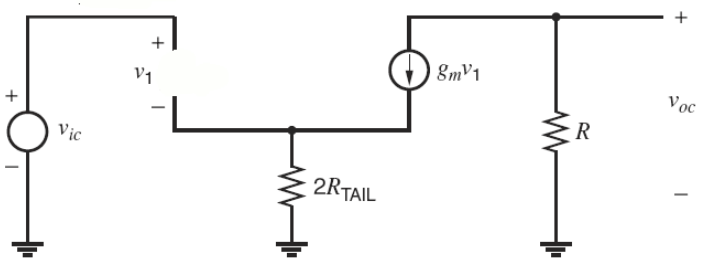
Common mode gain



Gray et al., ed. 3rd



$$A_{cm} \simeq -\frac{g_m R}{1 + g_m\,(2R_{\text{TAIL}})} = -\frac{g_m R}{1 + 2g_m R_{\text{TAIL}}}$$



the common-mode-rejection ratio, CMRR:

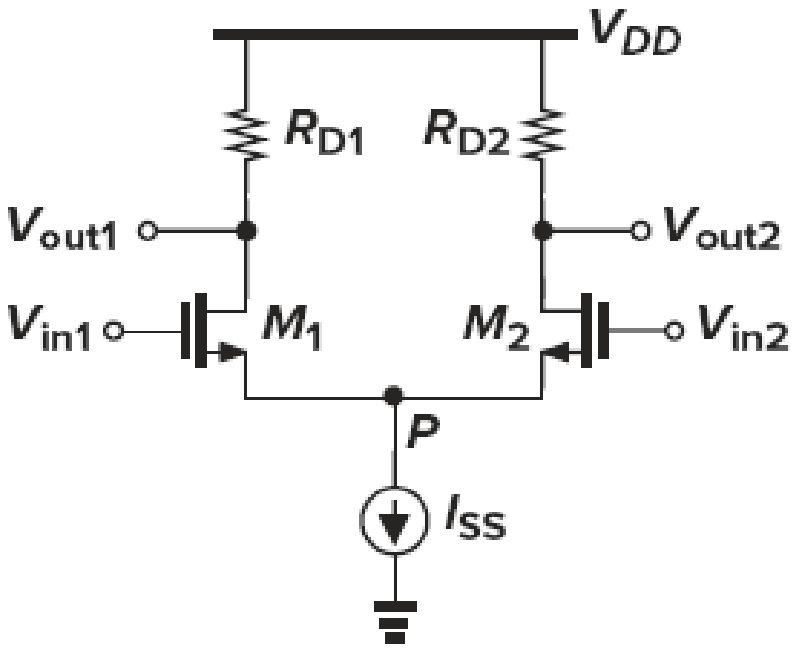
$$\text{CMRR} \equiv \left|\frac{A_{dm}}{A_{cm}}\right|$$

$$\text{CMRR} = 1 + 2g_m R_{\text{TAIL}}$$

nonzero g_{mb}

$$A_{cm} \simeq -\frac{g_m R}{1 + (g_m + g_{mb})(2R_{\text{TAIL}})} \longrightarrow \text{CMRR} \simeq 1 + 2(g_m + g_{mb})\,R_{\text{TAIL}}$$

Differential amplifiers – large signal



$$V_{in1} - V_{in2} = V_{GS1} - V_{GS2}$$

$$V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}} + V_{TH}$$

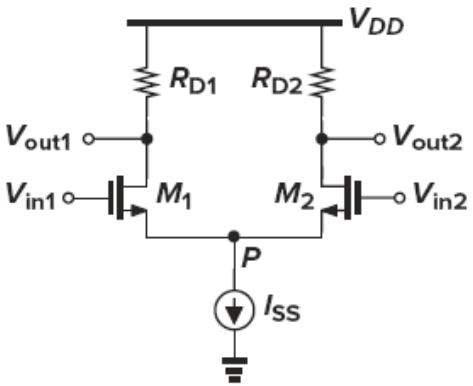
$$V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}}$$

We wish to calculate the differential output current, $I_{D1} - I_{D2}$ and we know that $I_{D1} + I_{D2} = I_{SS}$.

Razavi, ed. 2rd

Differential amplifiers – large signal

Razavi, ed. 2rd



$$I_{D1} - I_{D2} = \sqrt{\mu_n C_{ox}\frac{W}{L} I_{SS}}(V_{in1} - V_{in2})\sqrt{1 - \frac{\mu_n C_{ox}(W/L)}{4I_{SS}}(V_{in1} - V_{in2})^2}$$

$$I_{D1} + I_{D2} = I_{SS}$$

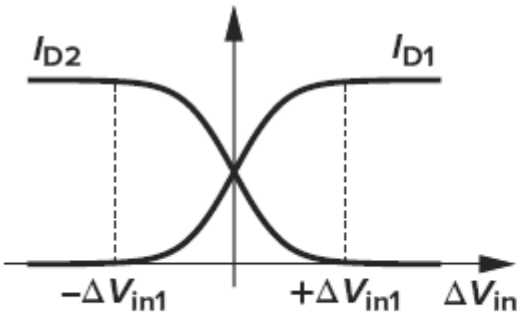
We can say that $M1$, $M2$, and the tail operate as a voltage-dependent current source producing $I_{D1} - I_{D2}$ according to the above large-signal characteristics. As expected, $I_{D1}-I_{D2}$ is an odd function of $V_{in1}-V_{in2}$

equivalent G_m of M_1 and M_2

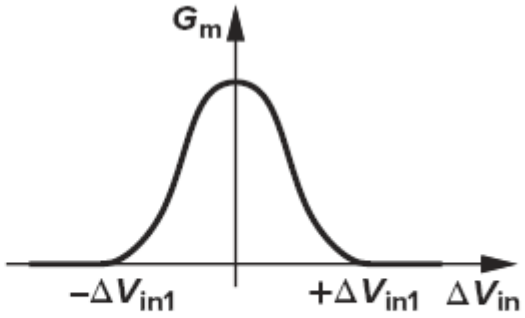
$$\frac{\partial \Delta I_D}{\partial \Delta V_{in}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\frac{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - 2\Delta V_{in}^2}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - \Delta V_{in}^2}}$$

For $\Delta V_{in} = 0$, G_m is maximum and equal to $\sqrt{\mu_n C_{ox}(W/L) I_{SS}}$

$$|A_v| = \sqrt{\mu_n C_{ox}\frac{W}{L} I_{SS}} R_D$$



(a)



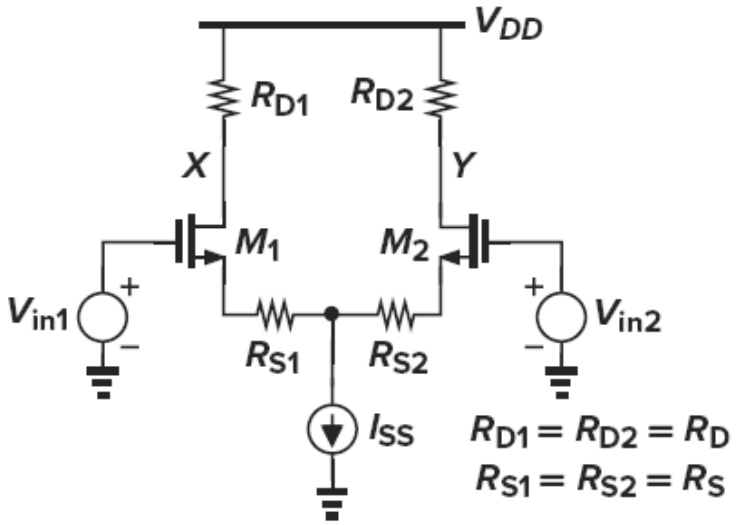
(b)

Variation of drain currents and overall transconductance of a differential pair versus input voltage.

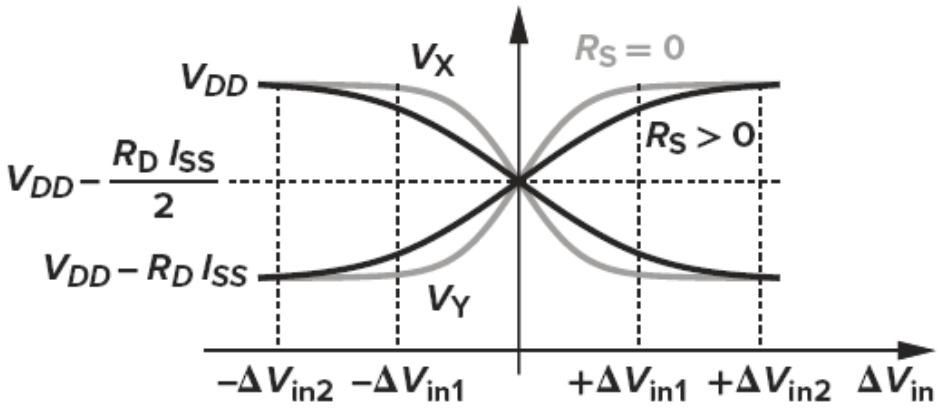
Degenerated differential pair

Razavi, ed. 2rd

As with a simple common-source stage, a differential pair can incorporate resistive degeneration to improve its linearity.



(a)



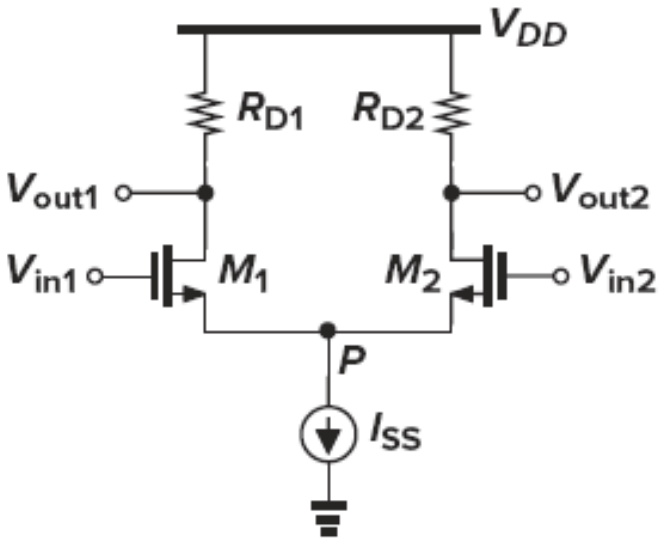
(b)

The small-signal voltage gain of the degenerated differential pair can be obtained by applying the half-circuit concept. The half circuit is simply a degenerated CS stage, exhibiting a gain of

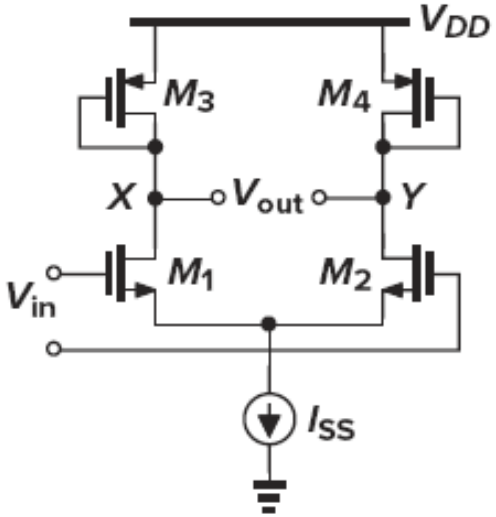
$$|A_v| = \frac{R_D}{\frac{1}{g_m} + R_S}$$

Differential pair with MOS loads (diode connected) – differentia gain

Razavi, ed. 2rd



$$A_v = -g_m R_D$$



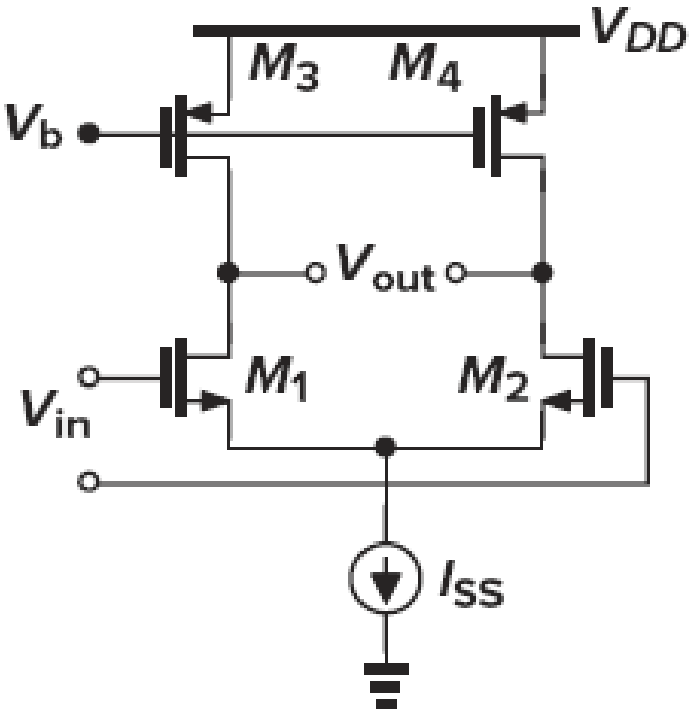
$$A_v = -g_{mN}\left(g_{mP}^{-1} \| r_{ON} \| r_{OP}\right)$$

$$\approx -\frac{g_{mN}}{g_{mP}}$$

$$A_v \approx -\sqrt{\frac{\mu_n (W/L)_N}{\mu_p (W/L)_P}}$$

Differential pair with MOS loads (current source load)

Razavi, ed. 2rd

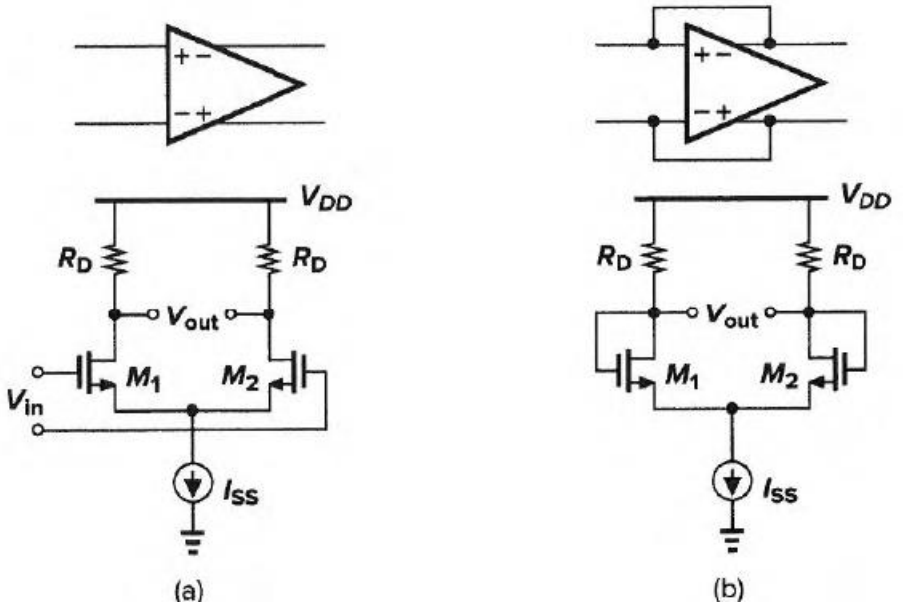


$$A_v = -g_{mN}(r_{ON} \| r_{OP})$$

High gain differential circuits require Common Mode Feedback (CMFB)

Common – mode feedback: basic concept

High gain differential circuits require Common Mode Feedback (CMFB)

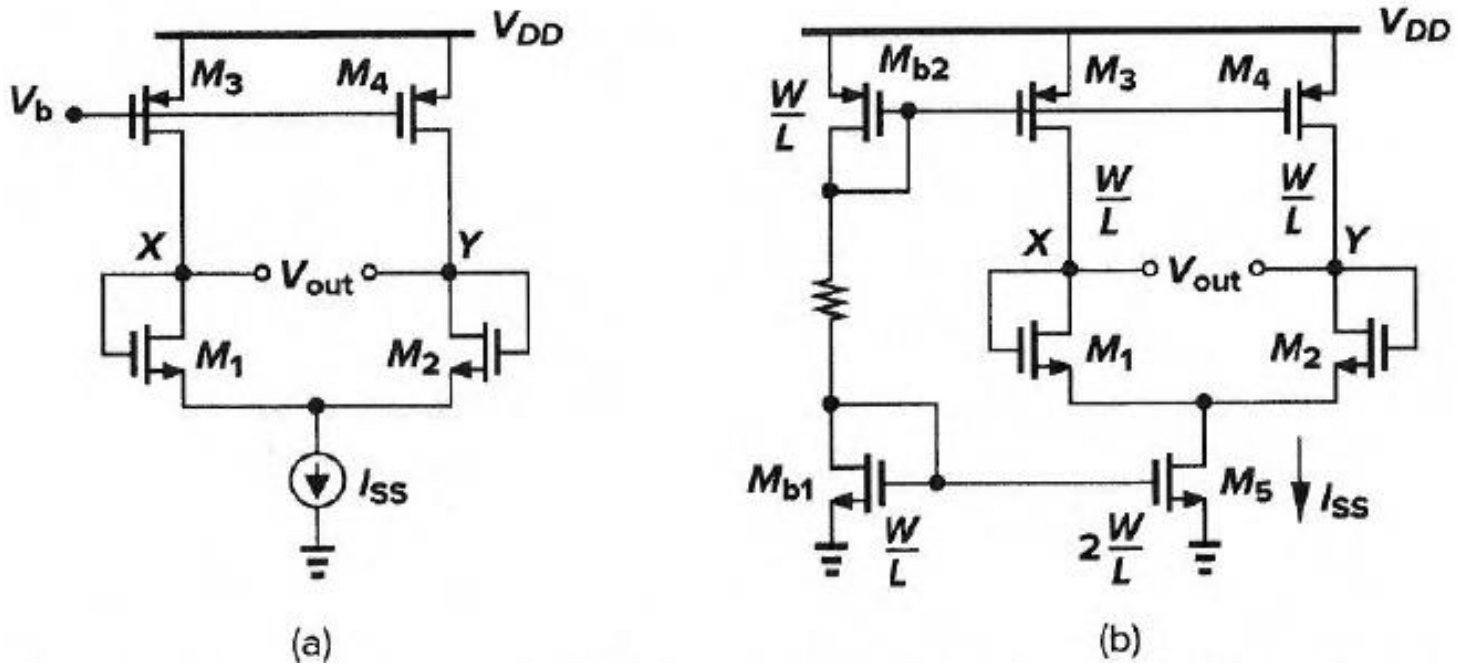


(a) Simple differential pair; (b) circuit with inputs shorted to outputs.

In some applications we short the inputs and outputs for part of operation, providing differential negative feedback. The input and output common-mode levels in this case are fairly well defined, equal to V_{DD}-$I_{SS}R_D$/2.

Common – mode feedback: basic concept

What is the common node level at nodes V_X and V_Y?

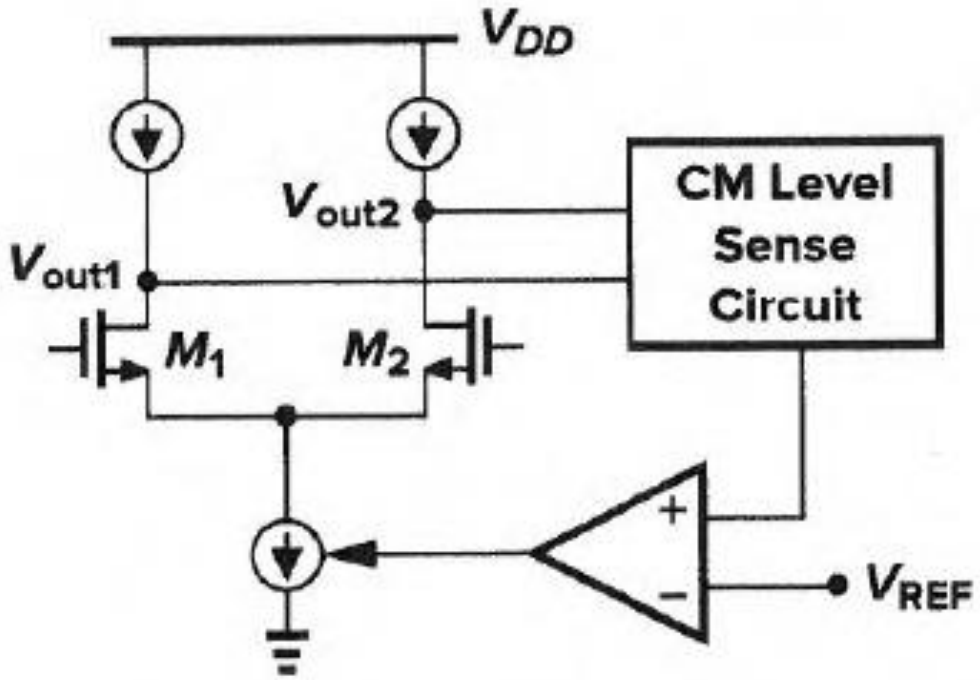


(a) High-gain differential pair with inputs shorted to outputs, and (b) effect of current mismatches.

Since each of the input transistors carries a current $I_{SS}/2$, the CM level depends on how close I_{D3} and I_{D4} are to this value.

1) $I_{D3,4} > I_{SS}/2$: M3 and M4 enter the triode region
2) $I_{D3,4} < I_{SS}/2$: M5 enters the triode region

Common – mode feedback: conceptual topology

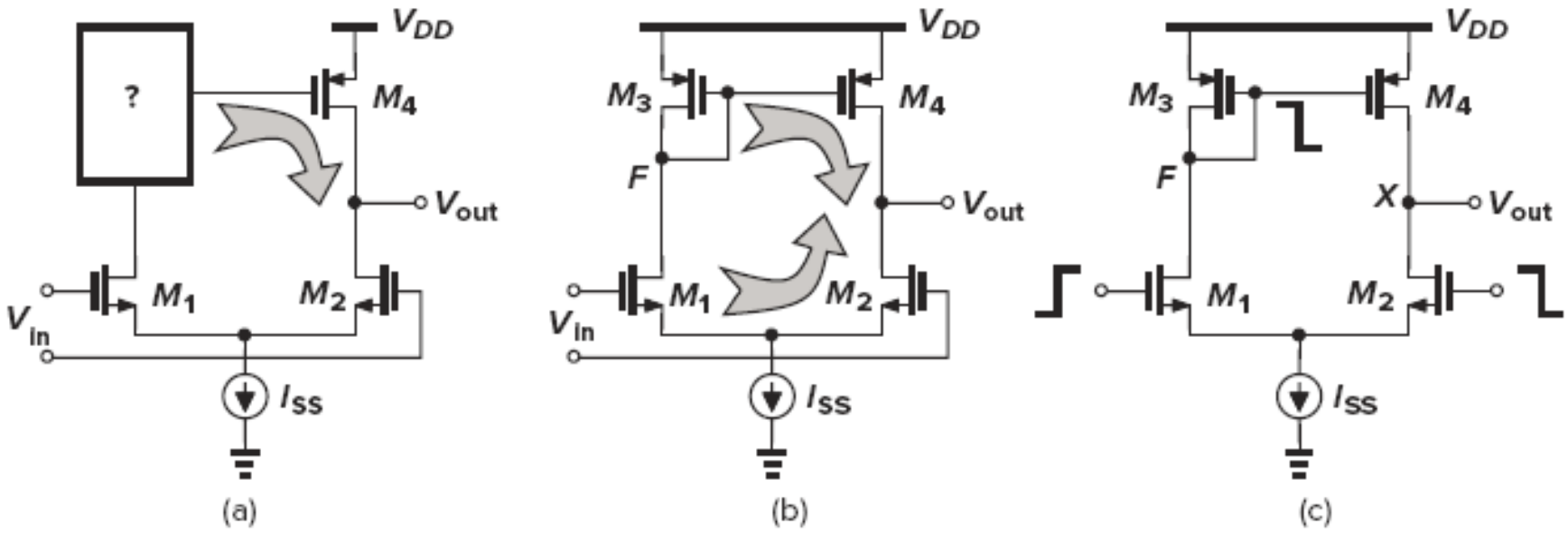


CM feedback is necessary – the task can be divided into 3 operation:

1) Sensing the output CM level,
2) Comparision with the reference
3) Returning the error to the bias amplifier's network

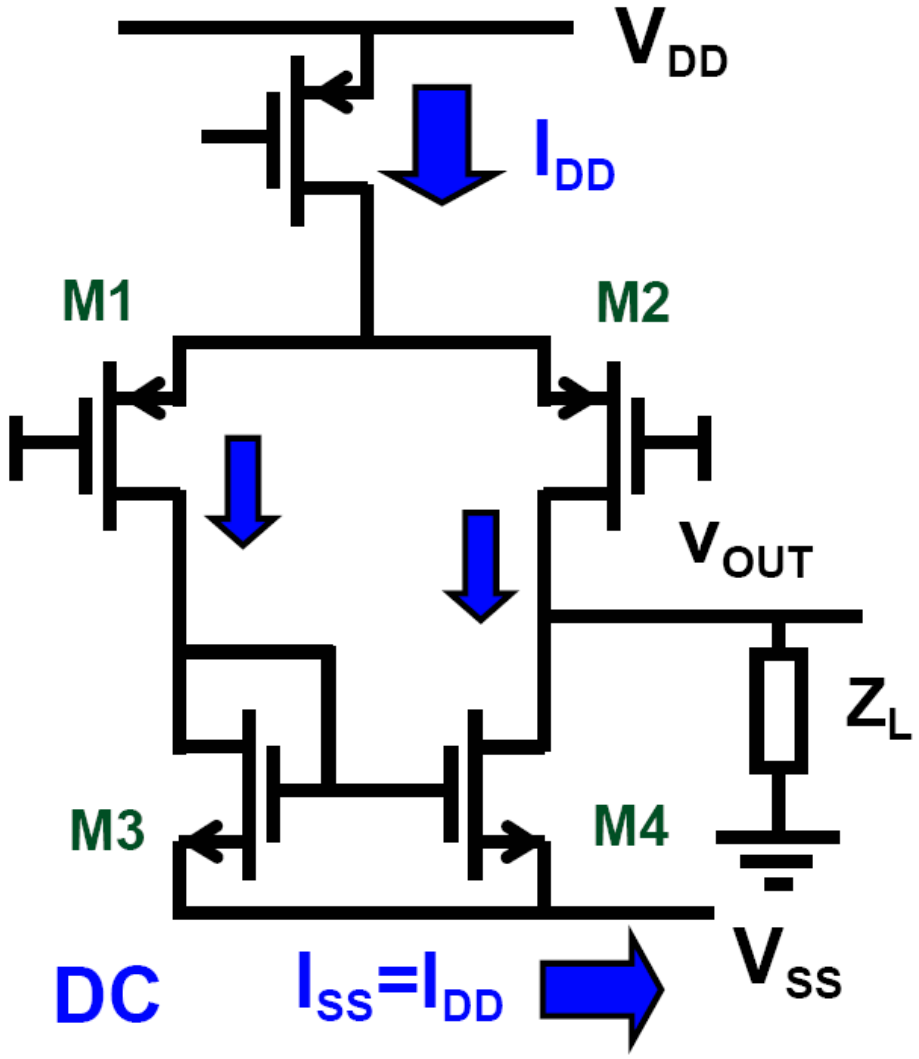
Razavi, McGrawHill, 2016

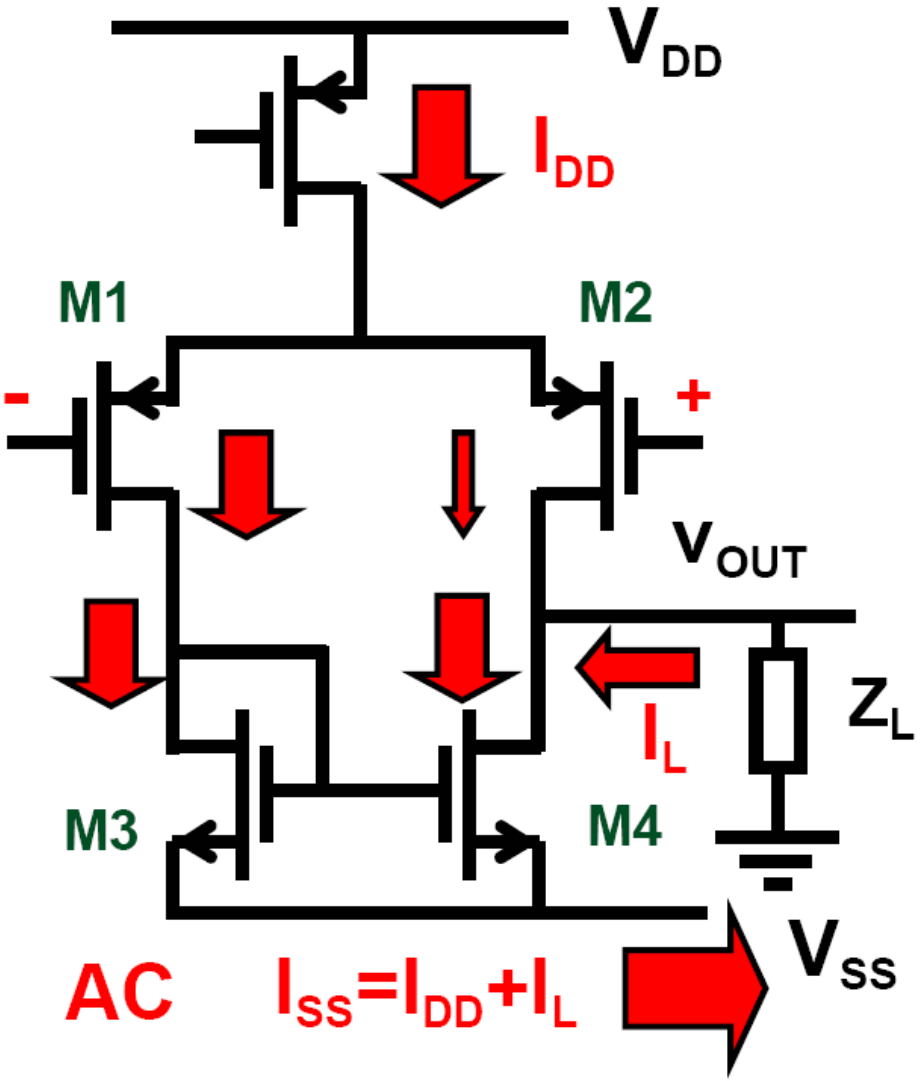
Differential pair with active load



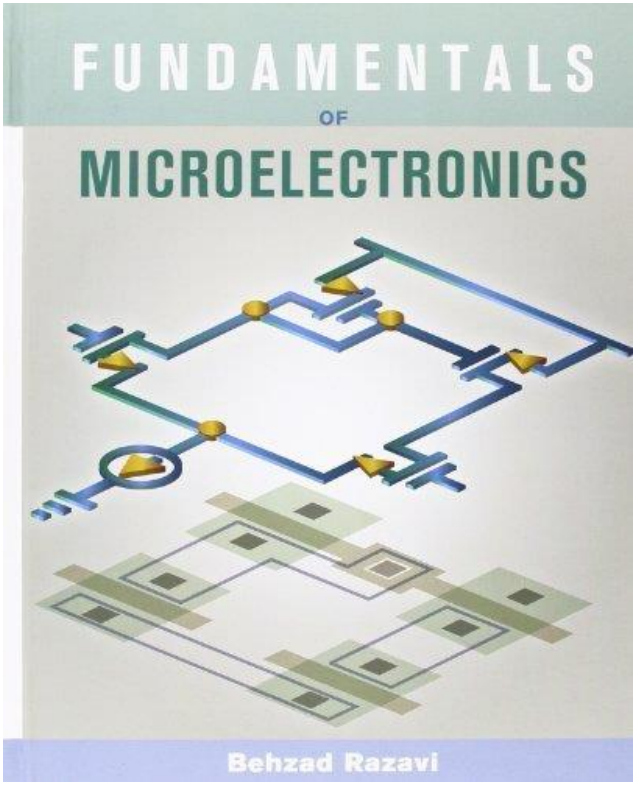
(a) Concept of combining the drain currents of M_1 and M_2, (b) realization of (a), and (c) response of the circuit to differential inputs.

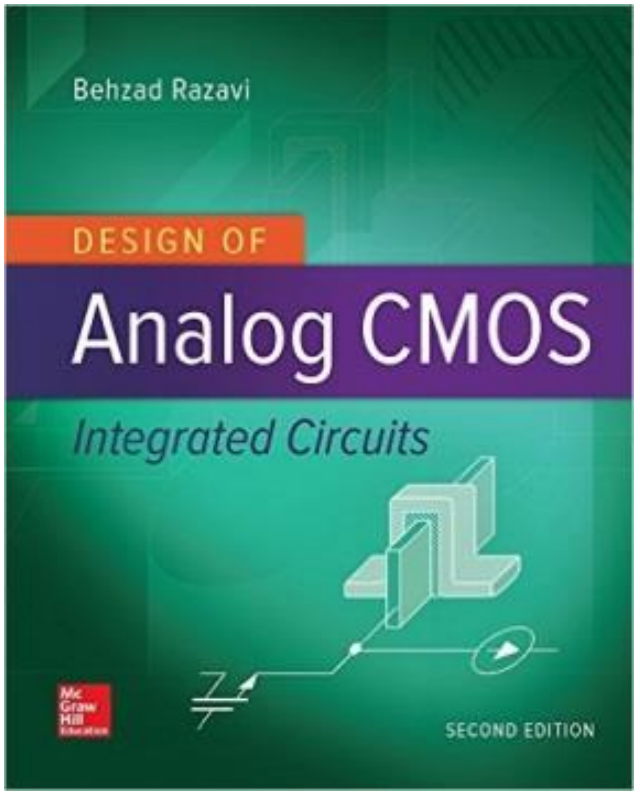
Operational Transconductance Amplifier (OTA)



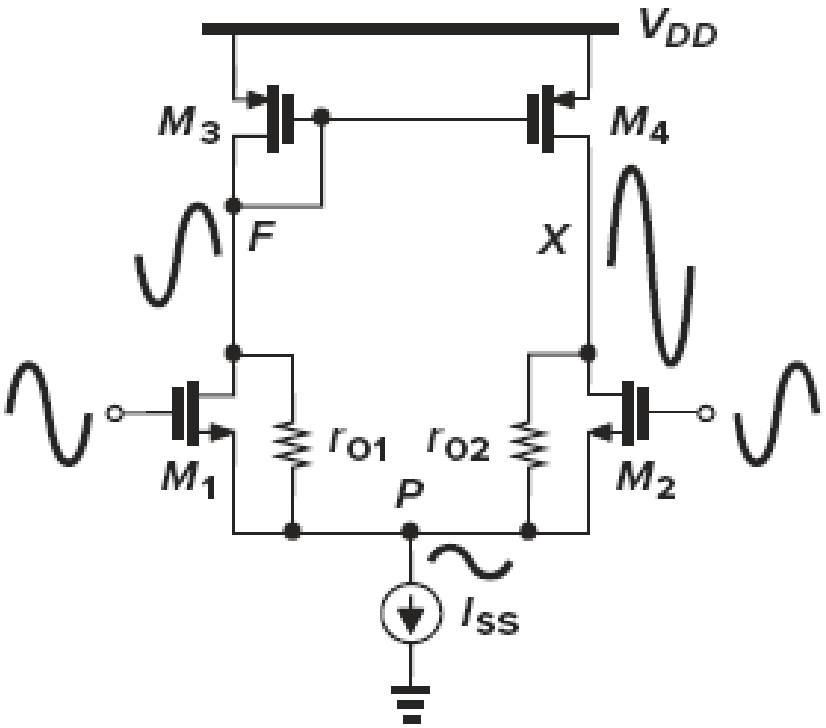


MOS Differential Pair with Active Load
Gain Calculation





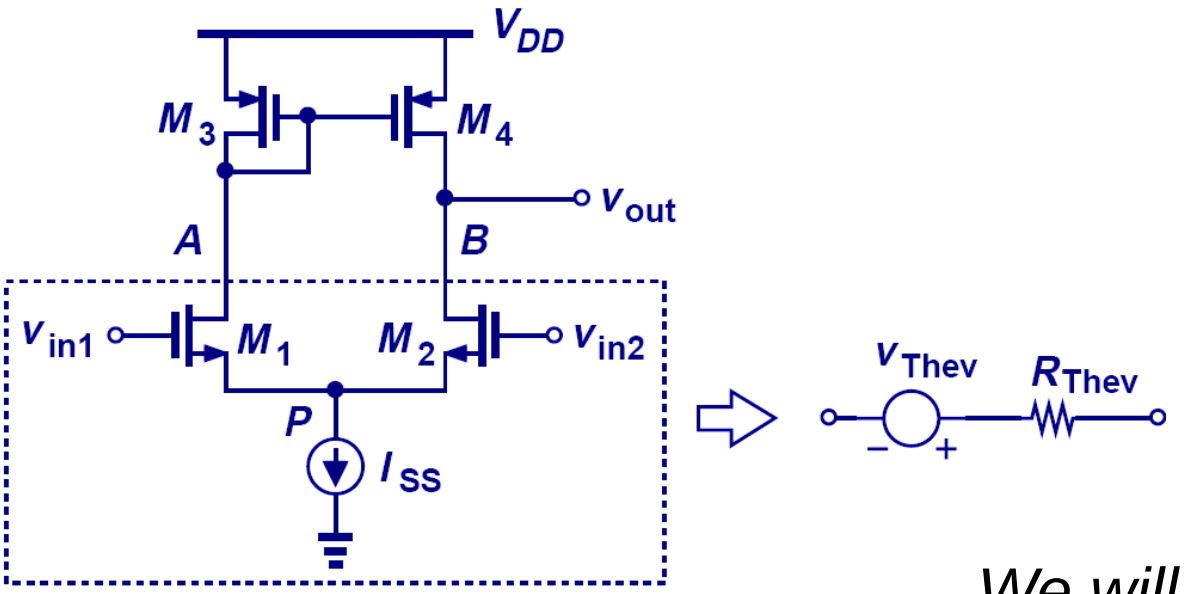
Small signal analysis
Can we use half circuit concept?



With small differential inputs, the voltage swings at nodes *F* and *X* are vastly different. This is because the diode-connected device M_3 yields a much lower voltage gain from the input to node *F* than that from the input to node *X*. As a result, the effects of V_F and V_X at node *P* (through r_{O1} and r_{O2}, respectively) do not cancel each other, and this node cannot be considered a virtual ground.

Thevenin Equivalent of the Input Pair – Approach II

In this approach, we decompose the circuit into sections that more easily lend themselves to analysis by inspection. As illustrated in Fig., we first seek a Thevenin equivalent for the section consisting of vin1, vin2, M1 and M2, assuming vin1 and vin2 are differential. Recall that v_{Thev} is the voltage between A and B in the "open-circuit condition."



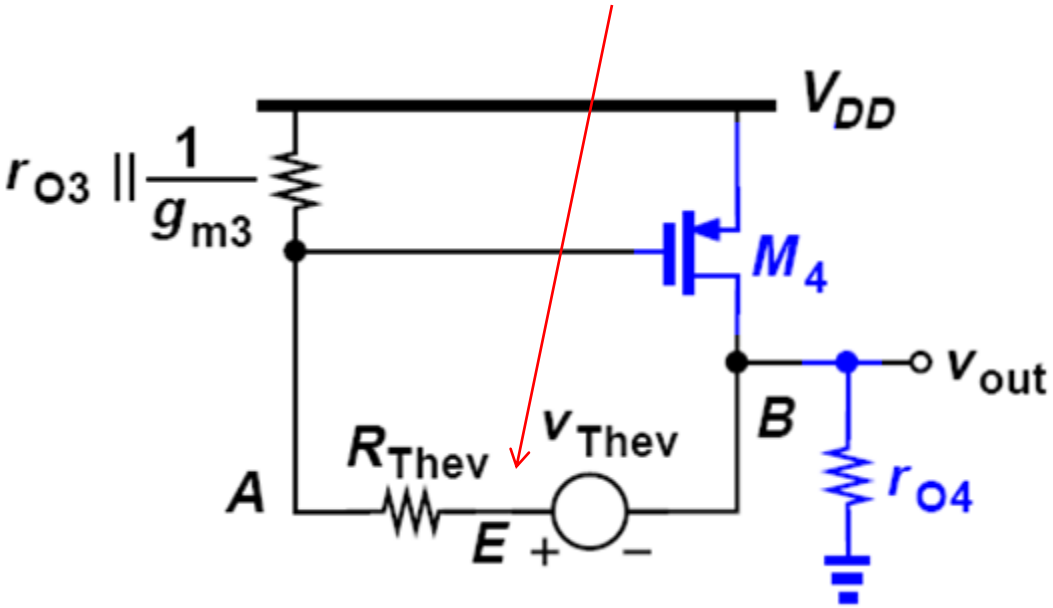
We will prove that:

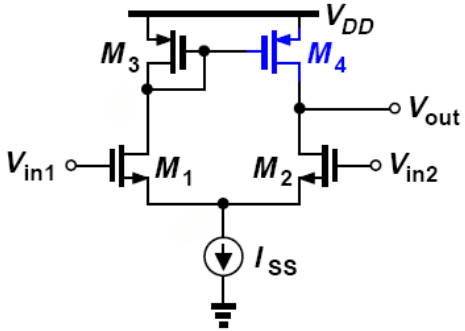
$$v_{Thev} = -g_{mN} r_{oN} (v_{in1} - v_{in2})$$

$$R_{Thev} = 2r_{oN}$$

Simplified Differential Pair with Active Load Approach II

Having reduced the input sources and transistors to a Thevenin equivalent, we now compute the gain of the overall amplifier. Figure depicts the simplified circuit, where the diode-connected transistor M_3 is replaced with $(1/g_{m3})||r_{O3}$ and the output impedance of M_4 is drawn explicitly. The objective is to calculate v_{out} in terms of v_{Thev}. Since the voltage at node E with respect to ground is equal to $v_{out} + v_{Thev}$, we can view v_A as a divided version of v_E:

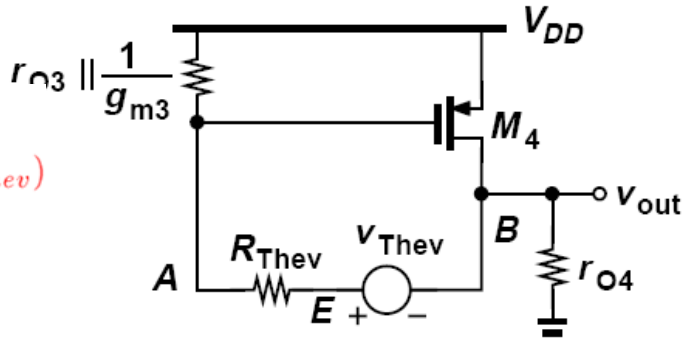




$$v_A = \frac{\frac{1}{g_{m3}}||r_{O3}}{\frac{1}{g_{m3}}||r_{O3} + R_{Thev}}(v_{out} + v_{Thev})$$

Simplified Differential Pair with Active Load Approach II

$$v_A = \frac{\frac{1}{g_{m3}}||r_{O3}}{\frac{1}{g_{m3}}||r_{O3} + R_{Thev}}(v_{out} + v_{Thev})$$



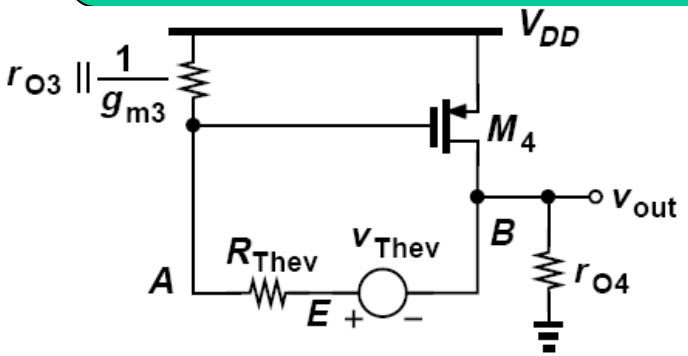
Given by $g_{m4}v_A$, the small-signal drain current of M_4 must satisfy KCL at the output node:

$$g_{m4}v_A + \frac{v_{out}}{r_{O4}} + \frac{v_{out} + v_{Thev}}{\frac{1}{g_{m3}}||r_{O3} + R_{Thev}} = 0$$

where the last term on the left hand side represents the current flowing through R_{Thev}. It follows

$$\left(g_{m4} \frac{\frac{1}{g_{m3}}||r_{O3}}{\frac{1}{g_{m3}}||r_{O3} + R_{Thev}} + \frac{1}{\frac{1}{g_{m3}}||r_{O3} + R_{Thev}} \right) (v_{out} + v_{Thev}) + \frac{v_{out}}{r_{O4}} = 0$$

Simplified Differential Pair with Active Load Approach II



$$\left(g_{m4} \frac{\frac{1}{g_{m3}} \| r_{O3}}{\frac{1}{g_{m3}} \| r_{O3} + R_{Thev}} + \frac{1}{\frac{1}{g_{m3}} \| r_{O3} + R_{Thev}} \right) (v_{out} + v_{Thev}) + \frac{v_{out}}{r_{O4}} = 0$$

Recognizing that $1/g_{m3} \ll r_{O3}$, and $1/g_{m3} \ll R_{Thev}$ and assuming $g_{m3} = g_{m4} = g_{mp}$ and $r_{O3} = r_{O4} = r_{OP}$, we reduce to

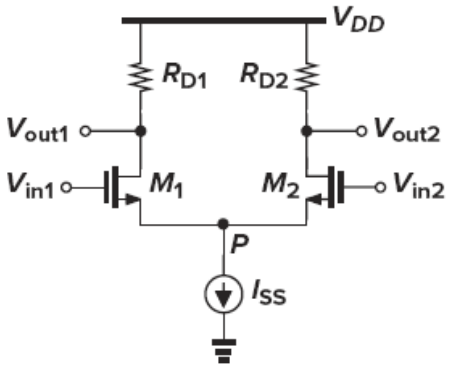
$$\frac{2}{R_{Thev}}(v_{out} + v_{Thev}) + \frac{v_{out}}{r_{OP}} = 0$$

$$v_{out}\left(\frac{1}{r_{ON}} + \frac{1}{r_{OP}}\right) = \frac{g_{mN} r_{ON}(v_{in1} - v_{in2})}{r_{ON}}$$

$$\frac{v_{out}}{v_{in1} - v_{in2}} = g_{mN}(r_{ON} \| r_{OP})$$

ADDITIONAL SLIDES

Differential amplifiers – large signal



$$V_{in1} - V_{in2} = V_{GS1} - V_{GS2}$$

$$V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}} + V_{TH} \qquad V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}}$$

We wish to calculate the differential output current, $I_{D1} - I_{D2}$. Squaring the two sides of above eq. and recognizing that $I_{D1} + I_{D2} = I_{SS}$, we obtain

$$(V_{in1} - V_{in2})^2 = \frac{2}{\mu_n C_{ox}\frac{W}{L}}(I_{SS} - 2\sqrt{I_{D1}I_{D2}})$$

$$\longrightarrow \qquad \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2 - I_{SS} = -2\sqrt{I_{D1}I_{D2}}$$

Squaring the two sides again and noting that

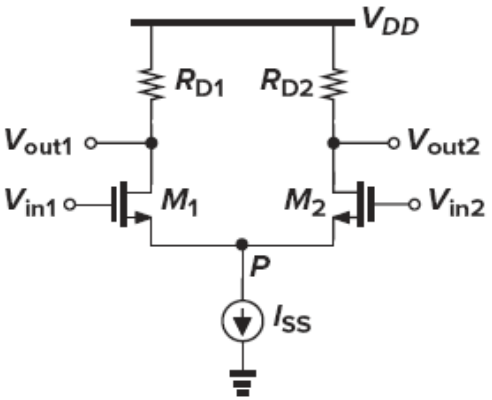
$$4I_{D1}I_{D2} = (I_{D1}+I_{D2})^2 - (I_{D1}-I_{D2})^2 = I_{SS}^2 - (I_{D1}-I_{D2})^2$$

we arrive at

$$(I_{D1} - I_{D2})^2 = -\frac{1}{4}\left(\mu_n C_{ox}\frac{W}{L}\right)^2 (V_{in1} - V_{in2})^4 + I_{SS}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2$$

Razavi, p. 107, ed. 2rd

Differential amplifiers – large signal



$$(I_{D1} - I_{D2})^2 = -\frac{1}{4}\left(\mu_n C_{ox}\frac{W}{L}\right)^2 (V_{in1} - V_{in2})^4 + I_{SS}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2$$

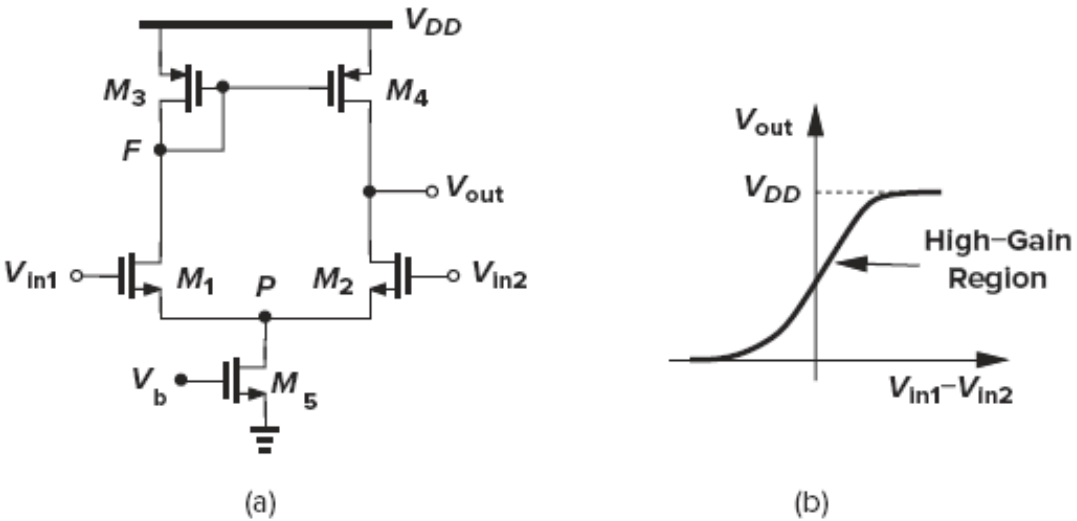
$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1} - V_{in2})^2}$$

$$I_{D1} - I_{D2} = \sqrt{\mu_n C_{ox}\frac{W}{L}I_{SS}}(V_{in1} - V_{in2})\sqrt{1 - \frac{\mu_n C_{ox}(W/L)}{4I_{SS}}(V_{in1} - V_{in2})^2}$$

We can say that *M*1, *M*2, and the tail operate as a voltage-dependent current source producing $I_{D1} - I_{D2}$ according to the above large-signal characteristics. As expected, $I_{D1}-I_{D2}$ is an odd function of $V_{in1}-V_{in2}$

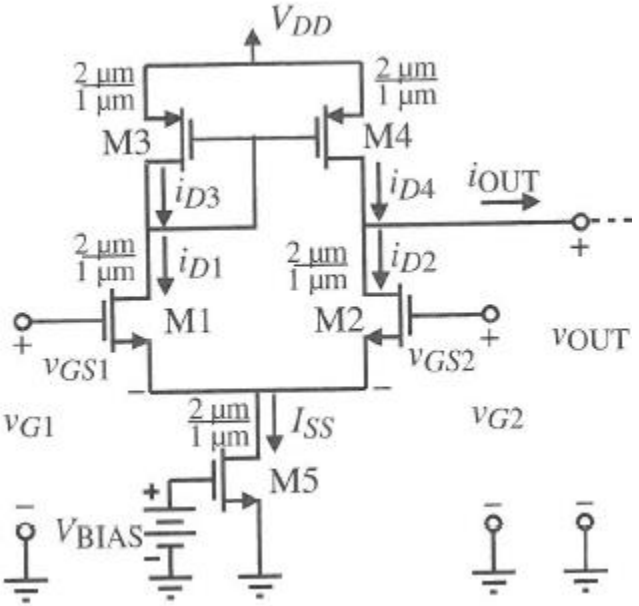
Razavi, p. 107, ed. 2rd

Large signal analysis (homework p. 149-150)

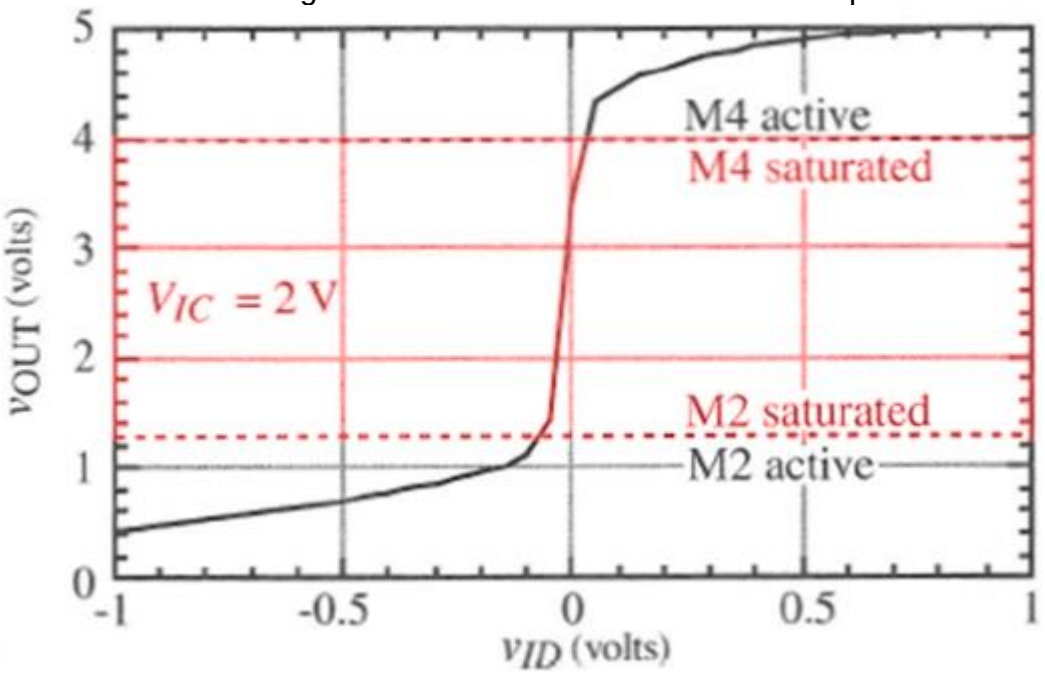


(a) Differential pair with active current mirror and realistic current source; (b) large-signal input-output characteristic.

Differential amplifiers
(large signal analysis)



Voltage-transfer curve for the differential amplifier



High gain <=> M2 and M4 must be saturated

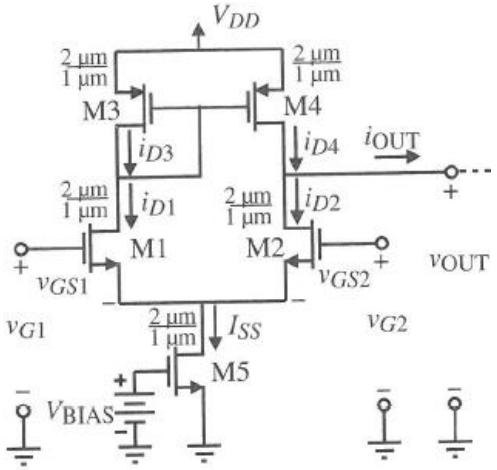
M2 is saturated when: $V_{out} \geq V_{S2}+V_{DS2sat} \rightarrow V_{out} \geq V_{S2}+(V_{IC} - V_{S2} - V_{TN}) \rightarrow V_{out} \geq V_{IC} - V_{TN}$

M4 is saturated when: $V_{out} \leq V_{DD} - | V_{DS4sat} | \rightarrow V_{out} \leq V_{DD} - | V_{GS4} - V_{TP} |$

Allen, CMOS Circuit Design ed. 3rd

Differential amplifiers
Input Common Mode Range

Another important characteristic of a differential amplifier is input common-mode range, ICMR. The way that the ICMR is found is to set v_{ID} to zero and vary v_{IC} until one of the transistors in the differential amplifier is no longer saturated.



There are two paths from V_{IC} to V_{DD} that we must examine. The first is from G1 through M1 and M3 to V_{DD}. The second is from G2 through M2 and M4 to V_{DD}.

1st path to V_{DD}: $V_{IC(max)} = V_{G1(max)} = V_{DD} - |V_{GS3}| - V_{DS1sat} + V_{GS1} = V_{DD} - |V_{GS3}| + V_{TN1}$

2nd path to V_{DD}: $V'_{IC(max)} = V_{DD} - |V_{DS4sat}| - V_{DS2sat} + V_{GS2} = V_{DD} - |V_{DS4sat}| + V_{TN2}$

path to V_{SS}: $V_{IC(min)} = V_{DS5sat} + V_{GS1(2)}$

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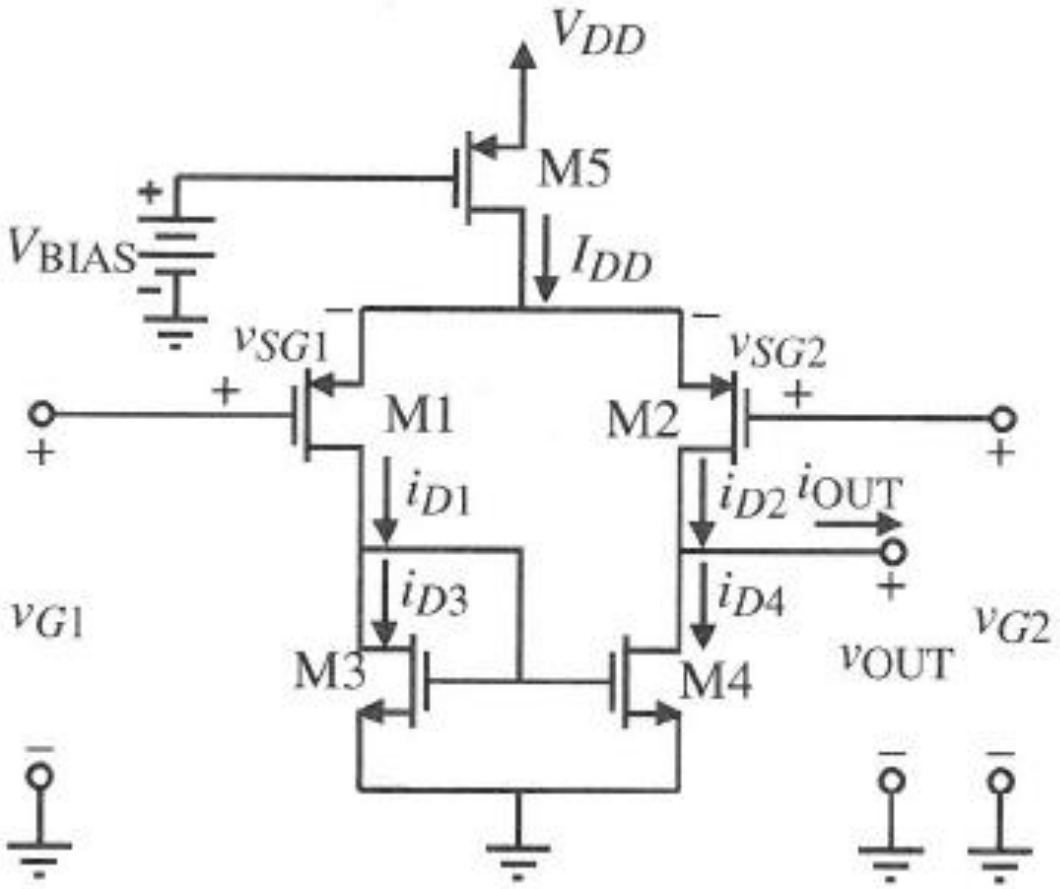
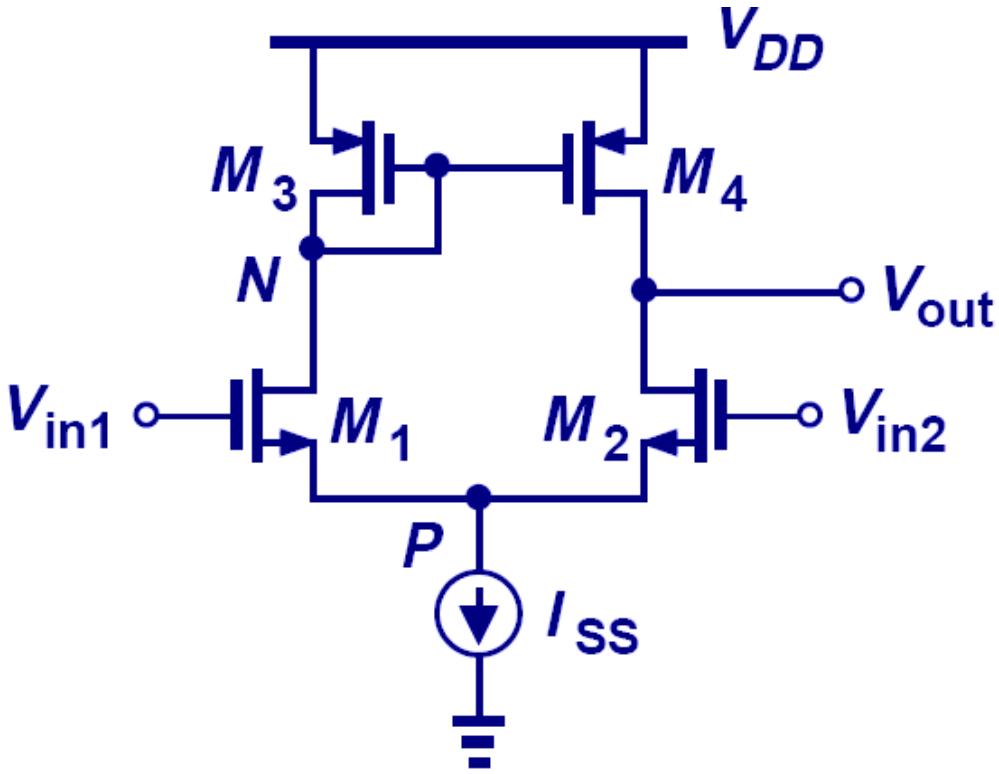
Differential amplifiers
PMOS input transistors



Allen, CMOS Circuit Design ed. 3rd

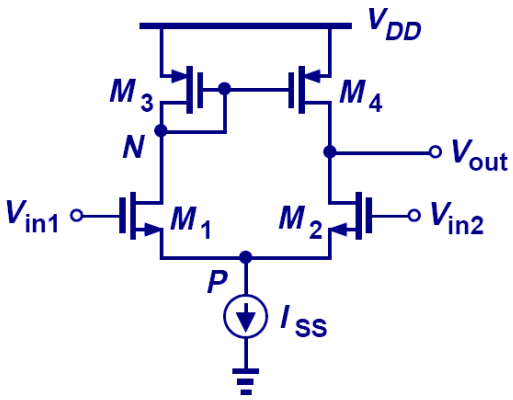
Asymmetric Differential Pair

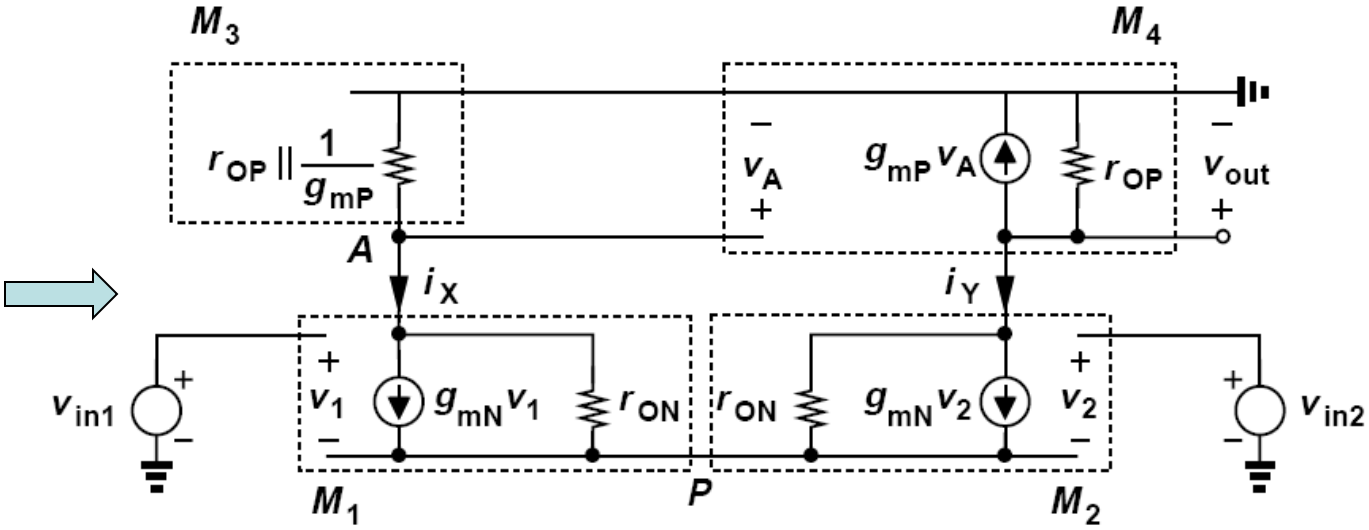


While the transistors themselves are symmetric and the input signals are small and differential, the circuit is asymmetric. With the diode connected device, M3, creating a low impedance at node A, we expect a relatively small voltage swing—on the order of the input swing—at this node. On the other hand, transistors M2 and M4 provide a high impedance and hence a large voltage swing at the output node.

The asymmetry resulting from the very different voltage swings at the drains of M1 and M2 disallows grounding node P for small-signal analysis. We present two approaches to solving this circuit.

Gain calculation – Approach I





Without a half circuit available, the analysis can be performed through the use of a complete small-signal model of the amplifier. Referring to the equivalent circuit shown in Fig., where the dashed boxes indicate each transistor, we perform the analysis in two steps.

In the first step, we note that i_X and i_Y must add up to zero at node P and hence $i_X = - i_Y$. Also,

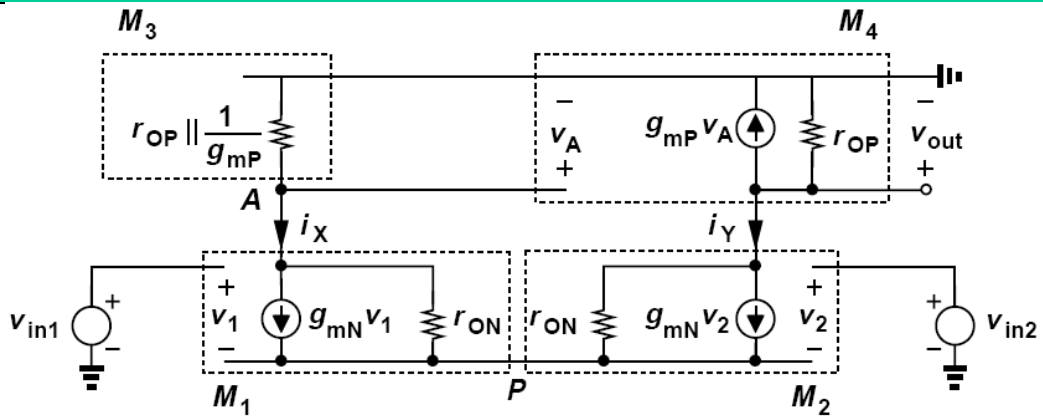
$$v_A = -i_X(g_{mP}^{-1} || r_{OP})$$

and

$$\begin{aligned} -i_Y &= \frac{v_{out}}{r_{OP}} + g_{mP} v_A \\ &= \frac{v_{out}}{r_{OP}} - g_{mP} i_X \left(\frac{1}{g_{mP}} || r_{OP}\right) \\ &= i_X. \end{aligned}$$

$$i_X = \frac{v_{out}}{r_{OP}\left[1 + g_{mP}\left(\frac{1}{g_{mP}} || r_{OP}\right)\right]}$$

Gain calculation – Approach I



In the second step, we write a KVL around the loop consisting of all four transistors. The current through r_{ON} of M_1 is equal to $i_X - g_{mN}v_1$ and that through r_{ON} of M_2 equal to $i_Y - g_{mN}v_2$. It follows that

$$-v_A + (i_X - g_{mN}v_1)r_{ON} - (i_Y - g_{mN}v_2)r_{ON} + v_{out} = 0.$$

Since $v_1 - v_2 = v_{in1} - v_{in2}$ and $i_X = -i_Y$,

$$-v_A + 2i_X r_{ON} - g_{mN}r_{ON}(v_{in1} - v_{in2}) + v_{out} = 0.$$

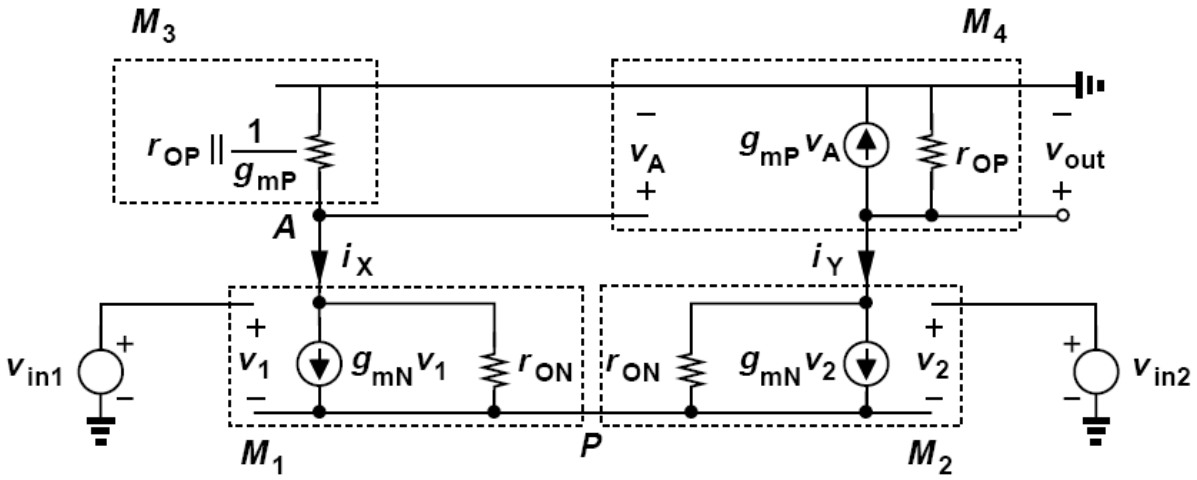
$$v_A = -i_X(g_{mP}^{-1} || r_{OP})$$

$$i_X = \frac{v_{out}}{r_{OP}[1 + g_{mP}(\frac{1}{g_{mP}} || r_{OP})]}$$

Substituting for v_A and i_X from above, we have

$$\frac{v_{out}}{r_{OP}[1 + g_{mP}(\frac{1}{g_{mP}} || r_{OP})]}(\frac{1}{g_{mP}} || r_{OP}) + 2r_{ON}\frac{v_{out}}{r_{OP}[1 + g_{mP}(\frac{1}{g_{mP}} || r_{OP})]} + v_{out} = g_{mN}r_{ON}(v_{in1} - v_{in2}).$$

Gain calculation – Approach I



Solving for v_{out} yields

~1

$$\frac{v_{out}}{v_{in1} - v_{in2}} = g_{mN} r_{ON} \frac{r_{OP}[1 + g_{mP}(\frac{1}{g_{mP}} || r_{OP})]}{2r_{ON} + 2r_{OP}}.$$

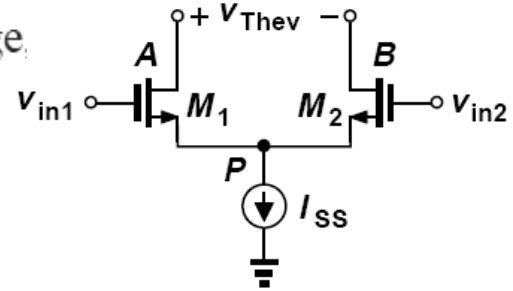
This is the exact expression for the gain. If $g_{mP} r_{OP} \gg 1$, then

$$\frac{v_{out}}{v_{in1} - v_{in2}} = g_{mN}(r_{ON} || r_{OP}).$$

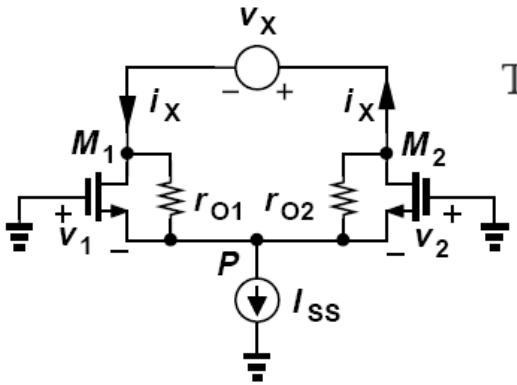
The gain is indepedent of g_{mP} and equal to that of the fully-differential circuit. In other words, the use of the active load has restored the gain.

Thevenin Equivalent of the Input Pair – Approach II

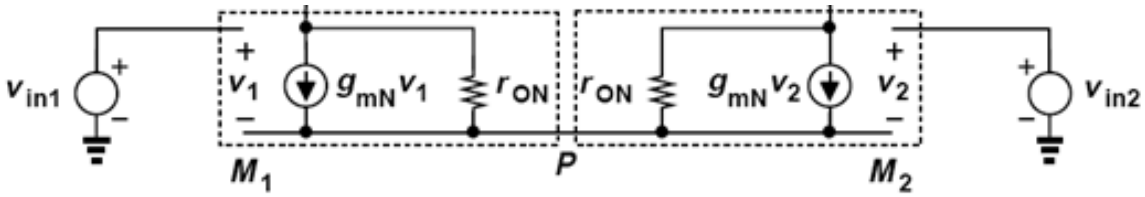
Thevenin voltage



Thevenin resistance



"open-circuit condition".



$$v_1 - v_2 = v_{in1} - v_{in2}$$

$$v_{Thev} = -g_{mN} r_{ON} (v_{in1} - v_{in2})$$

To determine the Thevenin resistance, we set the inputs to zero and apply a voltage between the output terminals [Fig. Noting that M_1 and M_2 have equal gate-source voltages ($v_1 = v_2$) and writing a KVL around the "output" loop, we have

$$(i_X - g_{m1} v_1) r_{O1} + (i_X + g_{m2} v_2) r_{O2} = v_X$$

$$\Rightarrow \quad R_{Thev} = 2 r_{ON}$$