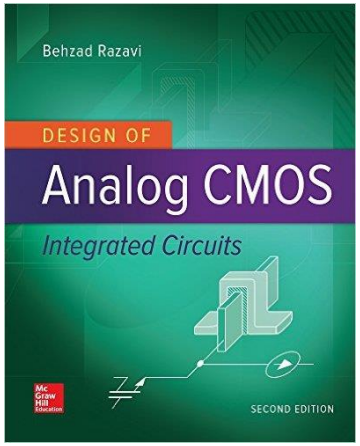
Analog circuits based on MOS transistor

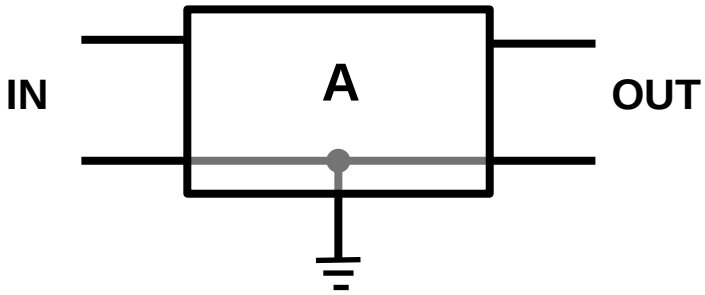
- **Basic configuration**
- **Zin, Zout**
- **Common source**
- **Current source (simple current mirror)**

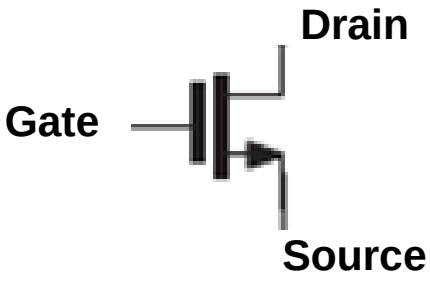
Recommended book:

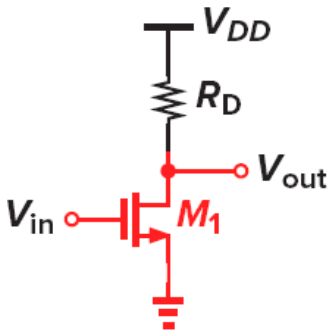


B. Razavi, McGraw-Hill Higher Education;
2 edition (January 22, 2016)

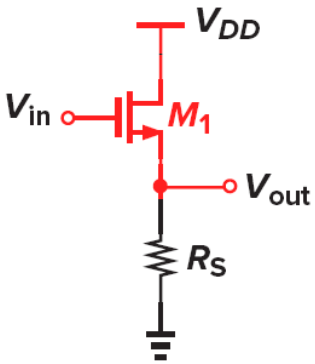
Basic configuration



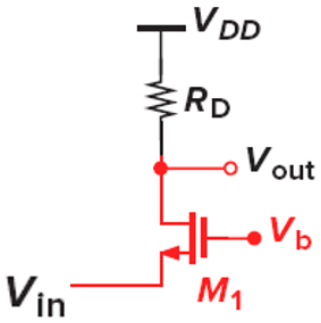




Common source



Common drain
(source follower)



Common gate

Main single stage amplifiers topolgies

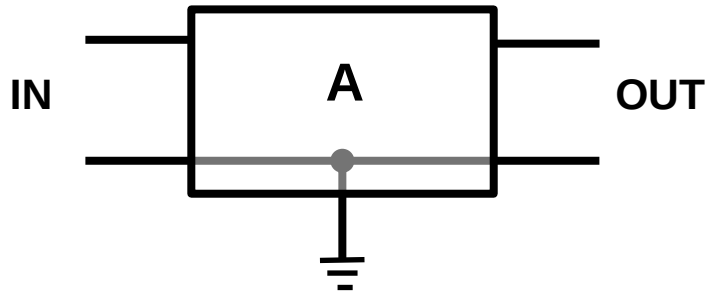
Common-Source Stage	Source Follower	Common-Gate Stage	Cascode
With Resistive Load	With Resistive Bias	With Resistive Load	Telescopic
With Diode-Connected Load	With Current-Source Bias	With Current-Source Load	Folded
With Current-Source Load			
With Active Load			
With Source Degeneration			

For these amplifiers, we must:

(1) set up proper bias conditions so that each transistor provides the necessary transconductance and output resistance with certain quiescent currents and voltages,

(2) analyze the circuit's behavior as the input and output signals cause small or large departures from the bias input (small-signal and large-signal analyses, respectively).

Two port network parameters
(example: voltage amplifier)

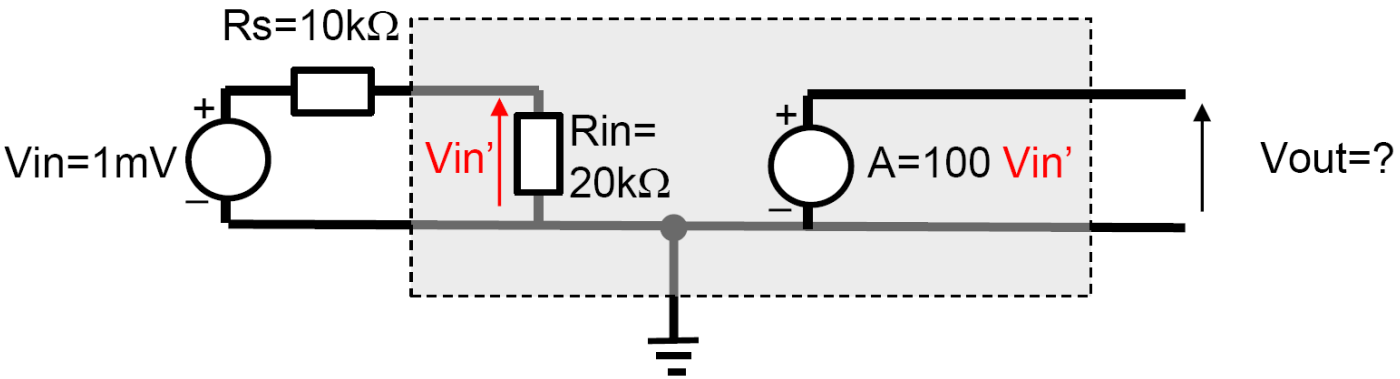


Ex. 1: Vin = 1 mV, A=100 V/V. Calculate Vout=?

Vout = 1 mV × 100V/V = 100 mV

Comment: if Rin=∞, and Rout =0)

Ex. 2: As above, but source resistance Rs=10kΩ, and amplifier Rin=20kΩ,

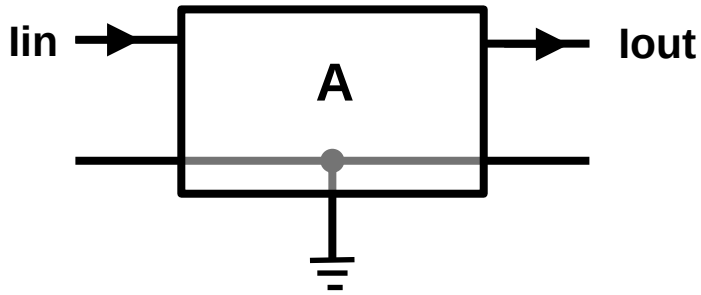


Vout = 1 mV × (voltage divider at input) × 100V/V

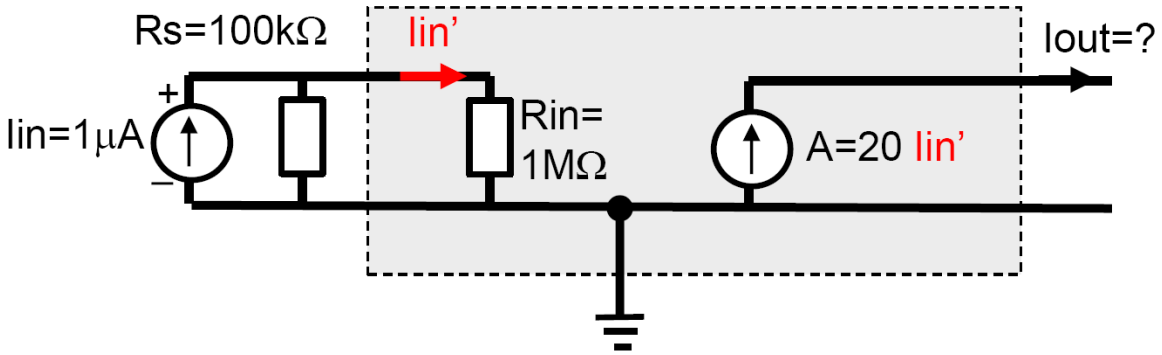
Vout = 1 mV × (20k/(10k+20k)) × 100V/V = 66 mV

Comment: It will be better if e.g. Rin = 1MΩ (for voltage amplifier Rin should be high)

Two port network parameters
(example: current amplifier)



Ex. 3: Iin = 1 μA, A=20 A/A, Rs= 100kΩ, Rin=1MΩ.
Calculate Iout=?



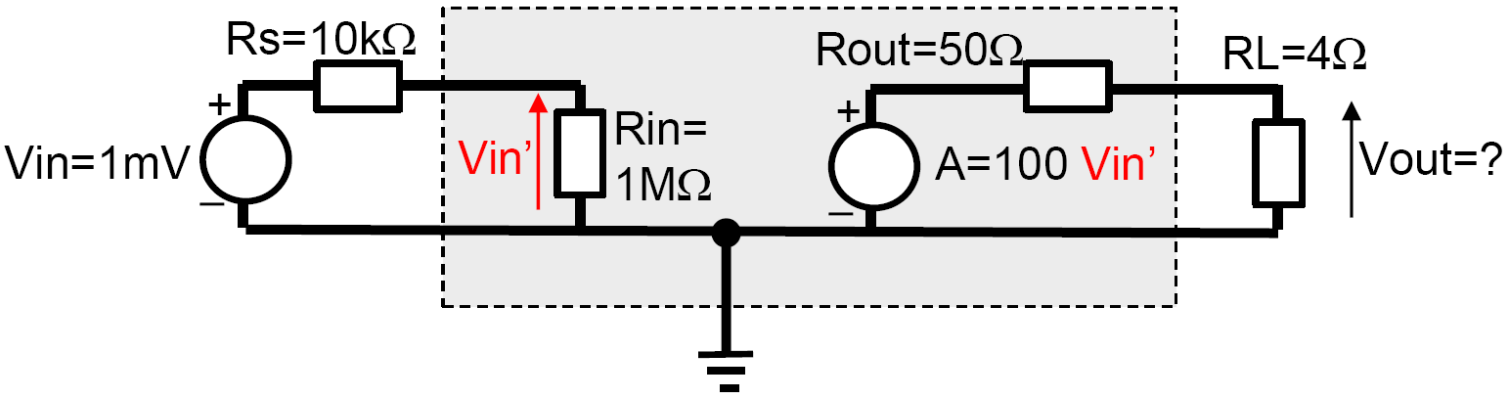
Iout = 1 μA × (current divider at input) × 20A/A

Iout = 1 μA × (100k/(100k+1M)) × 20A/A = 1.8 μA

Comment: It is better if Rin is small (for current amplifier Rin should be small)

Two port network parameters
(example: voltage amplifier with Rout)

Ex. 3: Vin = 1 mV, A=100 V/V, Rs=10kΩ, Rin=1MΩ, Rout=50Ω, RL=4Ω. Calculate Vout=?



Vout = 1 mV × (voltage divider at input) × 100V/V × (voltage divider at output)

Vout = 1 mV × (1M/(10k+1M)) × 100V/V × (4/(4+50)) = 7.4m

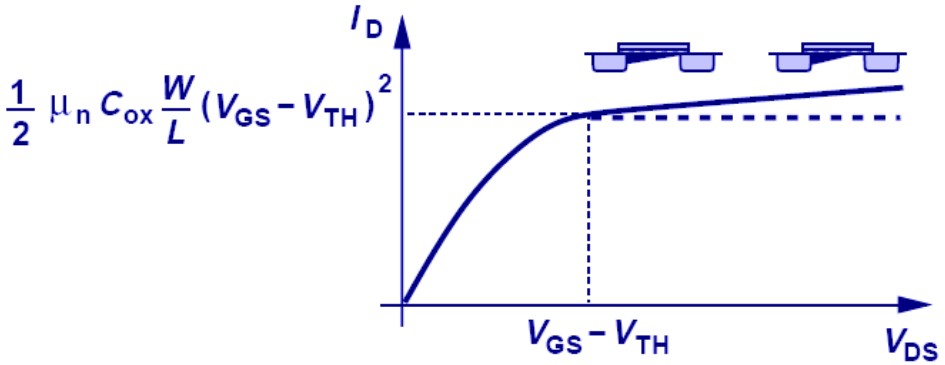
Comment: It will be better if Rout is small (for voltage amplifier Rout should be small)

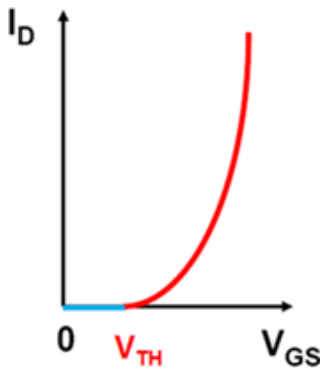
Conclusions:

- for amplifier not only gain, but also Zin and Zout are important,
- preference for Zin, Zout vaule depends on amplifier type (voltage, current, transimpedance, etc)
- other important parameter: power consumption, speed,noise, linearity, etc

MOS transistor models

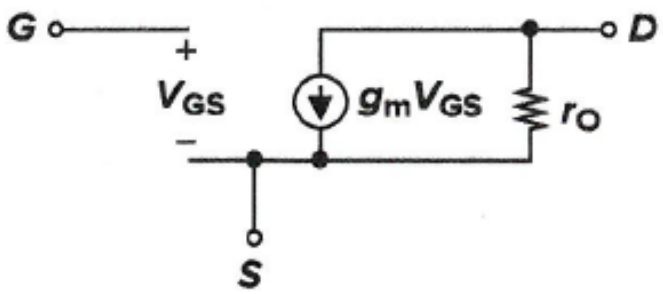
Large signal model





$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

Small signal model

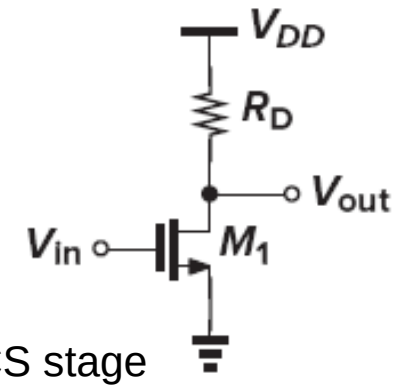


$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}$$

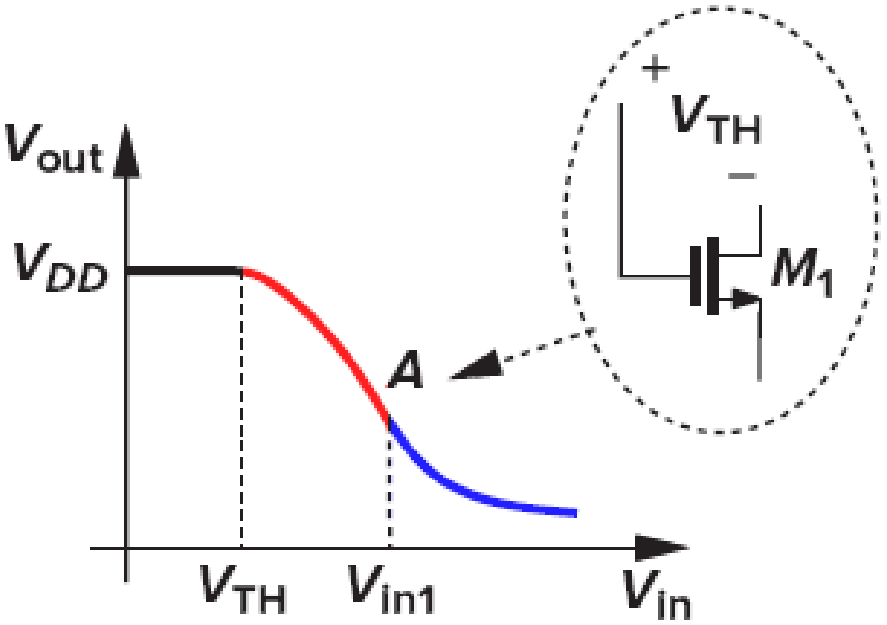
$$r_O \approx \frac{1}{\lambda I_D}$$

Common source with resistive load - description

By virtue of its transconductance, a MOSFET converts changes in its gate-source voltage to a small-signal drain current, which can pass through a resistor to generate an output voltage.



CS stage

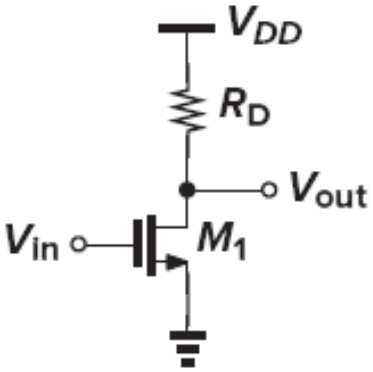


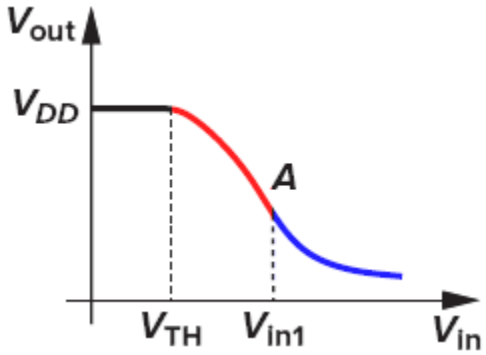
Input- output characteristics
(off – saturation - triode)

Saturation for $V_{DS} > V_{GS} - V_{TH} \Leftrightarrow V_{GS} < V_{DS} + V_{TH}$
Triode for for $V_{DS} < V_{GS} - V_{TH} \Leftrightarrow V_{GS} > V_{DS} + V_{TH}$

1) If the input voltage increases from zero, M1 is off and *Vout = VDD.*
2) As *Vin* approaches *VTH*, M1 begins to turn on, drawing current from *RD* and lowering *Vout* . Transistor M1 turns on in saturation
3) With further increase in Vin, Vout drops more, and the transistor continues to operate in saturation until Vin exceeds Vout by VTH [point A in Fig.].
4) For Vin > Vin1, M1 is in the triode region.

Common source with resistive load – large signal model





Gain calculation:

$$A_v = \frac{\partial V_{out}}{\partial V_{in}}$$
$$= -R_D \mu_n C_{ox} \frac{W}{L}(V_{in} - V_{TH})$$
$$= -g_m R_D$$

$V_{out} = V_{DD} - R_D I_D$

In saturation (channel- length modulation is neglected)

$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L}(V_{in} - V_{TH})^2$$

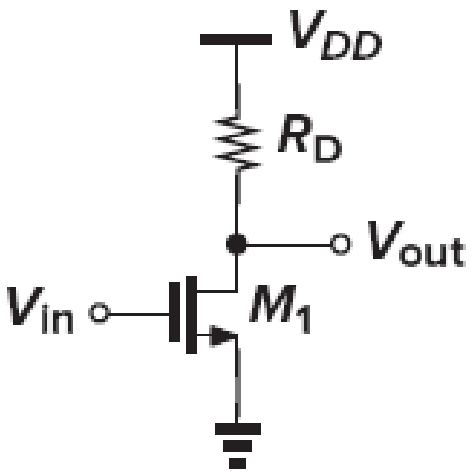
To increase the gain A_v: increase g_m or R_D

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

Homework: common source with resistive load – large signal model (with channel length modulation)

In saturation (channel- length modulation)

$$V_{out} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})^2(1 + \lambda V_{out})$$



HOMEWORK: calculate the gain:

$$\frac{\partial V_{out}}{\partial V_{in}} = -R_D\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})(1 + \lambda V_{out})$$
$$-R_D\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})^2\lambda\frac{\partial V_{out}}{\partial V_{in}}$$

We recognize that:

$$(1/2)\mu_n C_{ox}(W/L)(V_{in} - V_{TH})^2\lambda = 1/r_O$$

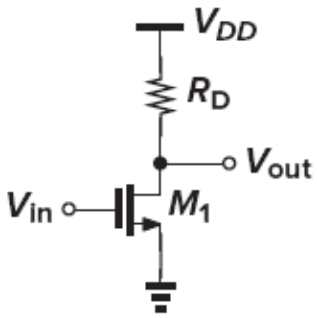
and:

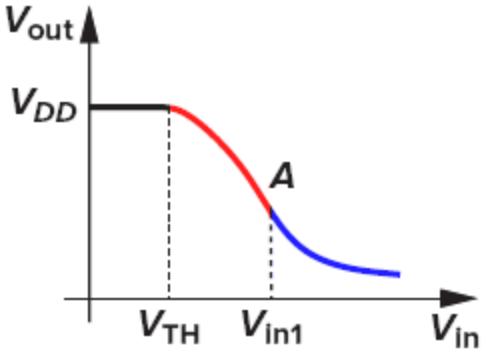
$$A_v = -R_D g_m - \frac{R_D}{r_O}A_v$$

$$A_v = -g_m\frac{r_O R_D}{r_O + R_D}$$

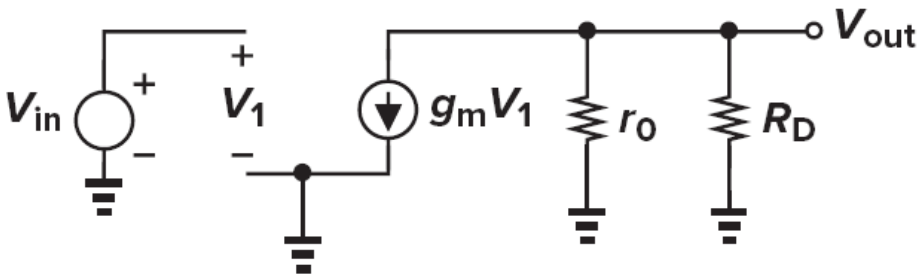
To increase the gain A_v: increase g_m or R_D

Common source with resistive load – small signal model (saturation, channel lenght-modulation included)





Input- output characteristics (off – saturation - triode)



Small signal model including output resistance (saturation)

$$g_m V_1 (r_O \| R_D) = -V_{out}$$

$$V_1 = V_{in}$$

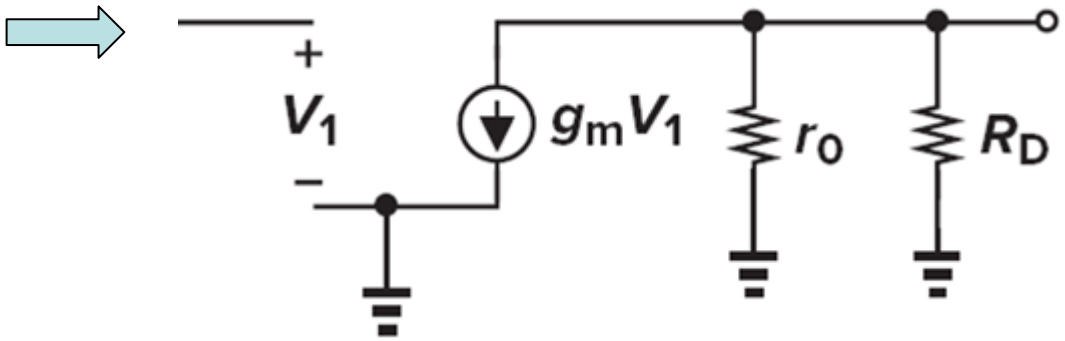
$$V_{out} / V_{in} = -g_m (r_O \| R_D)$$

The small-signal model of Fig. gives the same result with much less effort.

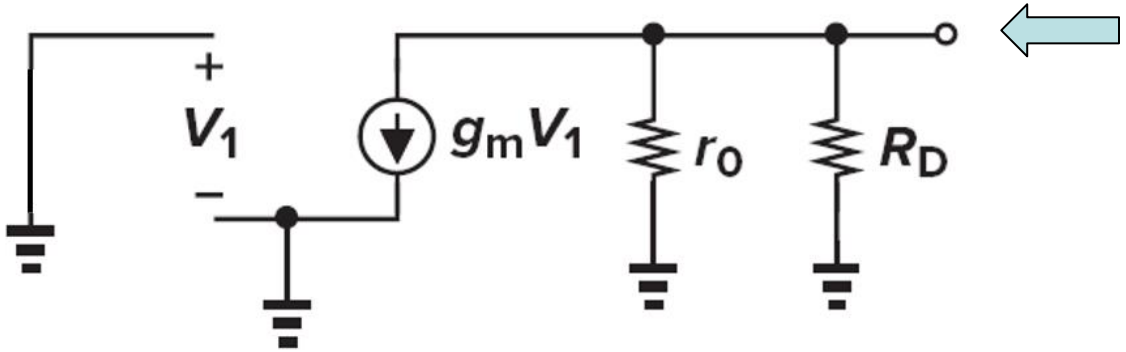
Common source with resistive load – output/input resistance

Intput resistance:

$r_{in} = \infty$



Output resistance: signal source at the input we replace by its output resistance (ideal voltage source – resistance equal to zero)

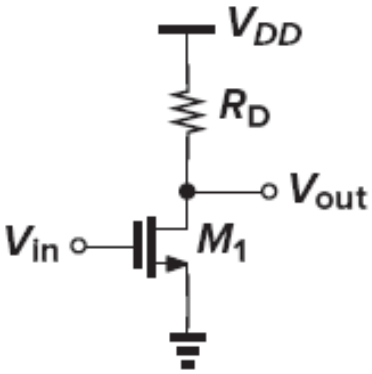


$r_{out} = r_o \text{ II } R_D$

Calculation at low frequency (at higher frequency capacitance must be taken into account)

Where is the gain limit?

Example:
I_D=0.5mA, μC_{ox} =100μA/V^2, W/L=10, λ=0.1V $^{-1}$

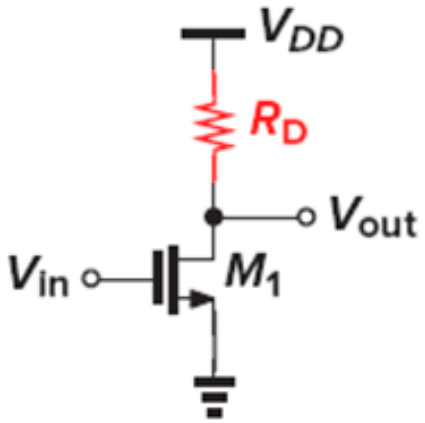


Calculation:
g_m=1mA/V, r_o =20kΩ

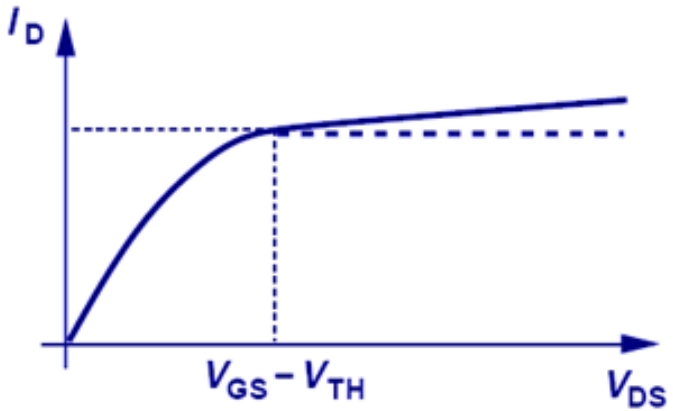
Assume output voltage at $V_{DD}/2$ for max. output linearity. Calculate R_D and gain for V_{DD}=5V and V_{DD}=2V.

Case with V_{DD}=5V:
$R_D = V_{DD}/2I_D$= 5kΩ and $A_v \approx - g_m R_D$= - 5V/V

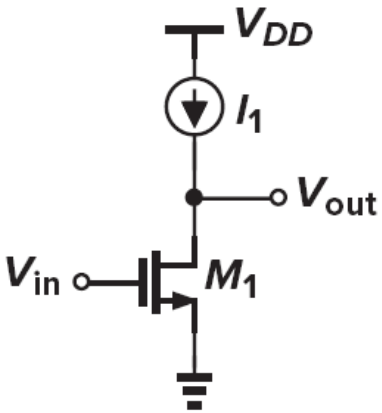
Case with V_{DD}=2V:
$R_D = V_{DD}/2I_D$= 2kΩ and $A_v \approx - g_m R_D$= - 2V/V

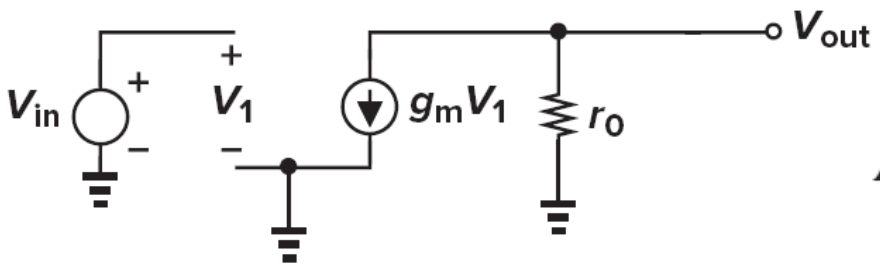


Limit in R: exchange to another element with
- less DC voltage drop
- higher AC resistance



Common source with currrent source load





$$A_v = -g_m r_O$$

Intristic transistor gain: $A_v = -g_m r_O$

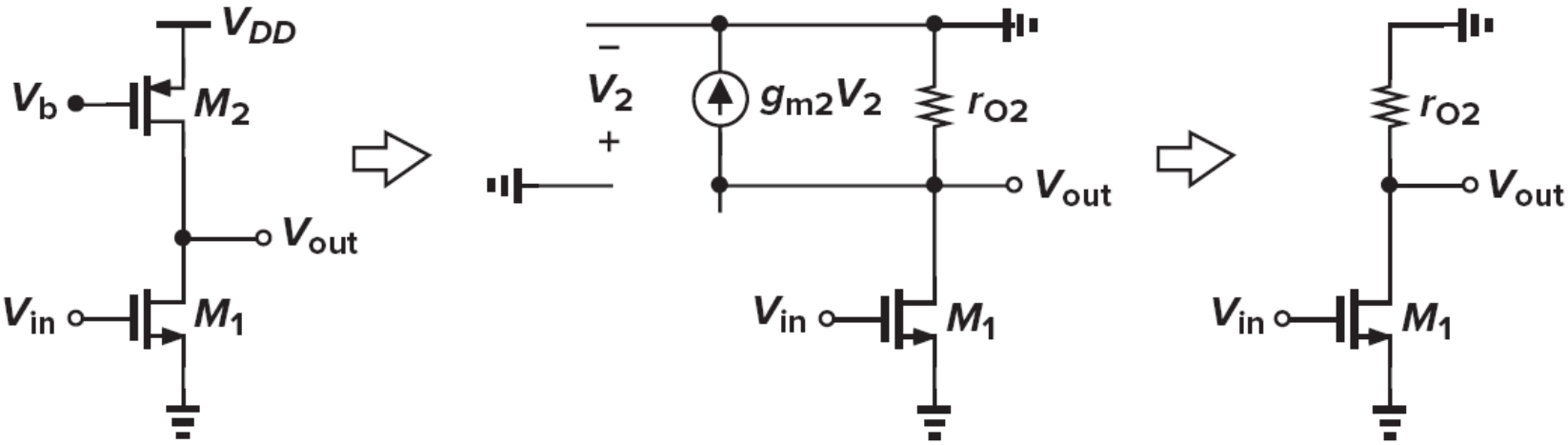
- CMOS technology: 10-30
- for the newest technology: 3-5

To increase the gain: $g_m\uparrow$ and $r_o\uparrow$:

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_D} \qquad r_O \approx \frac{1}{\lambda I_D}$$

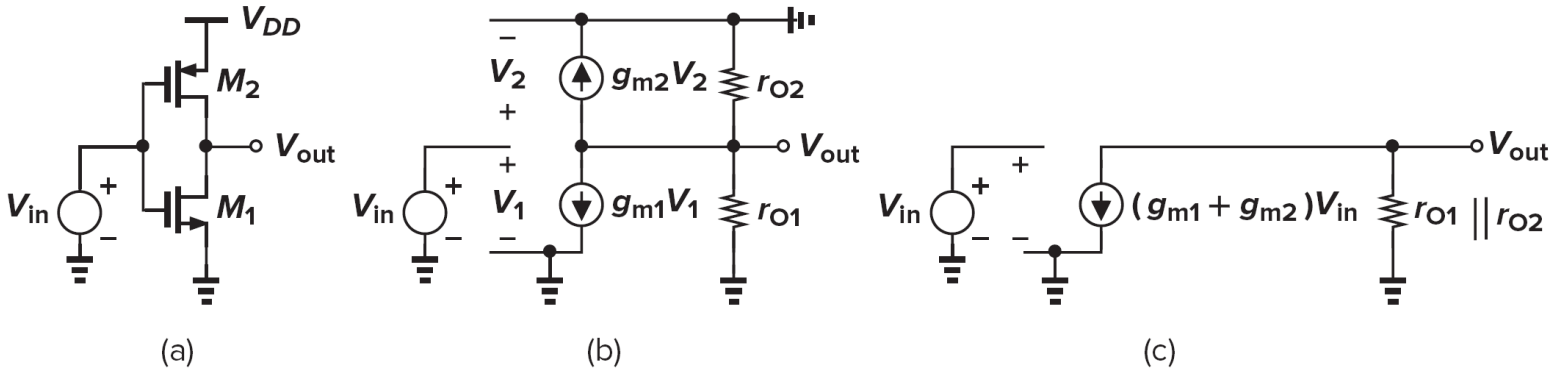
Remember the are other important parameters of amplifier, like gain, noise, etc.

Common source with currrent source load (based on transistor operating in saturation)



$$A_v = -g_{m1}(r_{O1} \| r_{O2})$$

Common source with active load



(a) CS stage with active load, (b) small-signal model, and (c) simplified model.

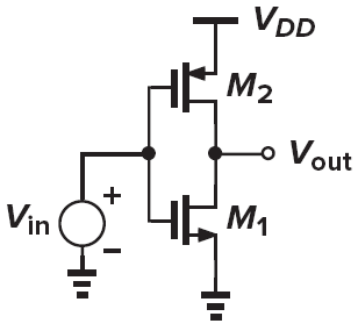
$$A_v = -(g_{m1} + g_{m2})(r_{O1}||r_{O2})$$

Compared to the amplifier with current source load, this circuit exhibits the same output resistance, $r_{O1}||r_{O2}$, but a higher transconductance. This topology is also called a "complementary CS stage."

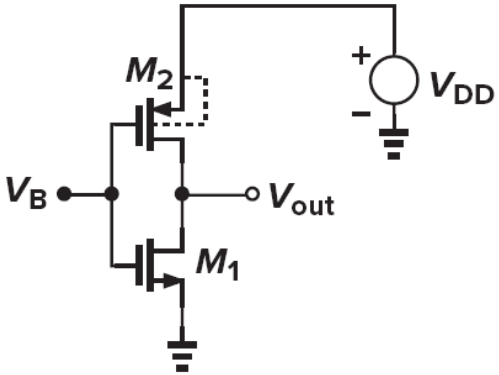
The amplifier of Fig. must deal with two critical issues:

1) The bias current of the two transistors is a strong function of PVT (proces-voltage-temperature). In particular, since $V_{GS1} + |V_{GS2}| = V_{DD}$, variations in V_{DD} or the threshold voltages directly translate to changes in the drain currents.
2) The circuit *amplifies* supply voltage variations ("supply noise")!

Common source with active load (Homework: problem with supply noise!)



CS stage with active load.

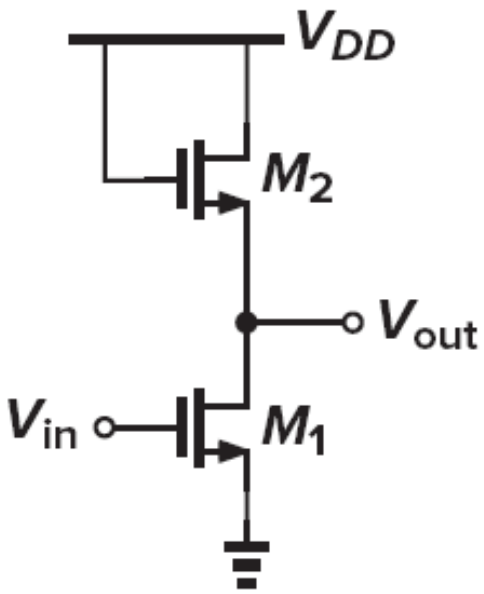


Arrangement for studying supply sensitivity of CS stage with active load.

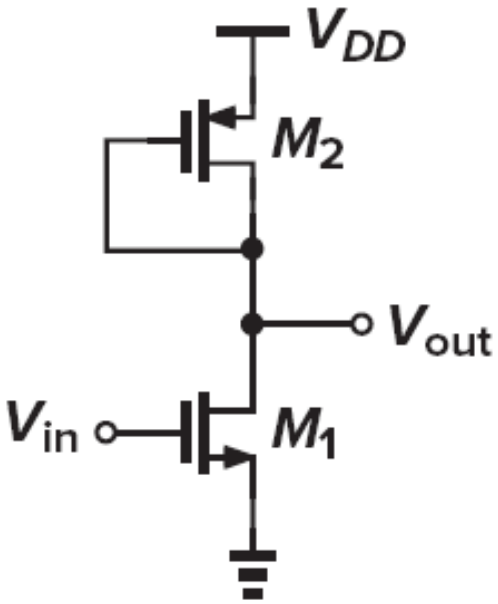
$$\frac{V_{out}}{V_{DD}} = \frac{g_{m2}r_{O2}+1}{r_{O2}+r_{O1}} r_{O1}$$

$$= \left(g_{m2} + \frac{1}{r_{O2}}\right)(r_{O1} \| r_{O2})$$

Common source with diode connected load



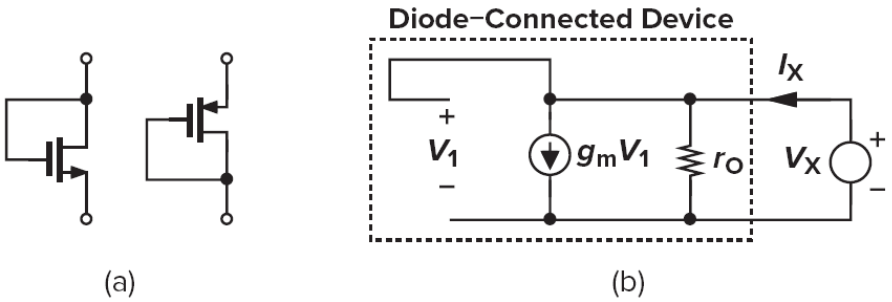
CS stage with diode connected NMOS device.



CS stage with diode connected PMOS device.

Diode connected load

For $V_{SB}=0$



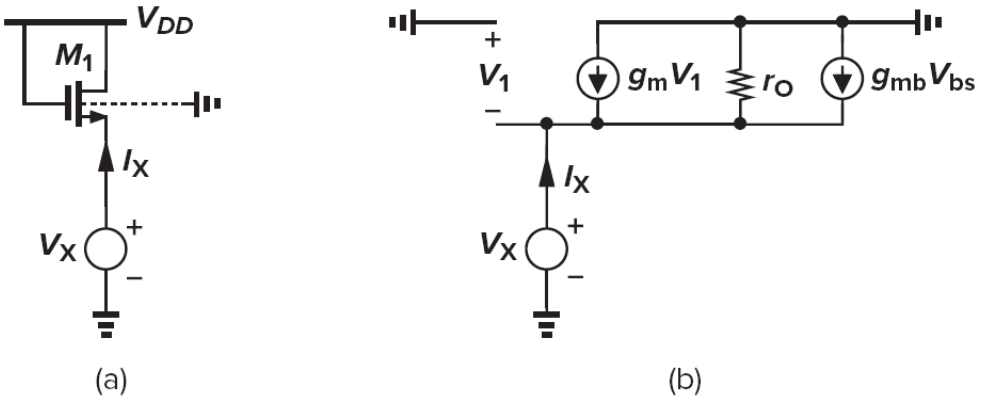
(a) Diode-connected NMOS and PMOS devices; (b) small-signal equivalent circuit.

$$V_1 = V_X$$

$$I_X = V_X/r_O + g_m V_X$$

$$V_X/I_X = (1/g_m)\|r_O \approx 1/g_m$$

HOMEWORK: for $V_{SB}\neq 0$



$$V_1 = -V_X,\ V_{bs} = -V_X$$

$$(g_m + g_{mb})V_X + \frac{V_X}{r_O} = I_X$$

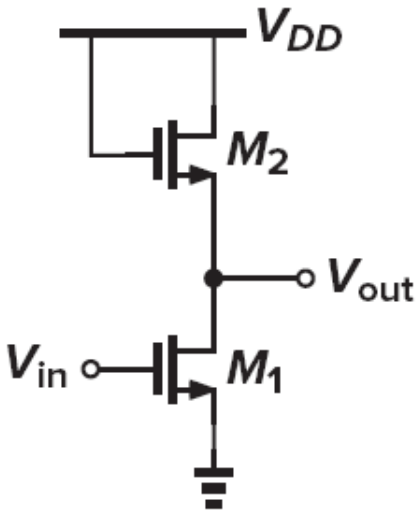
$$\frac{V_X}{I_X} = \frac{1}{g_m + g_{mb} + r_O^{-1}}$$

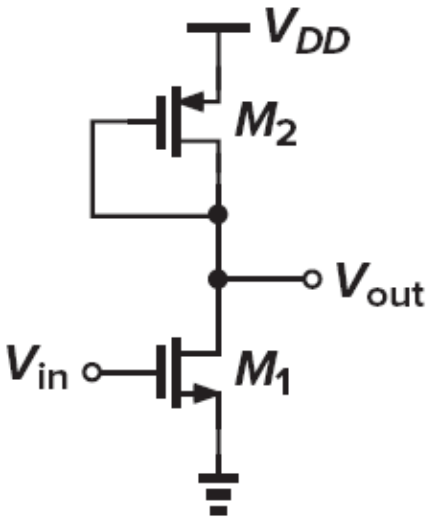
$$= \frac{1}{g_m + g_{mb}}\|r_O$$

$$\approx \frac{1}{g_m + g_{mb}}$$

(a) Arrangement for measuring the equivalent resistance of a diode-connected MOSFET; (b) small-signal equivalent circuit.

Common source with diode connected load





$$A_v = -g_{m1}\frac{1}{g_{m2} + g_{mb2}}$$

$$A_v = -\frac{g_{m1}}{g_{m2}}$$

Common source with diode connected load (Homework: example)

▶ **Example 3.6**

In the circuit of Fig. 3.17, M_1 is biased in saturation with a drain current equal to I_1. The current source $I_S = 0.75I_1$ is added to the circuit. How is (3.37) modified for this case? Assume $\lambda = 0$.

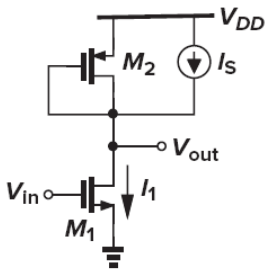


Figure 3.17

Solution

Since $|I_{D2}| = I_1/4$, we have

$$A_v = -\frac{g_{m1}}{g_{m2}} \tag{3.40}$$

$$= -\sqrt{\frac{4\mu_n(W/L)_1}{\mu_p(W/L)_2}} \tag{3.41}$$

Moreover,

$$\mu_n \left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH1})^2 = 4\mu_p \left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH2})^2 \tag{3.42}$$

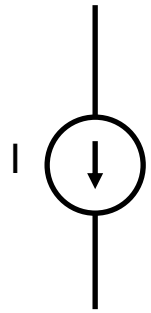
yielding

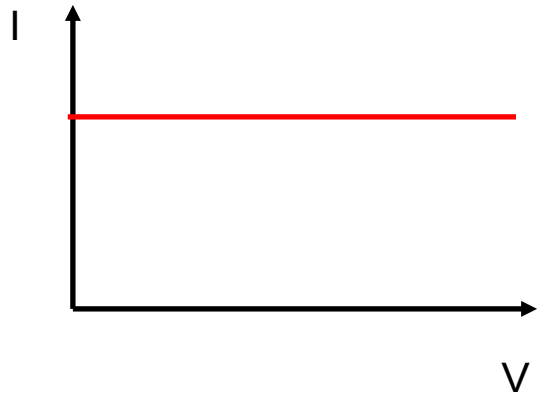
$$\frac{|V_{GS2} - V_{TH2}|}{V_{GS1} - V_{TH1}} = \frac{A_v}{4} \tag{3.43}$$

Thus, for a gain of 5, the overdrive of M_2 need be only 1.25 times that of M_1. Alternatively, for a given overdrive voltage, this circuit achieves a gain four times that of the stage in Fig. 3.16. Intuitively, this is because for a given $|V_{GS2} - V_{TH2}|$, if the current decreases by a factor of 4, then $(W/L)_2$ must decrease proportionally, and $g_{m2} = \sqrt{2\mu_p C_{ox}(W/L)_2 I_{D2}}$ is lowered by the same factor.

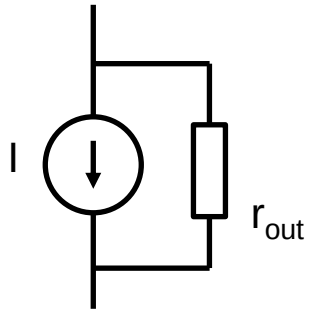
Current source

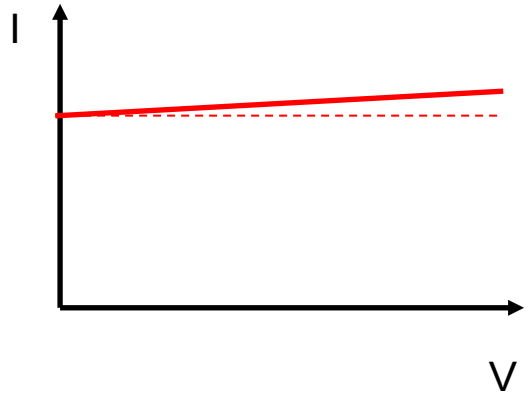
Ideal current source





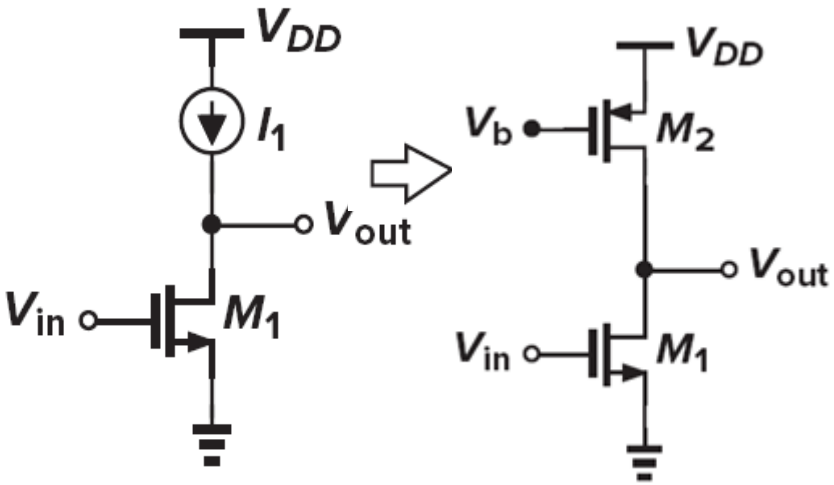
Current source has output resistance



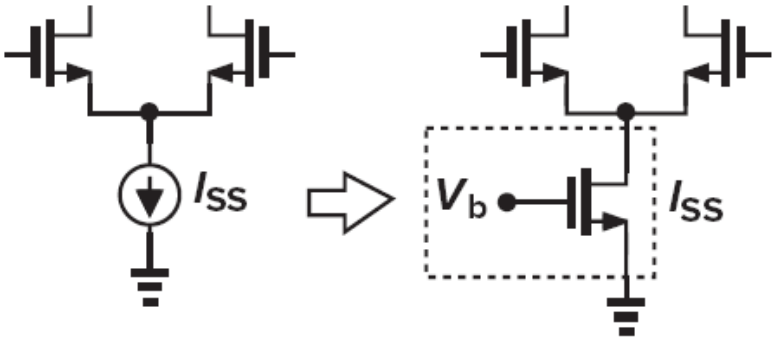


Current source - applications

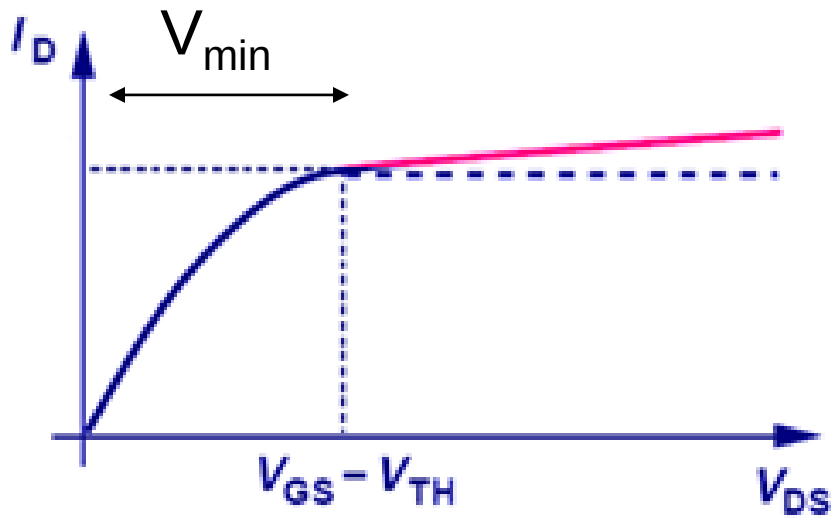
Active load



Biasing circuits

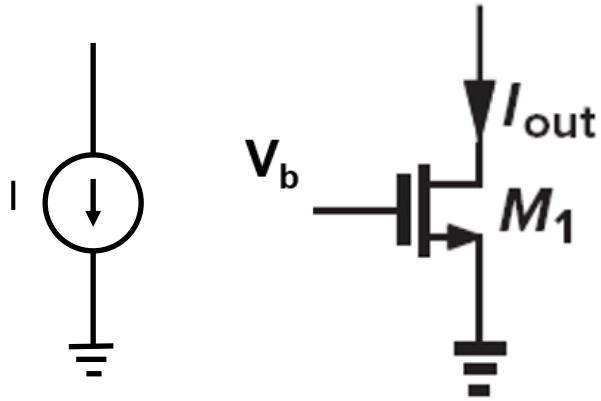


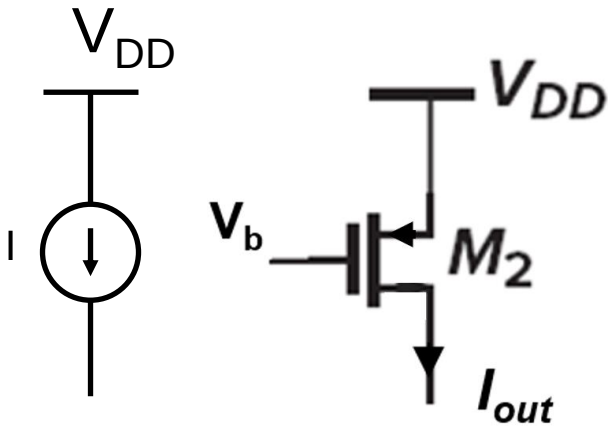
Current source – based on transistor in saturation



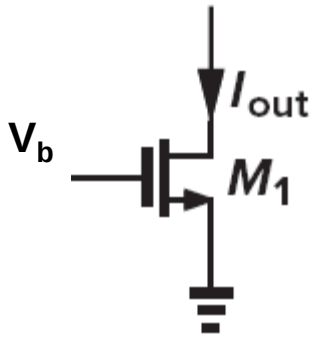
Good curent source:

1) $r_o \uparrow$
2) $V_{min} \downarrow$

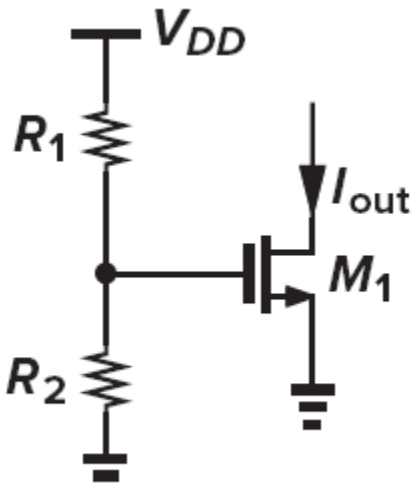




Current source: looking for proper bias



Resistive devider

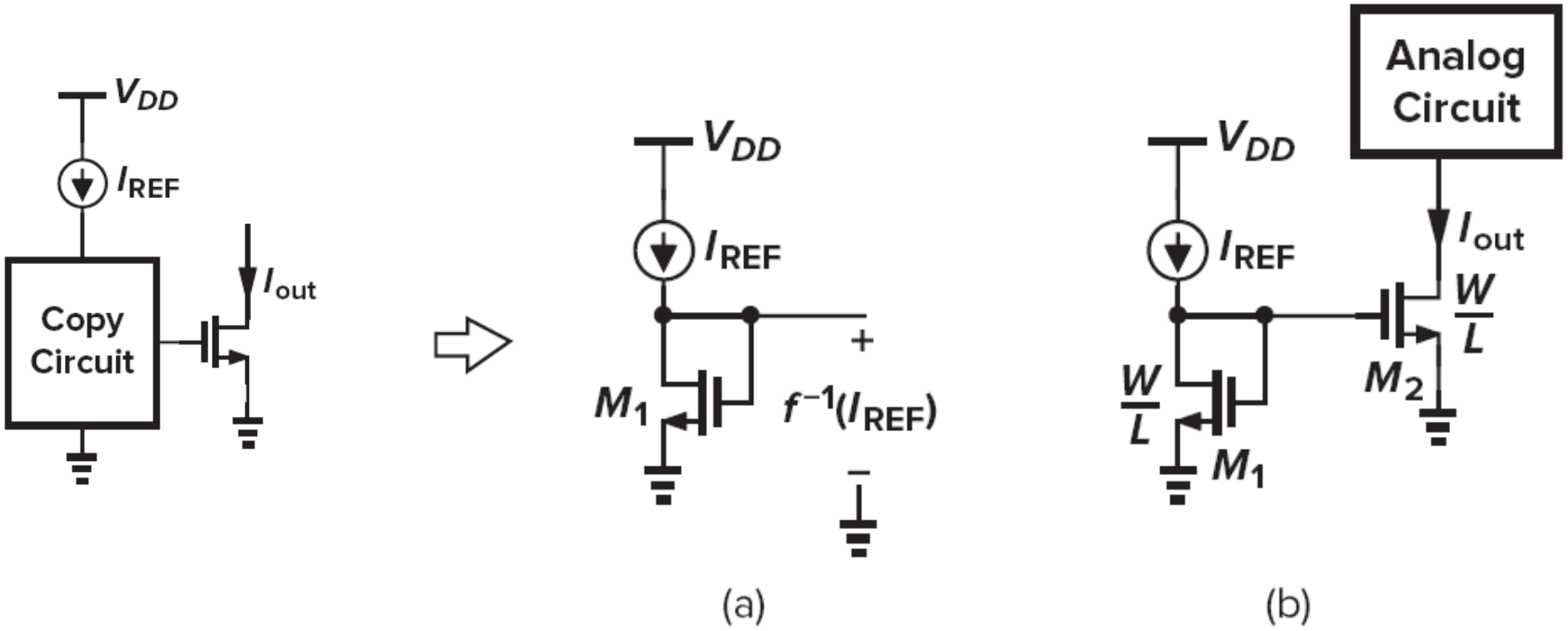


$$I_{out} \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_2}{R_1+R_2}V_{DD}-V_{TH}\right)^2$$

This expression reveals various PVT dependencies of I_{out}. The overdrive voltage is a function of V_{DD} and V_{TH}; the threshold voltage may vary by 50 to 100 mV from wafer to wafer. Furthermore, both μ_n and V_{TH} exhibit temperature dependence. Thus, I_{out} is poorly defined. The issue becomes more severe as the device is biased with a smaller overdrive voltage, e.g., to consume less headroom and support greater voltage swings at the drain. With a nominal overdrive of, say, 200 mV, a 50-mV error in V_{TH} results in a 44% error in the output current.

It is important to note that process and temperature dependencies exist even if the gate voltage is not a function of the supply voltage. In other words, if the gate-source *voltage* of a MOSFET is precisely defined, then its drain *current* is not! For this reason, we must seek other methods of biasing MOS current sources.

How to generate copies of current source



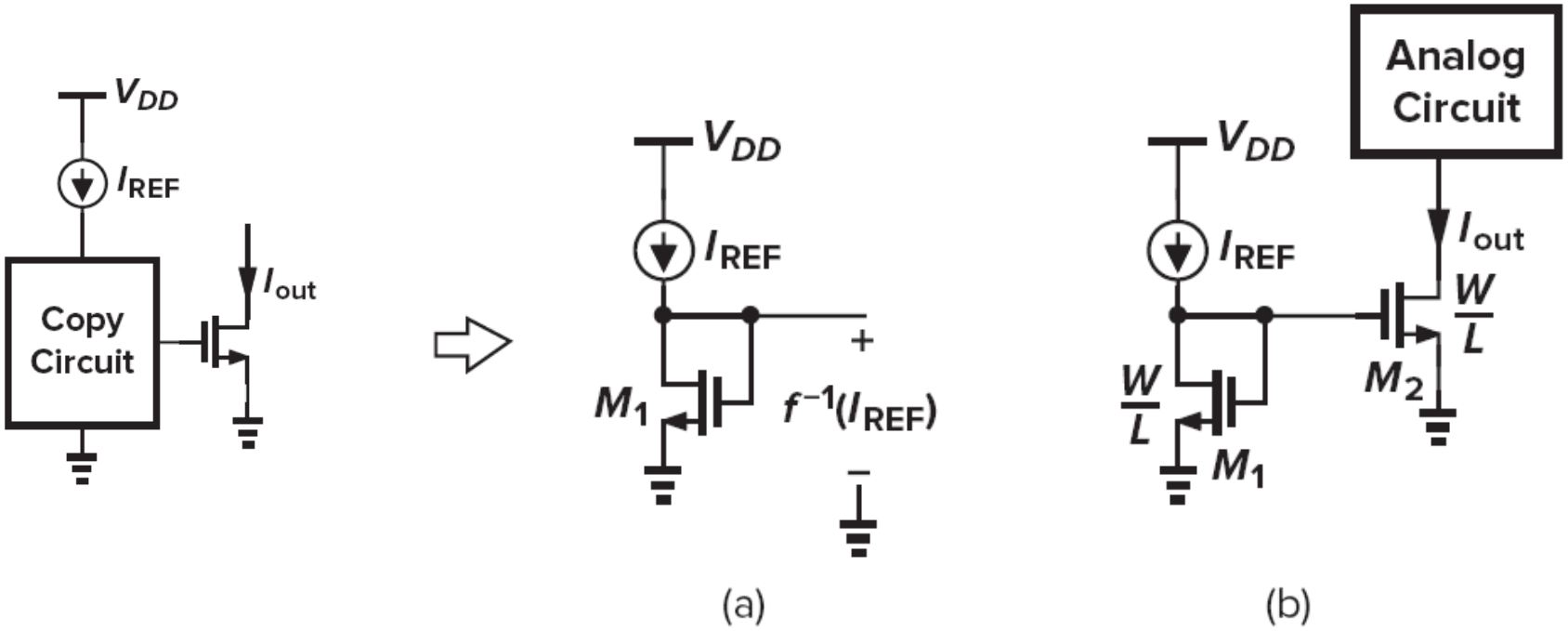
(a) Diode-connected device providing inverse function; (b) basic current mirror.

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2$$

$$\Rightarrow \quad I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}$$

How to generate copies of current source



(a) Diode-connected device providing inverse function; (b) basic current mirror.

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$$\Rightarrow \quad I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}$$

Multiply current

Current mirrors usually employ the same *length* for all of the transistors so as to minimize errors due to the side-diffusion of the source and drain areas (L_D). For example, in Fig. (a), the NMOS current sources must have the same channel length as $M0$. This is because if L_{drawn} is, say, doubled, then $L_{eff} = L_{drawn} - 2L_D$ is not. Furthermore, the threshold voltage of short-channel devices exhibits some dependence on the channel length. Thus, current ratioing is achieved by scaling only the width of the transistors.

Suppose we wish to copy a reference current, I_{REF}, and generate $2I_{REF}$. We begin with a width of W_{REF} for the diode-connected reference transistor and hence choose $2W_{REF}$ for the current source [Fig. (a)]. Unfortunately, direct scaling of the width also faces difficulties. As illustrated in Fig. (b), since the "corners" of the gate are poorly defined, if the drawn W is doubled, the actual width does not exactly double. We thus prefer to employ a "unit" transistor and create copies by *repeating* such a device [Fig. (c)].

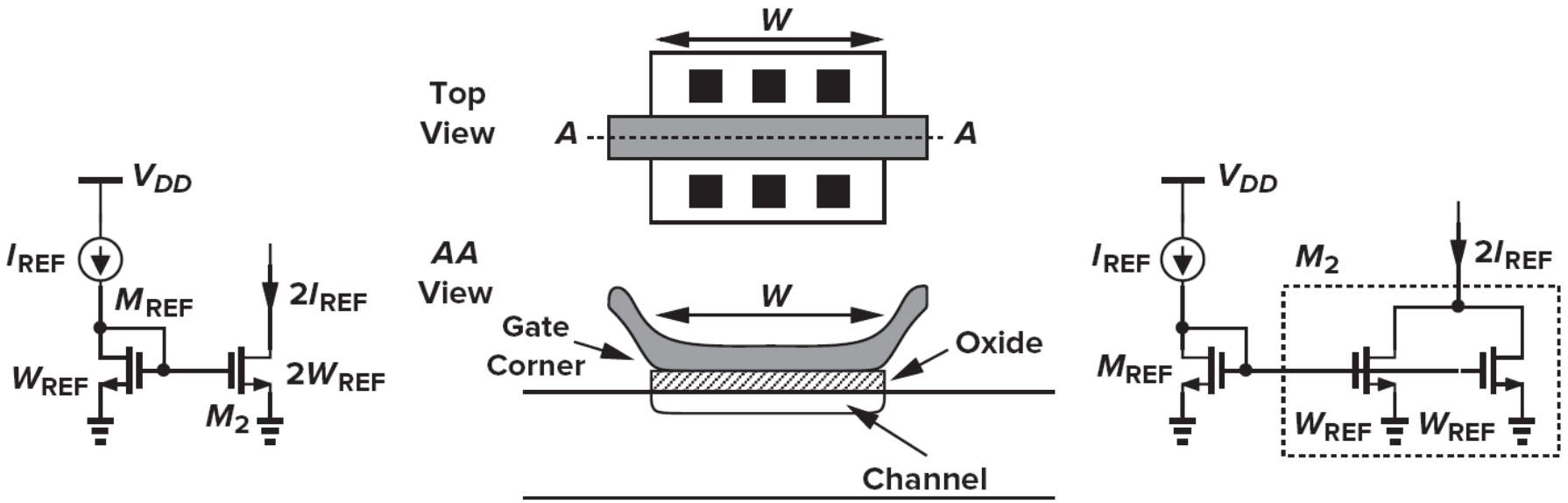


Figure (a) Current mirror multiplying I_{REF} by 2, (b) effect of gate corner on current accuracy, and (c) more accurate current multiplication.

Multiply current

But how do we generate a current equal to $I_{REF}/2$ from I_{REF}? In this case, the diode-connected device itself must consist of *two* units, each carrying $I_{REF}/2$. Figure (a) depicts an example for the generation of both $2I_{REF}$ and $I_{REF}/2$; each unit has a width of $W0$ (and the same length).

The above approach requires a large number of unit transistors if many different currents must be generated. It is possible to reduce the complexity by scaling the lengths, but not directly. In order to avoid the errors due to L_D, we can, for example, double the equivalent length by placing two unit transistors in series. Illustrated in Fig. (b), this approach preserves an effective length of $L_{drawn}-2L_D$ for each unit, yielding an equivalent length of $2(L_{drawn} - 2L_D)$ for the composite device and hence halving the current. Note that this structure is not a cascode because the bottom device is in the triode region.

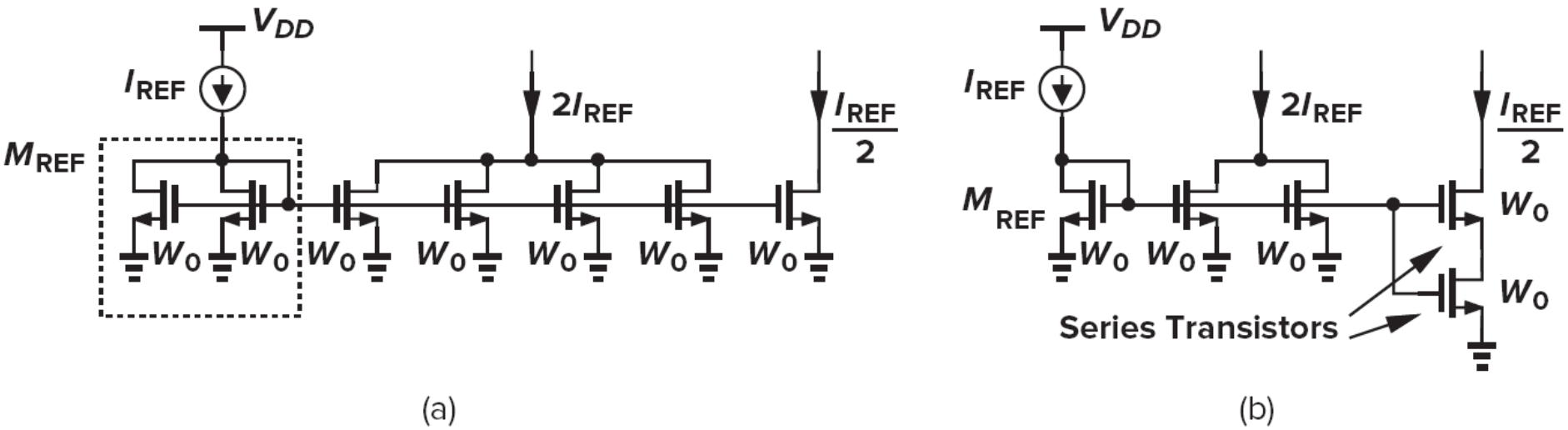
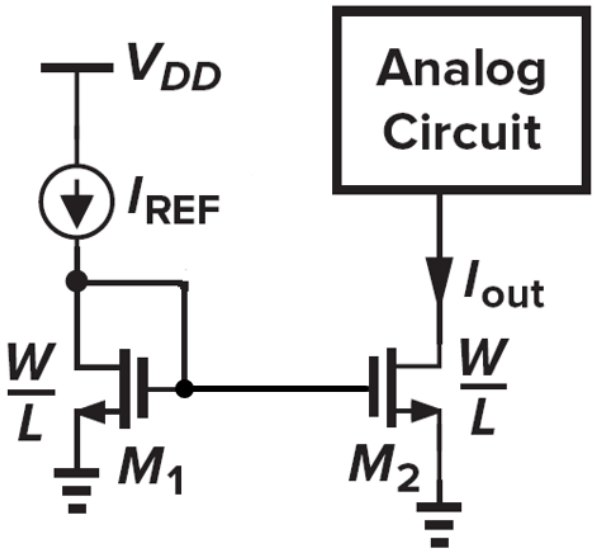
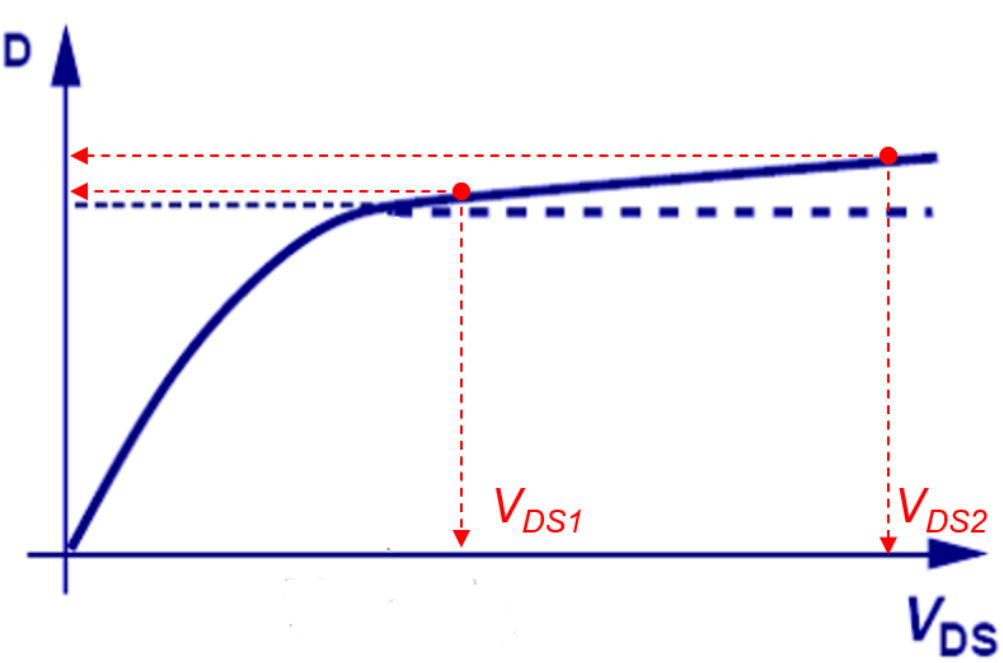


Figure Current mirrors providing $I_{REF}/2$ from I_{REF} by (a) half-width device and (b) series transistors.

Problem with single current mirror

Drawback: limited output resistance (it should be higher)





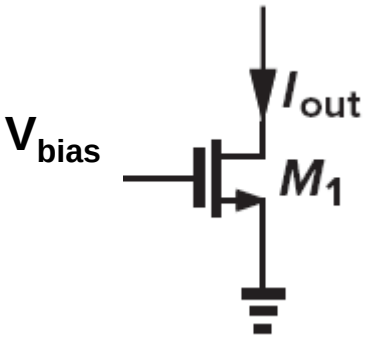
$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS1})$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS2})$$

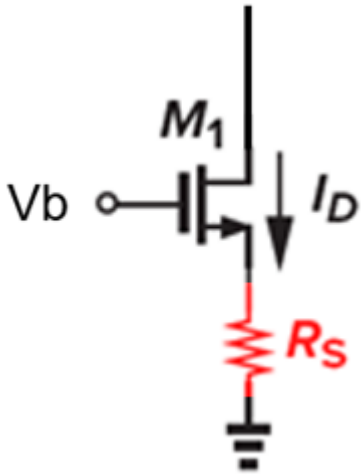
$$\Rightarrow \quad \frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$

Problem solutions: cascode current mirror.

Current source – how to increasing R_{out}



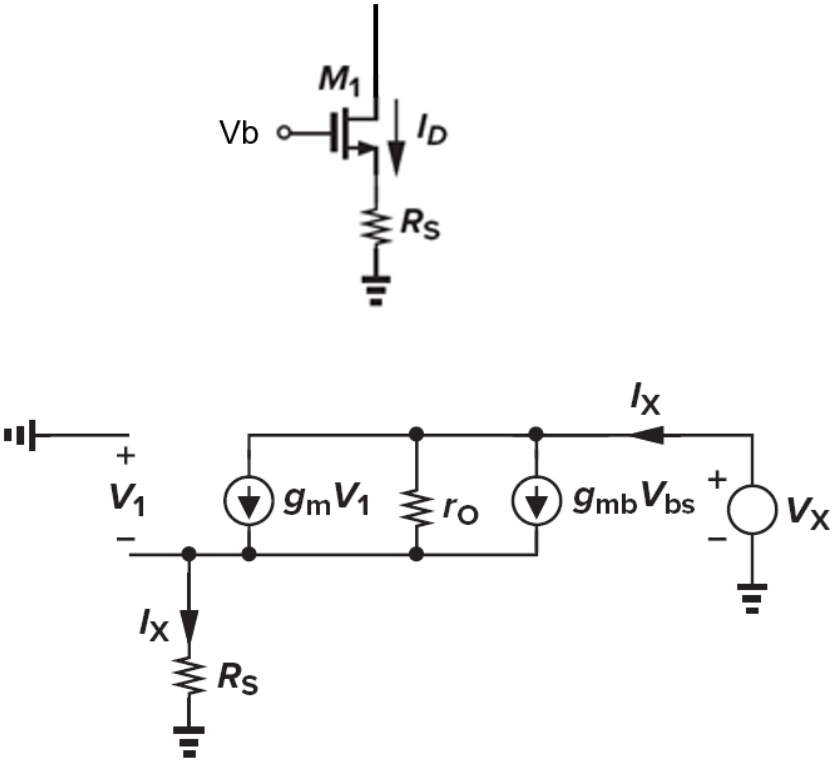
$R_{out} = r_O$



$R_{out} \approx g_m R_S \times r_O$

Cureent source with source degradation – R_{out}
(increasing the output resistance)

Important consequence of source degeneration is the increase in the output resistance of the stage. We calculate the output resistance first with the aid of the equivalent circuit shown in Fig. (below). Note that body effect is also included to arrive at a general result. Since the current through RS is equal to I_X , $V_1 = -I_X R_S$, and the current flowing through r_O is given by $I_X - (g_m + g_{mb})V_1 = I_X + (g_m + g_{mb})R_S I_X$. Adding the voltage drops across r_O and R_S, we obtain:



$$r_O[I_X + (g_m + g_{mb})R_S I_X] + I_X R_S = V_X$$

It follow that:

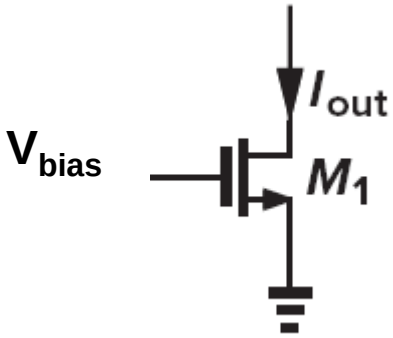
$$R_{out} = [1 + (g_m + g_{mb})R_S]r_O + R_S$$
$$= [1 + (g_m + g_{mb})r_O]R_S + r_O$$

Equation R_{out} indicates that r_O is "boosted" by a factor of $1 + (g_m + g_{mb})R_S$ and then added to R_S.

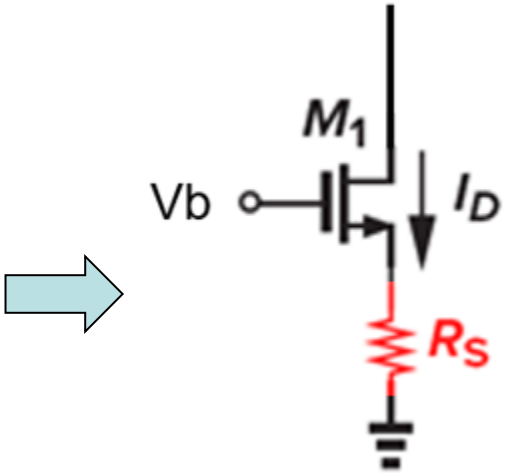
As an alternative perspective, eq. suggests that R_S is boosted by a factor of $1 + (g_m + g_{mb})r_O$ (a value close to the transistor's intrinsic gain) and then added to r_O.

Both views prove useful in analyzing circuits.

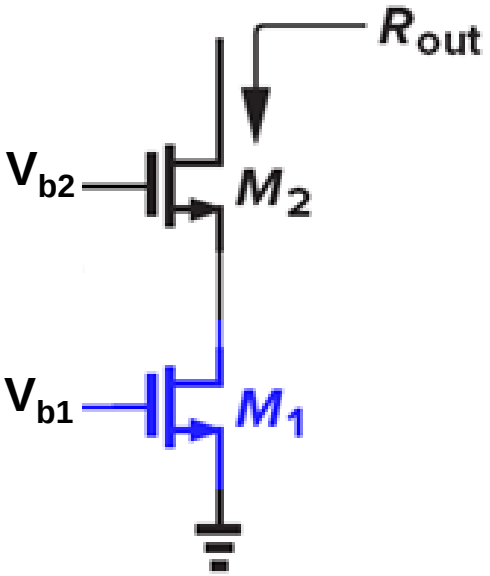
Current source – further increase R_{out}



$R_{out} = r_O$



$R_{out} \approx g_m r_O R_S$



$R_{out} \approx g_{m2} r_{O2} r_{O1}$

Cascode current source

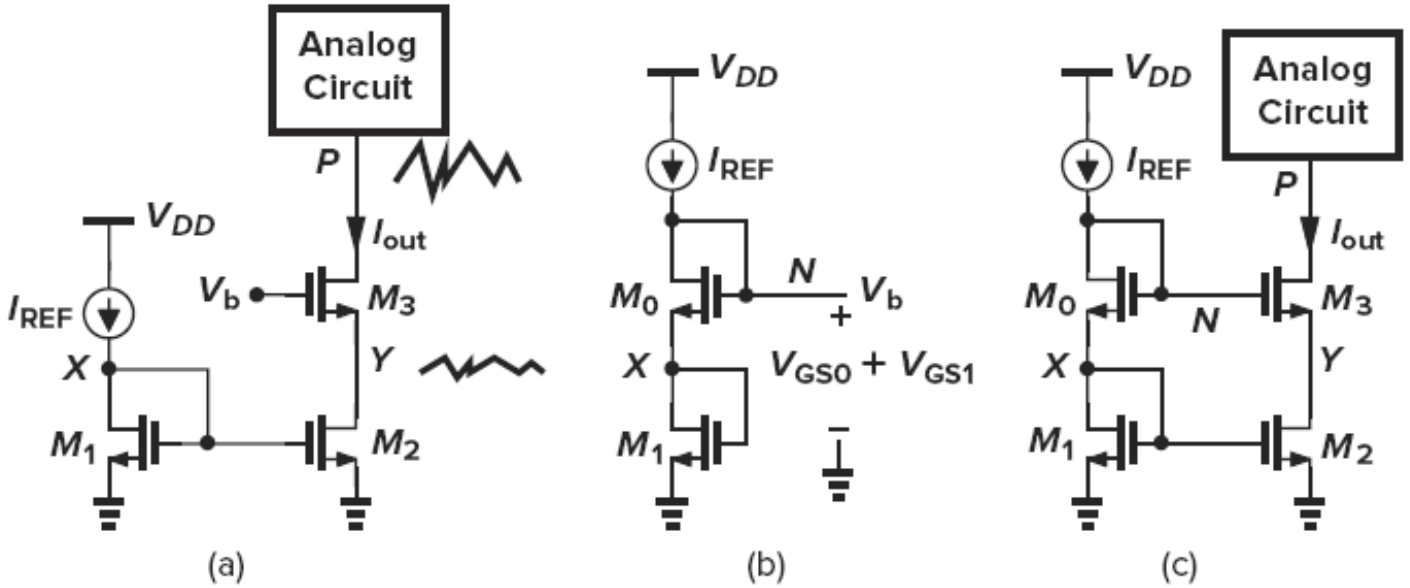


Figure 5.12 (a) Cascode current source, (b) modification of mirror circuit to generate the cascode bias voltage, and (c) cascode current mirror.

While operating as a current source with a high output impedance and accurate value, the topology of Fig. 5.12(c) nonetheless consumes substantial voltage headroom. For simplicity, let us neglect the body effect and assume that all of the transistors are identical. Then, the minimum allowable voltage at node P is equal to

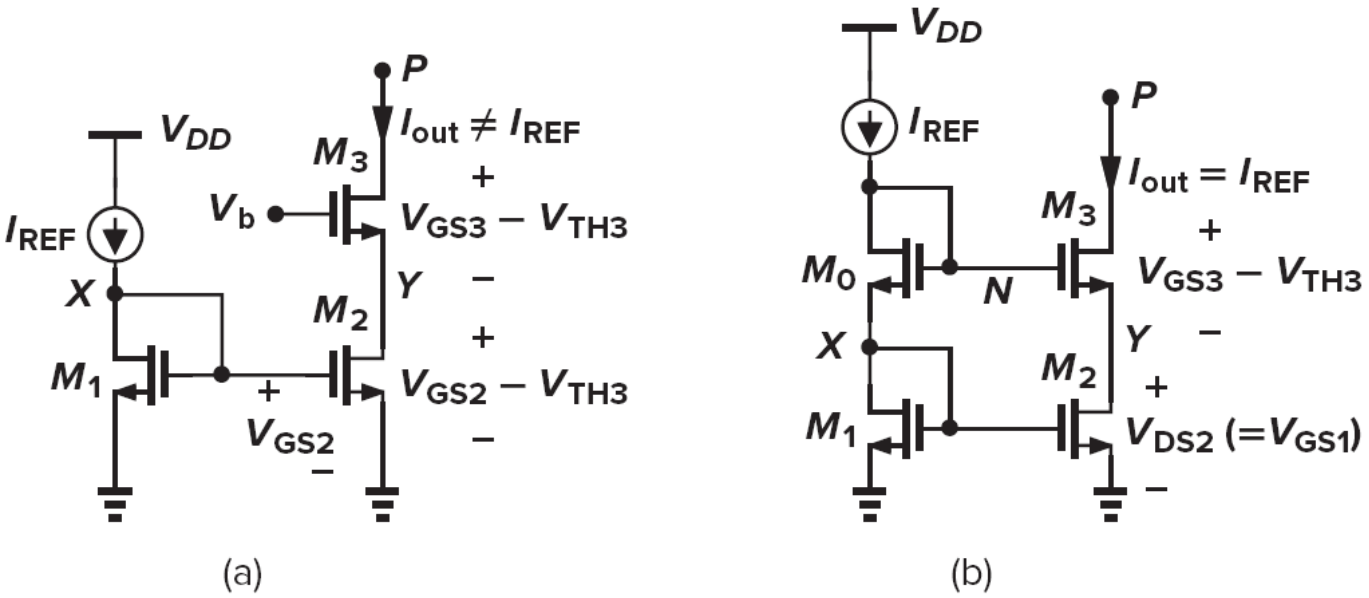
$$\begin{aligned} V_N - V_{TH} &= V_{GS0} + V_{GS1} - V_{TH} \\ &= (V_{GS0} - V_{TH}) + (V_{GS1} - V_{TH}) + V_{TH} \end{aligned}$$

i.e., two overdrive voltages plus one threshold voltage.

Cascode current source

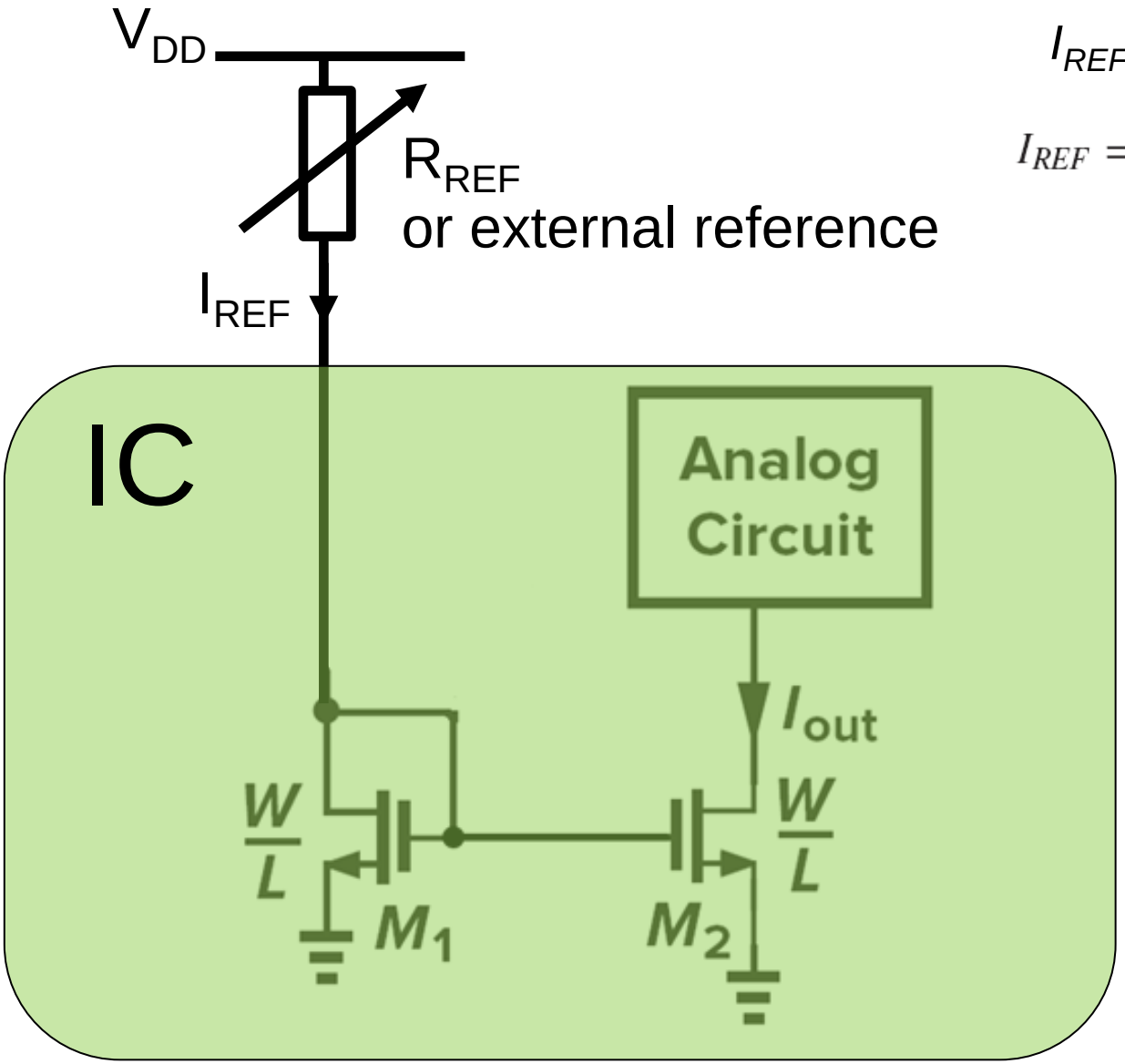
As shown in Fig. (a), *Vb* could be so low (= $V_{GS3} + V_{GS2} - V_{TH2}$) that the minimum allowable voltage at P is merely two overdrive voltages. Thus, the cascode mirror of Fig. (b) "wastes" one threshold voltage in the headroom. This is because $V_{DS2} = V_{GS2}$, whereas V_{DS2} could be as low as $V_{GS2} - V_{TH}$ while maintaining M2 in saturation.

Figure (below) summarizes our discussion. In Fig. (a), Vb is chosen to allow the lowest possible value of V_P , but the output current does not accurately track I_{REF} because M1 and M2 sustain unequal drain-source voltages. In Fig. (b), a higher accuracy is achieved, but the minimum level at P is higher by one threshold voltage.



(a) Cascode current source with minimum headroom voltage; (b) headroom consumed by a cascode mirror.

What to do if in IC we do not have a stable Iref



$$I_{REF}=(V_{DD}-V_{GS})/R_{REF}$$

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2$$