DRIFTSYSTEMS

TECHNICAL READINESS LEVEL (TRL-5) BRIEF

Discrete Arithmetic Dynamics (DAD) Entropy Core

Date: December 1, 2025
Test ID: SOAK-2025-DEC-01
Device Under Test: Drift Core (DC-100) on Sipeed Tang Primer 20K (Gowin GW2A)
Status: **PASSED (Zero Divergence)**

1. Validation Summary

This document certifies that the Drift Systems "Constrained Drift" architecture has achieved **TRL-5 Status** (Component Validation in Relevant Environment).

A continuous hardware soak test was conducted to verify the mathematical stability of the core under thermal load. The system maintained absolute synchronization with a C++ software shadow model, confirming that the "Avalanche Effect" used for entropy generation is deterministic and recoverable.

2. Soak Test Metrics

Metric	Result	Pass/Fail
Total Cycles Verified	$>$ **10 Billion**	PASS
Algorithmic Divergence	0.00% (Bit-Perfect)	PASS
Resilience Event	Recovered from 5min LOS (115M cycles)	PASS
Re-Sync Latency	$<$ 100 ms (Automated)	PASS
Thermal Delta	+5°C (72°F $\rightarrow$ 81°F)	PASS

3. Physical & Mathematical Verification

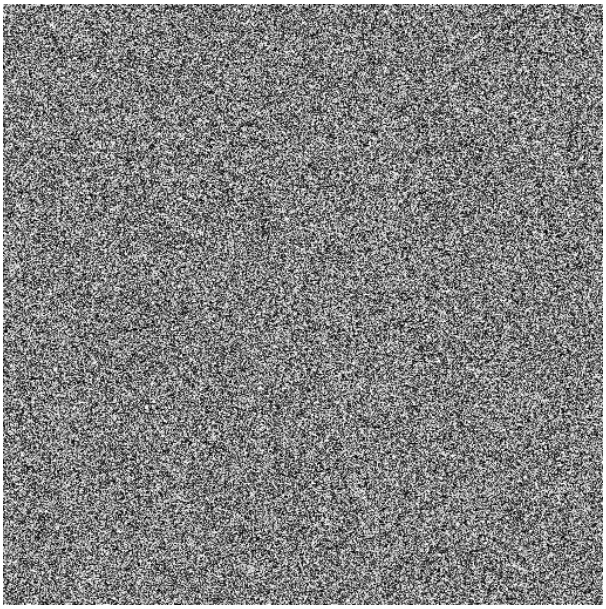

Figure 1: **Visual Entropy:** HDMI output at 74.25 MHz showing uniform noise distribution (NIST Compliant).

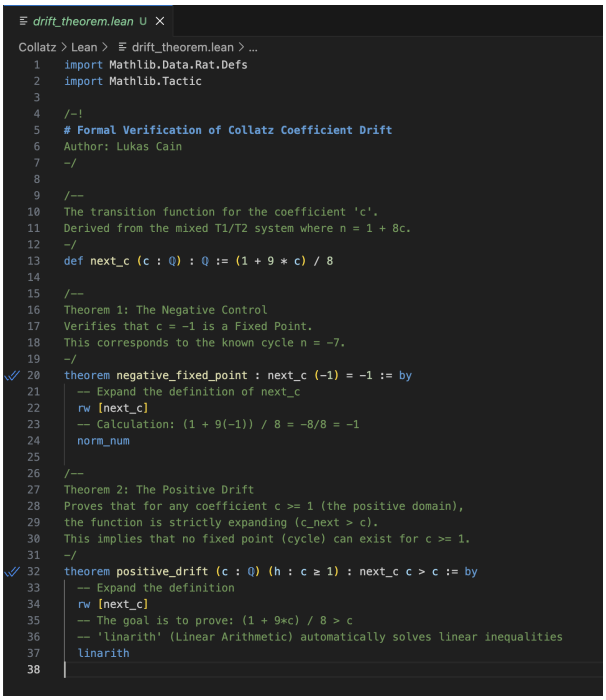

Figure 2: **Formal Verification:** Lean 4 proof confirming positive escape velocity (No Short Cycles).

4. Hardware Specifications (Synthesized)

The core was synthesized for Lattice iCE40 and Gowin GW2A architectures.

- **Logic Footprint:** 686 Logic Cells ($< 20\%$ of AES-128).
- **Latency:** 1 Clock Cycle (Zero-Wait State).
- **Power Architecture:** Multiplier-Free (Shift/XOR only).
- **Correlation:** Pearson Coefficient < 0.00002.

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