

## Research

# Back-contact Solar Cells: A Review

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*Ever since the first publications by R.J. Schwartz in 1975, research into back-contact cells as an alternative to cells with a front and rear contact has remained a research topic. In the last decade, interest in back-contact cells has been growing and a gradual introduction to industrial applications is emerging. The goal of this review is to present a comprehensive summary of results obtained throughout the years. Back-contact cells are divided into three main classes: back-junction (BJ), emitter wrap-through (EWT) and metallisation wrap-through (MWT), each introduced as logical descendents from conventional solar cells. This deviation from the chronology of the developments is maintained during the discussion of technological results. In addition to progress on manufacturing these cells, aspects of cell modelling and module manufacturing are discussed and an outlook towards industrial implementation is presented. Copyright © 2005 John Wiley & Sons, Ltd.*

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## INTRODUCTION

### Background

The research and development in the field of photovoltaic solar cells for terrestrial applications is focusing on lowering production costs. Next to producing larger volumes and exploiting highly automated production facilities, the use of larger and thinner substrates forms a cornerstone of this development.

Module manufacturing has had to follow this trend and in spite of the complexity of automating the interconnection of classical solar cells, fully automated equipment has entered the market to perform cell tabbing and stringing at competitive costs.<sup>1</sup> The conventional way of interconnecting cells by soldering highly conductive tabs to the front and rear of neighbouring cells is however being operated at the edge of what is possible. As cells become larger, the current increases and in order to keep the resistive losses within this tabbing material insignificant, the cross-section of the material perpendicular to the current flow has to increase. The cross-section can be increased by introduction of thicker tabs. The thickness of the tab is however limited by stresses built up in the solder joint due to the difference in thermal expansion coefficient of the tabbing material and silicon<sup>2</sup> which is even more crucial as cells become thinner. The width of the tab is the other parameter to increase its cross-section, but also this is severely restraint as it increases the shadowing losses proportionally.

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Wider tabs can eventually be used if the interconnection material is exclusively located behind the cells, except for a number of specific locations where it surfaces through the devices at the front of the module to be attached to the front surface grid of the cells.<sup>3,4</sup> The only changes to the conventional cells are the holes through which the interconnection is to be made. These holes can be made prior to the classical cell processing<sup>5,6</sup> or after finishing the solar cells.<sup>7,8</sup>

Another solution to maintain the interconnection circuitry behind the cells is by using back-contact solar cells. This is a general definition for all cell structures that have both the positive and negative external contact pads positioned on the rear surface.

Moving all interconnection circuitry to the rear of the module allows for an optimised module efficiency by increasing the packing density of the cells, and furthermore changes the visual appearance into a uniform dark plane. This aspect is much appreciated by designers and architects and, in contrast to thin-film modules that also exhibit this uniform dark plane and furthermore often are flexible, allowing easier integration into building components,<sup>9</sup> the higher efficiencies of rigid modules based on crystalline silicon make the modules very attractive for building integration. Within this fast growing market segment, the selected technology ultimately depends on a combination of the installation cost (cost/m<sup>2</sup>) and the cost per kWh, which results from the efficiency and area.<sup>10</sup>

Next to a potentially very simple interconnection technology related to the contacts being in a single plane, in such back-contacted structures both the shading losses and the resistive losses in the metal grids can significantly be reduced. The large variation in process steps, starting materials and cell sizes makes it difficult to compare published cell results amongst each other. However, with comparative experiments performance improvements of the back contact cells over conventional cells on the same starting material and with the same technology could be demonstrated.<sup>11,12</sup> On the other hand, the advanced cell structures generally invoke process modifications of which the related costs have to be compensated by the gain in performance and reduced module manufacturing costs.

### *Back-contact solar cells*

This review paper summarises the research and development efforts that have been undertaken on back-contact cell structures during the last 30 years, addressing the relevant features of the many designs that have been suggested. Before entering the technological discussion, in this section, the structural properties of the metallisation wrap-through (MWT), emitter wrap-through (EWT) and back-junction (BJ) cell structures are briefly introduced as they act as model classes to which the different cell designs can be categorised. Contrary to the technological discussion, where the structures are introduced according to the historical chronology, a logical evolution from conventional solar cells pointing out the most characteristic features is presented.

A schematic representation of part of a conventional bulk crystalline silicon solar cell is depicted in Figure 1. The silicon base is the main part of the mechanical structure. The emitter is located near the top or front surface. A metal grid to extract the carrier from the device contacts each of these silicon regions. Whereas the rear surface is often fully covered (as in the drawing), on the front surface the metal grid is the result of a trade-off between having low coverage to limit optical losses and high coverage to limit resistive losses. Most manufactures apply a front grid consisting of thin parallel lines (fingers) that transport the current to centrally located busbars. The busbars are relatively wide and can be used as solder pads to connect the to external leads.

The contact wrap-through or metallisation wrap-through (MWT) back-contact cell is the concept that is most closely linked to the conventional cell structure. In these cells, the emitter is located near the front surface, but part of the front metallisation grid is moved from the front to the rear surface. In the schematic representation in Figure 2, this is depicted as the busbar moving from one surface to the other. The remaining front surface grid is connected to the interconnection pads on the rear surface by extending it through a number of openings in the wafer.

In the emitter wrap-through (EWT) cell concept, the front surface is void of any metallisation. Whereas the emitter is still located near the front surface, all contacts are on the rear surface. In Figure 3, an embodiment of

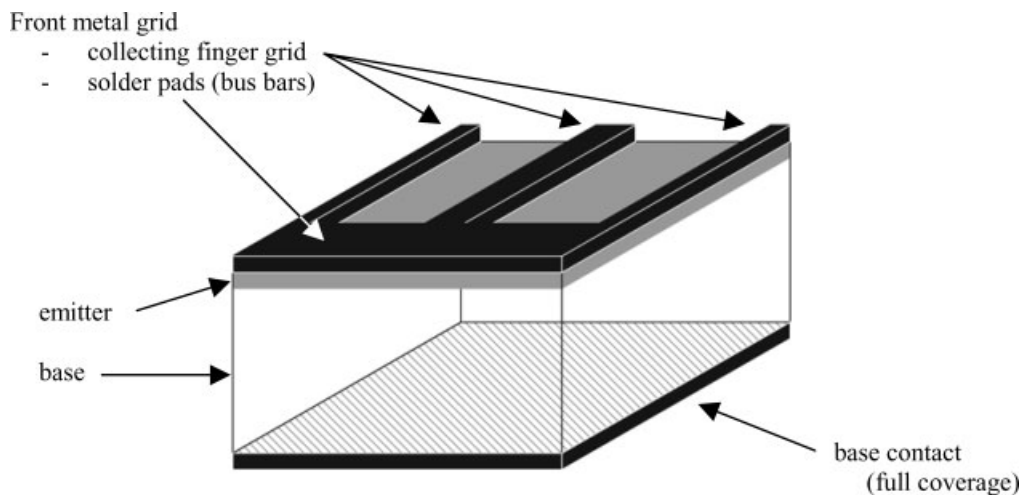


Figure 1. Schematic representation of a conventional solar cell

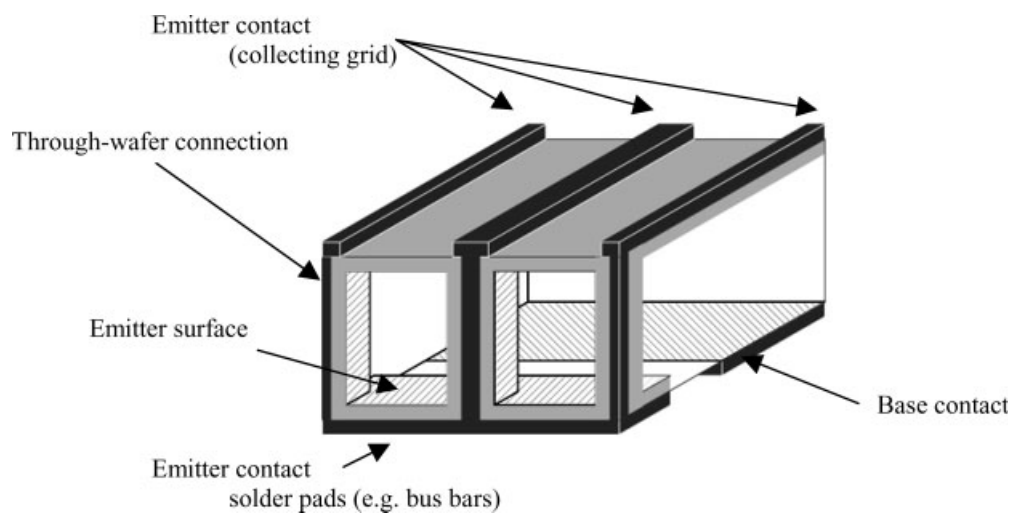


Figure 2. Schematic representation of a metallisation wrap-through solar cell

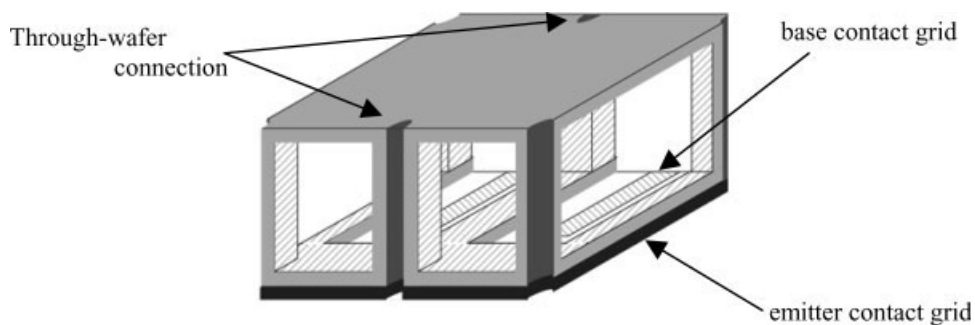


Figure 3. Schematic representation of an emitter wrap-through solar cell

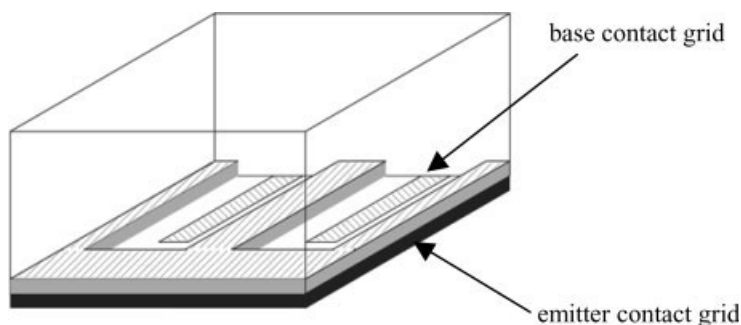


Figure 4. Schematic representation of a back-junction solar cell

this structure is shown where the emitter contact grid from the conventional cell in Figure 1 is moved to the rear surface. As such, the base contact is reduced to a similar grid that interdigitates with the emitter contact grid. The connection between the active emitter near the front surface and the emitter contacts on the rear surface is provided by extending the emitter in the walls of holes in the substrate.

Finally, in the back-junction cell concept, the emitter is no longer located near the front surface, but together with the contacts moved to the rear surface, as shown in Figure 4.

The technology discussion presented in the remainder of this paper starts with these cells with the emitter on the rear surface, followed by the designs that maintain the emitter on the front surface. As many of the relevant topics for the latter category are addressed within the discussion of the former, only the differences are pointed out further on.

## THE TECHNOLOGICAL DEVELOPMENT OF BACK CONTACTED SOLAR CELLS

### *Back-junction solar cells*

Interdigitated back-junction solar cells have been suggested as a cell design to cope with high intensities of incoming energy fluxes and the related high current densities such as in concentrator applications<sup>13,14</sup> or thermophotovoltaics.<sup>15</sup> In these devices, the electron-hole pairs are generated in a high-lifetime bulk region and are collected at interdigitated diffused junctions on the rear side of the cell. With both the  $p^+$  and  $n^+$  junctions on the rear side of the device, there is no metallisation pattern on the front surface to shadow the incident photon flux. Also, since nearly one half of the back surface can be covered with the metallisation pattern of each type, the series resistance of the metal pattern can be very low. Furthermore, as there is no need to conduct the current along the emitter as with front-contacted cells, there is no trade-off between series resistance and grid shading and the rear junction can be optimised in terms of the lowest saturation current only.<sup>16</sup>

Another possible use for back-junction cells is as the bottom cell for tandem solar cells. Its use can reduce the losses related to current mismatch between the bottom cell and top cell(s) as the excess current generated in the bottom cell can be extracted through emitter contacts at the rear surface without the need to pass through the remainder of the device.<sup>17,18</sup>

From the onset of the developments it was clear that this structure requires a high ratio of the minority-carrier diffusion length within the bulk  $L$  over the device thickness  $W$  combined with exceptionally low values for the front surface recombination velocity  $S_f$ . In this respect, the use of highly resistive base material is favoured. On the other hand, using higher doped substrates retains the base in low-level injection, which results in cells with lower diode ideality factors and thus increased fill factors.<sup>19</sup> Next to the use of high-quality starting substrates, processing conditions for these solar cells have to be such that the high minority-carrier lifetime is maintained and low front surface recombination velocities are obtained.

The strong dependence of the device performance on the  $L/W$  ratio of the cells limits its application to high-quality materials such as FZ-silicon or using very thin substrates or even epitaxially grown layers.<sup>20</sup> Alternatively, a high effective ratio is obtained by deviating from classical planar cell structures and sculpting the devices chemically<sup>21,22</sup> or mechanically.<sup>23</sup> With the sculpted features formed on the front surface, these devices furthermore exhibit a larger ratio of illuminated area to cell volume compared with a planar device, which has a beneficial impact on the open-circuit voltage of the cell.<sup>21</sup>

However, as silicon is only weakly absorbing the light, decreasing the cell thickness degrades the optical characteristics of the cells unless light trapping schemes such as surface texturing are introduced.<sup>24–26</sup> Making the back surface highly reflective will reflect many of the photons reaching this surface towards the front and give them additional opportunities to produce electron–hole pairs.<sup>27</sup> In this respect the limiting the contact region of the cell is advantageous as it has been found that it is much easier to make the undoped, uncontacted regions reflective than contacted regions.<sup>28</sup>

While in the original concentrator applications, the emitter saturation current was the main loss mechanism, for application at 1 sun, the surface recombination proved to be the dominant mechanism.<sup>29,30</sup> A low front surface recombination velocity can be achieved by the use of passivating dielectrics (high-quality thermal oxides,<sup>31,32</sup> deposited layers such as  $\text{SiN}_x$ , front surface fields<sup>33,34</sup> or front surface floating junctions<sup>34</sup>).

On untextured surfaces, the recombination velocities obtained by thermal oxides can be below 2 cm/s. However, this passivation is not stable under illumination<sup>35,36</sup> and it is very hard to achieve such low recombination velocities on textured surfaces.<sup>37</sup>

Using doped layers at the front surface shields the minority carriers from the actual surface recombination. With careful design of the doping profiles,<sup>38</sup> the recombination velocity at the physical surface will have no influence on the short-circuit current of the cell up to values of  $10^4$  cm/s. This is one of the reasons why no performance degradation is observed, even under concentrated ultraviolet light.<sup>39</sup> Furthermore, such dopant diffusion introduces a quadratic dependence of the surface recombination velocity on the carrier concentration. This limits the loss in voltage and fill factor resulting from the linear dependence observed at oxide passivated surfaces.<sup>40</sup>

Front surface fields or floating junctions can either physically be present or induced by fixed charges in a covering dielectric layer. The latter seems preferred as the diffusion or implantation of a more highly doped region introduces the possibility of lattice damage, reducing the lifetime or even leading to a dead layer at the surface.<sup>41</sup> Surface passivation by means of a floating junction furthermore depends on the forward bias over the junction. In case of application at the front surface, under normal operation conditions, such a bias is induced by diffusion of photogenerated carriers, but the nonlinear decrease of the short-circuit current density for lower illumination intensity indicates the critical dependence of this mechanism on carrier generation.<sup>42</sup> The forward bias over the junction not only causes photogenerated carriers to migrate to the back junction, but also eliminates the reduction in photoresponse over the rear surface base contact regions as encountered in cells with passivation relying on front surface fields.<sup>43</sup> as the floating emitter collects minority charge carriers from the base above these regions and re-injects them in the base above the collecting emitter.<sup>44</sup> On the other hand, the devices with a front floating junction suffer from the disadvantage of additional recombination in the depletion region between the inversion and base regions, especially when in case of induced junctions the potential built up by the fixed charges is insufficient. This recombination is most significant at low intensity levels.<sup>41</sup>

Next to a low surface recombination velocity at the front surface, the need for back surface passivation is evident.<sup>53</sup> Its importance is proportional to the minority-carrier mobility divided by the doping concentration in the base and by turning to lower base resistivities, the influence of the rear surface passivation can be reduced. Furthermore, this surface hosts the extended termination of the junction, leading to a space-charge region surface recombination that can significantly contribute to the second diode recombination current and thereby lower both the open-circuit voltage and fill factor of the cell.<sup>45</sup> Furthermore, the presence of diffused regions of both polarities and corresponding contacts on the rear imposes further constraints on the passivation scheme. Contrary to the front surface, when applying dielectrics that achieve the passivation based on inducing a junction or surface field in the silicon, precautions have to be taken that no surface conductance channels are formed between the emitter and base contacts.<sup>46</sup> A thermal oxide or densified deposited oxide are the preferred materials to passivate the rear surface when different polarity regions are present.<sup>47</sup>



The recombination at the edge of the cells is another important parasitic loss mechanism.<sup>42,48</sup> It can be overcome by passivation of the edges, moving the edges far from the active region and using the cells in a shingled mode such that the borders are shadowed, using higher base doping levels or making large cells in order to minimise the perimeter relative to the active area.<sup>49</sup>

As for all back-contact structures, ultimately, large-scale implementation relies on a low-cost way of defining, isolating and contacting regions of different polarities on the rear surface. Especially for the back-junction concept this is very challenging as the concept imposes that the base-contact regions are sufficiently small to maintain a high collection probability for minority carriers generated above these regions.<sup>50</sup> Additionally, the resistive losses related to majority carriers flowing through the base to the contact regions impose a high density of these contact regions. This lateral current of majority carriers through the base of the cell is also occurring at the location of the connection pads of the emitter area. These pads must have a large enough area to connect electrical leads to it, but it pays to reduce their width as much as possible.<sup>51,52</sup>

The use of photolithography permits for the definition of small emitter and base diffusions and contact regions without excessive shunting.<sup>45,53</sup> The alignment of steps can be avoided when the first steps create surface structures such as sharp edges that allow for self-aligned metallisation of the different contact regions.<sup>54,55</sup> This introduces possible disadvantages as an increased area of dopant diffusions, having its effect on the attainable voltage, and a lower reflectivity at the rear surface as the metal in contact with the silicon is not as good as a rear mirror as when an intermediate dielectric layer is present. At the cost of an extra mask, additional degrees of freedom can be introduced in the design when an oxide is grown over the diffused areas and windows are cut just prior to metal deposition. In this way, the diffused areas are largely passivated and the rear surface mirror is restored.<sup>56,57</sup> Additionally, the range of surface concentration for the diffusion is broadened as the trade-off between low doping in order to avoid shunting and high doping in order to assure a good ohmic contact is avoided.<sup>58</sup>

Processes with multiple aligned lithographic steps can hardly be applied in high-throughput process. With more cost-effective processes based on the laser grooved buried contact technology, the lasers can be used to contact buried layers and automatic isolation between *n*- and *p*-type metallisation is provided.<sup>59</sup> For the screen printing technology lasers can as well be applied for the junction isolation<sup>60</sup> next to a number of other possibilities such as mechanical abrasion, using the metal grids on the rear as a mask for self-aligned plasma etching,<sup>61</sup> selective chemical etching either directly by means of deposition of an etching agent<sup>62</sup> or indirectly by means of printing etch resist,<sup>63</sup> the use of diffusion barriers either directly<sup>64</sup> or indirectly<sup>65</sup> formed, co-diffusion of aluminium and phosphorus,<sup>66</sup> etc. The complexity of the process modifications required for these approaches limited their application to laboratory-scale developments.<sup>67</sup> Furthermore, if abrasive methods are used, the region that host the junction termination is highly damaged, which affects the recombination current. An easier solution resides in the development of self-doping contacts, where formation of the junction and the ohmic contact is defined by the metallisation pattern and confined into a single step. On *n*-type substrates, the quality of a *pn* junction alloyed from a screen printed aluminium paste is sufficient as an emitter on the rear of the cell<sup>68</sup> although the high recombination current density imposes to apply localised junctions.<sup>69</sup> Similar contacting schemes are being explored for the formation of *n*-type junctions in *p*-type wafers based on adding dopant atoms to Ag pastes. The additional dopant atoms are required as Ag does form an alloy with silicon, but it is not a dopant.

For a screen-printing-based technology however, a potential complication for manufacturing exists as several metal grids have to be printed within very tight tolerances of line width and spacing.<sup>70</sup> This is even more stressed as for successive metallisations on the same surface, the height of the deposited pattern during the first print makes the second print less accurate.<sup>63</sup> Additionally, the conductivity of the base metallisation has to be sufficiently high to limit an increase of series resistance invoked by replacing the full coverage base metallisation with a gridded structure.<sup>71</sup> As for the buried contact cell technology, the multiple high-temperature furnace steps included in a buried contact process may degrade the bulk lifetime, which is a particular concern with solar-grade silicon materials.<sup>70</sup>

Once the base lifetime is sufficiently high and all the surfaces are passivated, recombination in the contact areas becomes dominant. This is the primary reason for reducing the contact coverage fraction as in the 'point contact' cell.<sup>72,73</sup> Characteristic for this cell are the alternating *n*- and *p*-regions, forming a polkadot array on

the bottom surface of the device. The reduction of the recombination in the contact areas results in an increased open-circuit voltage, but the design has to be carefully evaluated such that this improvement is sufficient to balance the reduction of the short-circuit current and/or the fill factor.<sup>74–76</sup>

For concentrator applications, back-contact cells have demonstrated the highest efficiencies. However, the fabrication process and the structural design have evolved and matured to a stage that is similar in complexity to that of high-efficiency front gridded cells, especially if one considers the sophisticated technologies used to minimise the losses related to the front surface grid.<sup>77</sup> Although the metal contacts may cover almost the entire surface, and may be as thick as desired, even for concentrator cells as small as 15 mm<sup>2</sup>, the metal resistance remains a problem at moderate illumination levels.<sup>78</sup> This can be resolved by designing the cells with multi-level metallisation schemes<sup>79</sup> at the expense of additional process steps.<sup>80</sup> On the other hand, the use of such multi-level metallisation schemes relying on expensive intermetal dielectric layers, resolves issues with scalability of this cell concept to large area, one-sun cells,<sup>81</sup> although the involved costs do not outweigh the gain in efficiency when using highly conductive contact structures.<sup>82</sup> Alternatively, the cells can be implemented on rectangular substrates of limited width. In this case, the length of the grid lines is limited when they are running parallel to the short edge. As rectangularity is a natural feature of many thin ribbon silicon materials, the IBC cell should receive consideration as ribbon growth techniques well adapted to thin wafer production become more prominent.<sup>47</sup>

The primary disadvantage of the high-efficiency back-junction solar cell is its high cost related to complicated processing involving several lithographic patterning steps. The price of the cells is affordable to just a few niche applications or for concentrators,<sup>83</sup> where the original design and processing is still relevant.<sup>84</sup> However, the potential for high efficiencies triggered the development of lithography-free processes. As these developments benefit from the studies of bulk and surface passivation for conventional solar cell structures, the major obstacles towards an industrial process prove to be providing sufficient conductivity to the rear surface interdigitated grids<sup>85</sup> and avoiding shunting.<sup>86,87</sup> Both with the buried contact technology<sup>88</sup> and with the oblique evaporation of contacts<sup>89</sup> efficiencies above 19% have been reached albeit on relatively small areas. Some preliminary efforts towards back-junction cells with screen-printed metallisation were reported.<sup>60,90,91</sup> However, it should be noted that this technology faces more challenges than merely demonstrating its potential by using adapted evaporation masks.<sup>92</sup>

#### *Front junction solar cells*

The main incentive for maintaining the junction at the front surface of the cell is to improve the effectiveness of the collection, especially for material with a low minority-carrier diffusion length over device width ratio  $L/W < 3$ . Furthermore, the necessity of close control of the front surface recombination velocity for rear junction cells complicates the process and is difficult to apply to textured surfaces.

Further improvement of the collection of deeply-generated carriers can be achieved by an additional collecting junction at the rear of the cell.<sup>93–95</sup> Such tandem structures can alleviate some of the problems encountered within the tendency towards the use of thin substrates such as back-surface recombination. The structures have a reduced rearside recombination area since the highly doped base contact region is limited and alternated with extended emitter regions. As the cells become thinner, the amount of back-junction collection will increase because the recombination in the base material decreases. A 300- $\mu\text{m}$ -thick tandem structure demonstrated an increase in short-circuit current density of 2–3 mA/cm<sup>2</sup> from the back junction<sup>96</sup> while a short-circuit current density of 37.4 mA/cm<sup>2</sup> was measured on 200- $\mu\text{m}$ -thin screen-printed large-area multi-crystalline cells.<sup>97</sup>

#### *Emitter wrap-through solar cells*

These cells exhibit next to the collecting junction on the front surface a junction of the same type over most of the back. Photocurrent is collected by both junctions connected in parallel by a multiplicity of small-area interconnections paths. By this mechanism, the EWT cell performance is over a wide range nearly independent of the cell thickness to diffusion length ratio.<sup>98</sup>

These vias can be formed by photolithographical patterning and etching pyramidal indentations that do not<sup>99</sup> or barely<sup>100</sup> penetrate through the wafer. In a thin-film approach, after formation of the holes, a thin silicon film

is separated from its supporting substrate by etching the underlying layer through the via-holes.<sup>101,102</sup> Drilling of the vias by means of a laser is a more universal approach towards lower-quality materials as it is independent of surface orientation.<sup>103</sup> Although laser processing has demonstrated high efficiency and high flexibility, mechanical sculpting seems more favourable towards this application. Mechanical scribing can be used to generate holes in the wafer by scribing deep lines on the front surface and then also scribing perpendicular grooves onto the rear surface. The intersection of these grooves forms the hole.<sup>59</sup> Assuming a uniform distribution of the interconnection vias, hole densities above  $100\text{ cm}^{-2}$  are needed to keep the resistive losses sufficiently low. This number can be somewhat relaxed by densification of the hole density in one dimension, allowing a broadening in the other. At its extreme, this results in the formation of slots of which the spacing is similar to the finger grid spacing of conventional solar cells.<sup>104</sup>

The presence of the front surface diffusion relaxes the limitations on contact size and spacing encountered with the back-junction cells up to a level that can be attained with screen printing,<sup>71</sup> although the theoretical deduced optimal pattern is still very hard to achieve within the accuracy of a screen-printing-based technology.<sup>105</sup> The buried contact cell technology seems exceptionally suited for the EWT cell process as formation of the grooves and vias can be done in a single step, ensuring good alignment.<sup>103</sup> As such, the process flow for EWT cells only differs slightly from process flows for conventional solar cells and as such most of the processes required for fabrication are well developed. The new processes required for the fabrication of an EWT cell include laser drilling of the vias, diffusion of phosphorus through the vias with low electrical resistance and incorporation of an interdigitated base contacting into the process sequence.

The diffusion within the walls of the vias is no problem whether the diffusion occurs in a gas atmosphere or using screen printed sources.<sup>106</sup> The vertical junction along the emitter covered edge of the holes shows no further improvement of the collection probability, but neither shows any detrimental effects that could be induced by remaining surface damage.<sup>107</sup>

Cell efficiencies up to 21.4% on small areas ( $6\text{ cm}^2$ ) demonstrate the potential of the cell concept<sup>108</sup> and the advantage of EWT structures over back junction structures on materials with relatively low diffusion lengths compared with the cell thickness could be demonstrated experimentally.<sup>109</sup> Large-area EWT cells with screen printed metallisation suffer from a high series resistance that limits the fill factor. Similar problems were encountered for cells with evaporated contacts<sup>110</sup> and for cells where the contacts are formed by electroless plating.<sup>111</sup> With the latter technologies, this could be overcome by extended evaporation or plating, which indicates that the low fill factor is mainly related to the conductivity of the contact metallisation.

To date no solution has been found to have sufficiently fast drilling of the vias. A typical via spacing of 1 mm would require almost 25 000 holes in a  $156\text{ cm}^2$  substrate. Even with laser systems capable of drilling holes in silicon in a single pulse with a repetition rate greater than 1 kHz, the throughput of modern production lines (1000 cells/hr) cannot be reached.

#### *Metallisation wrap-through solar cells*

These cells are characterised by the presence of a metal grid on the front surface in combination with the presence of interconnection pads for both polarities on the rear surface. This cell design does not eliminate the front surface shading losses, but by avoiding the interconnect pads and solder strips, these losses are significantly reduced.

The front metal grid is connected to the corresponding pads either around the edge of the wafer<sup>93</sup> or through holes<sup>112,113</sup> or slots<sup>114</sup> made in the substrate. The formation of holes through the substrate resolves the scalability of wrapping the contacts around the edge of the wafer. Shunting between the contacts is avoided by wrapping the junction along with the metallisation and performing the junction separation on the rear surface. Contrary to the EWT cells, the surface termination of the space charge region is thus limited in length. Alternatively, the emitter can be restricted to the front surface and the metal contact separated from the silicon by a thick insulator on its way to and on the rear surface.<sup>114</sup> The functionality of the rear surface pads can be restricted to the interconnection,<sup>115</sup> but can optionally be combined with an extended contacted emitter region at the rear of the cell.

As only the contact pads are on the rear surface, the base contact still covers most of the rear surface and the need for very high conductivity of the base metallisation is less than for the IBC and EWT cells and the increase in junction bordering is reduced which allows the use of the technically simpler abrasive junction isolation



methods described above. Furthermore, with the exception of wrapping the contacts around the edge, the concept is fully scalable as an increase of wafer dimension can be counteracted by simply increasing the number of through wafer connections<sup>116</sup> and using dedicated grid designs.<sup>117</sup>

As for the EWT solar cells, the processing of these structures only shows small differences with industrial processes for conventional cells. Next to the formation of the openings (in case of wrapping the contacts through the wafers), the additional steps are the formation of the contact pads on the rear surface and the connection between the front grid and contact pads. The connection through the holes or around the edges can be done without additional steps by screen printing<sup>104,118</sup> or plating<sup>11</sup> of contacts. Alternatively, the contacts may be remotely prepared and transferred to the cells.<sup>119</sup>

## CELL MODELLING

In back-contact solar cells both the base and emitter contacts are placed on the rear surface. A comprehensive analysis of such a structure has to take into account two-dimensional effects. To some extent however, one-dimensional simulations suffice to gain insights in the behavior of the back-contact structures as a function of physical parameters of the cells as these characteristics are mainly governed by the predominant cross-section. The combined effect of minority-carrier diffusion length  $L$ , cell thickness  $W$  and surface recombination  $S_f$  are typical examples. Also the impact of a combined collection on the front and rear surface was studied by one-dimensional simulations and confirmed by a detailed study, including the two-dimensional effects.<sup>120</sup>

Contrary to the short-circuit current and open-circuit voltage, the fill factor and thus conversion efficiency are influenced by the internal series resistance  $R_s$  of the cell. The series resistance of the back contact solar cells is increased by the important contribution of the base region and that of the base metallisation grid since the current of majority carriers flows in the base in a direction parallel to the cell surface. This imposes contrary design considerations to the tendency of maximizing the  $L/W$  ratio, as some advantage exists in using thicker cells or low resistive base material because of a reduction in series resistance.<sup>121,122</sup> One-dimensional modeling can be extended by indirectly including the geometrical and material characteristics in the model parameters such as the series resistance,<sup>123</sup> but still cannot address the essential multi-dimensional aspect of the problem and cannot tackle the issues of optimum contact size and spacing. Several compromise methods can be used to avoid the exact numerical solution of the semiconductor transport equations in the complex multi-dimensional geometry. Often, these methods offer interesting insights in the operation of the devices. One such method is based on emphasising the accurate determination of the total recombination current, rather than carrier densities and fluxes.<sup>28</sup>

Another method is based on the use of one-dimensional analyses to determine an equivalent lumped circuit model for the different areas of the cell. These can be connected together using resistors representing the resistive losses occurring along the possible current paths. Thus the whole cell can be transformed into an equivalent electrical network and a nodal analysis can be carried out without the need of extensive computing power.<sup>114</sup>

Typically, the components used to represent the different areas are a diode and a current source. The diode is characterised by its dark saturation current and ideality factor and represent the recombination losses in the cell and at the surfaces. The current source represents the photogenerated current in such an elementary section. However, the presence of an additional doped region on the front as front surface field or floating junction cannot just be simulated by replacing it in the model as an intensity dependent effective recombination velocity similar to the behaviour of a back surface field in a conventional solar cell. The recombination of carriers generated in the highly doped front region will cause a decrease in the quantum efficiency at low wavelengths which cannot be explained by such a straightforward model.<sup>38</sup> The nonlinear behaviour can be described by a shunt-like effect at the doped region.<sup>42</sup> In case of collecting junction both on the front as rear surface, the circuit can include a transistor<sup>124</sup> or its related Ebers—Moll model.<sup>51</sup>

The use of numerical simulators is becoming increasingly common as computing power increases. These simulations could only validate and confirm the conclusions of the multi-dimensional analyses carried out by nodal analysis.<sup>125</sup>

## MODULE MANUFACTURING

The back-contact cell structures have inherent advantages for module production. As the external contacts of both polarities are on the rear surface, the packing density of the module can be very high, further increasing the performance gain by the use of back-contact cells.<sup>126</sup> On the other hand, it should be understood that merely offering the interconnection pads on the rear surface does not automatically lead to a simplification of the module manufacturing. The processes involved in the formation of the interconnection circuitry will impose certain constraints on the geometrical location and size of these pads. The interdependence of the structures and processes requires a close cooperation between the development of advanced module concepts and cell designs as a number of technical challenges can either be tackled on the level of the cell processing<sup>127</sup> or by adapting the module manufacturing processes.<sup>128</sup>

A new module assembly process is needed that takes advantage of the opportunities offered by the back-contact solar cells. The process must produce a module package that is reliable and durable. At minimum, the new process must pass commonly accepted environmental, mechanical and electrical qualification test requirements (ASTM, IEA, IEEE, etc.). Within any interconnection concept, one of the more critical issues is the reliability of the formed interconnection, especially when other technologies than soldering are applied.

A class of very appealing module fabrication concepts includes the monolithic module assembly processes.<sup>129</sup> In these advanced processes, the connections between the cells form as a consequence of processing steps applied to the whole module structure as opposed to connecting cells one by one and then placing them onto the module structure.

The interconnection circuitry on which the cells are positioned can be formed directly on the back sheet or on an intermediate screen. The latter solution prevents movements of the cell interconnects during lamination, provides positional accuracy and allows the rear encapsulant to flow through and encapsulate the back surface of the cell. The circuitry consists of bonded metal foil traces or a deposited conductive material.

The actual interconnection can be done by means of solder, pressure-sensitive or thermosetting acrylic-based conductive adhesives or silver-filled conductive epoxies. As long as silver-coated surfaces are used, conductive adhesives readily available on the market offer a feasible alternative to soldering for the interconnection of back-contacted solar cells.<sup>130</sup> The conductive epoxies have excellent electrical and mechanical properties, and are capable of meeting qualification tests,<sup>131</sup> but cost is a concern. Acrylic conductive adhesives meet the cost goals, but although they have been used in applications with similar reliability requirements as photovoltaic modules, their reliability has yet to be demonstrated in a process compatible with module manufacturing. The mechanical fixation of the conductive adhesives before curing is poor, but with slight modifications to the commonly applied heat–pressure cycle, a combined curing of the adhesive and lamination in a single process step can be realised without disturbing the electrical interconnection of the module by shifting of cells or connectors.<sup>132</sup>

One of the challenges module manufacturing will have to cope with is that several of the cell structures under investigation will require that the interconnection circuitry crosses metallised areas of both polarities on the cell rear.<sup>133</sup> If no special measures are taken to avoid physical contact between the circuitry and the metal on the cell rear, the risk of shunting is very high. This is a typical example of the interdependence of the developments as it is not clear whether the formation of local isolation should occur either on the level of the cell production<sup>105</sup> or module manufacturing.<sup>132</sup>

Most of the material costs for the module assembly are similar to present technology (e.g., glass, encapsulant and backsheet). If one furthermore assumes the encapsulation equipment and throughput similar to present industry standards, the difference in cost is due to differences in the electrical circuit assembly. The module assembly cost can be reduced by using planar processes that are easy to automate, by reducing the number of steps, and by eliminating low throughput steps as individual cell tabbing, cell stringing, etc. Using a single pick-and-place station to lay out the cells for encapsulation will replace tabbing machines, cell stringers and layout work stations of the present process, increasing throughput and yield at lower capital cost of current production.<sup>134</sup> Consequently, a cost reduction of nearly 50% is estimated for labour and capital in the module area of the PV module manufacturing plant. Conservative estimates of the added cost for the manufacturing of the dedicated interconnection structures and materials required reduce this cost advantage to saving of 10–20%

at the module level. Any increase in cost for the fabrication of the back contact cells would reduce these potential cost savings further. On the other hand, including advanced roll-based encapsulation technologies, even further cost reductions could be achieved.

Next to the large-scale power generation, the back contact cells are very well suited to address the needs of the increasing number of power intensive mobile consumer and telecommunication electronics. Typically, these applications offer a small useful area and demand output voltages of several volts, efficiencies well beyond the predominant amorphous silicon thin-film arrays and sufficient device performance at low illumination intensities. On a single wafer, a large number of unit cells can be manufactured that can be mounted onto a circuitry carrying substrate.<sup>135</sup> The transfer to the substrate can be done either before or after separation from the wafer.

Demonstration modules have been made with module efficiencies up to 21.6% with high-efficiency back-junction solar cells<sup>126</sup> and 14.7% with screen-printed metallisation wrap-through cells.<sup>127</sup>

## INDUSTRIAL IMPLEMENTATION

Not the cost, but drivers such as weight and radiation resistance have invoked a trend towards thinner and larger substrates for silicon space solar cells.<sup>136</sup> In view of the minor process changes required for metallisation wrap-through devices, these structures became the first back-contact cells to appear in pilot line production. The cells fitted within the objective of the Spectrolab large-area, low-cost solar cell development towards combining space quality with low cost processing potential.<sup>137</sup> More recently, this cell type has been at the centre of a growing industrial interest in back-contacted solar cells. In 2003, the research work carried out at IMEC was exploited as the 10 MW<sub>p</sub> production line of Photovolttech NV was constructed such that both conventional and MWT cells can be produced on the same line.<sup>138</sup> After the announced expansion, 25% of the 80 MW<sub>p</sub> capacity will be dedicated to MWT solar cells. Also Solland Solar Energy BV announced the production of this cell type from 2006 in its production lines currently under construction.<sup>139</sup>

Further technical developments of the pioneering work at Purdue University on the back-junction cell concept<sup>140</sup> resulted in a cell technology that could be commercialised for concentrator applications.<sup>141</sup> This was achieved by Amonix and SunPower. At Sunpower, the technology developed at Stanford University was completely revised, avoiding the use of pyrophoric gases and hazardous chemicals. A large-volume production of point contact solar cells was established in a class 100 clean room corresponding to 7.5 MW of concentrator cells per year.<sup>142</sup> The first time these cells were used for a non-concentrating application was on the Honda car in the 1993 World Solar Challenge. The large-area cells were produced with a slightly simplified technology compared with the concentrator cells, but still requiring several photolithographical masking steps. Over a period of 4 months, more than 7000 cells were produced with a very tight efficiency distribution from 20 to 22%. This was further improved as in 1996 the average efficiency over a production volume of 10000 cells was increased by 1% absolute to 22.1%. With an average of 500 cells/day, the throughput of the production at this stage was rather limited, which is not surprising in view of the technology.<sup>143</sup> Further process simplifications were introduced towards mass-production of the high-efficiency devices and large-area cell efficiencies above 20% were achieved within in 1 MW/yr pilot line.<sup>144</sup> Based on the results of the pilot line, Sunpower designed a 25 MW/yr factory that was completed in 2004. Recently, the company announced an expansion of the capacity to 50 MW by the second half of 2005.

Also the emitter wrap-through concept is explored for industrial implementation as Advent Solar is starting up in a pilot line mode based on the technology exclusively licensed from Sandia Labs.<sup>145</sup> The company expects to build a 50 MW<sub>p</sub> production facility in 2006.

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