EMITTER WRAP-THROUGH SOLAR CELL

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ABSTRACT

We present a new cell concept (Emitter Wrap-Through or EWT) for a back-contact cell. The cell has laser-drilled vias to wrap the emitter on the front surface to contacts on the back surface and uses a potentially low-cost process sequence. Modeling calculations show that efficiencies of 18 and 21% are possible with large-area solar-grade multi- and mono-crystalline silicon EWT cells, respectively.

INTRODUCTION

Commercial one-sun silicon solar cells have the photocarrier-collection junction (emitter) and a current-collection grid on the front surface. A front-surface emitter is necessary for good internal collection efficiency; solar-grade silicon materials typically have diffusion lengths less than the device width. The front-surface grid is necessary for low series resistance. Front-gridded cells have the well-known grid optimization tradeoff - increasing the grid coverage reduces losses due to series resistance but increases losses due to grid obscuration. Other problems associated with the front-grid cell design include the following: increased complexity for cell manufacturing due to the requirement for fine-line grid definition, poorly optimized emitter due to requirements of low-cost metallizations (i.e., high surface concentration), and reduced packing density of cells in the module and increased complexity of module assembly due to front-to-back cell stringing [1]. Commercial one-sun silicon solar cells use screen-printed silver lines that have relatively poor aspect ratios (grid height divided by width), conductivity, and contact resistance. Wenham estimates that losses due to grid obscuration, grid resistance, and poor emitter characteristics reduce the cell performance of commercial screen-printed solar cells by nearly 30% relative to high-efficiency (i.e., > 20%) laboratory cells [1].

Placing both the n-type and the p-type current-collection grids on the back surface of the solar cell (i.e., "back-contact") has several advantages compared to the front-grid cell. The most obvious advantage of a back-contact cell is higher performance from no grid obscuration and low grid resistance; the only constraint on the grid design is the technological limits of the metallization technology. Another important advantage of back-contact cells is simplified module assembly and better packing factor of cells in the module; front-to-back stringing of front-contact cells requires additional space between cells for the tabs, is difficult to automate, and has a non-uniform surface for encapsulation. Back-contact cells also present a more aesthetic uniform appearance, which is important for some consumer applications (e.g., photovoltaic sunroofs for automobiles). Finally, back-contacted cells allow for the possibility of a high-voltage cell through monolithic series connection of cells on a single substrate.

There are two approaches for placing both contacts on the back surface of a solar cell. In the first approach, photocarrier-collection junctions and grids for both polarities are located on the back surface ("back-junction" cell). Swanson *et alia* demonstrated an efficiency of 21% with a one-sun, 35-cm^2, back-junction silicon solar cell [2]. The photogenerated carriers must diffuse to the back surface for collection in back-junction cells; hence, these cells require materials with diffusion lengths much longer than the device width for good photocarrier-collection efficiency. The back-junction cells are therefore not useful with many solar-grade silicon materials that have diffusion lengths shorter than the device width.

The second approach for placing both contacts on the back surface of the solar cell keeps the collection junction on the front surface, which is more desirable for one-sun solar cells. This approach requires holes ("vias") through the substrate for the current-collection grid on the back surface to contact the collection junction on the front surface. Hall and Soltys described such a cell in 1980 that used aligned photolithography and wet-chemical etching to form the vias [3]. K. Fujui, K. Shirasawa, and H. Watanabe recently described a back-contact cell with a front-surface collection junction that they named the Through-Hole Back-Contact Solar Cell [4]. They did not provide a description of the process sequence. They reported results of 2-dimensional modeling that indicated efficiencies approaching 28% were possible, and reported a J_{sc} of 40 mA/cm^2 and a V_{oc} of 543 mV for a 4-cm^2 test device.

In this paper, we describe a new approach for a back-contact cell with a front collection junction. We refer to the new cell concept as the Emitter Wrap-Through cell since the emitter is wrapped through vias to the back surface for contacting. An important feature of the EWT cell is the process sequence; the EWT-cell process is based on the buried-contact cell process, which has been shown by several authors to be potentially cost competitive with conventional screen-printed cells and is in pilot production at several locations [5].

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CELL AND PROCESS DESCRIPTION

Figure 1 presents a schematic of the EWT cell. For the purposes of this discussion, we assume that the substrate is p-type silicon. The front surface has only a phosphorus diffusion (emitter) and an anti-reflection coating. The front surface may also be textured for low reflectance and light trapping. The back surface has two sets of interdigitated grids. The two sets of grids are the p-type and the n-type contacts. The n-type grid is a laser-scribed groove that has been heavily diffused with phosphorus and filled with metal. The front-surface emitter is contacted from the back surface through laser-drilled vias [6]. The vias are aligned with the n-type grooves on the back surface and are also heavily phosphorus diffused and metallized at the same time as the n-type grooves. The heavy groove diffusion reduces contact resistance and contact recombination. As will be discussed later, there are several options for the interdigitated p-type grid and substrate contact.

Figure 2 presents a relatively simple variation of the EWT cell with a double-junction emitter; i.e., there is a photocarrier-collection junction on both surfaces. A double-junction emitter cell collects photogenerated carriers from both surfaces, which improves the collection efficiency for materials with diffusion lengths shorter than the device width [7]. The conversion efficiency of a double-junction cell should also be quite good for rear-surface illumination, which is important for module applications that use bifacial illumination of the cell [8].

The process sequence for an EWT cell is similar to a buried-contact cell. First, phosphorus is diffused to around 100 Ω/□ on the front surface for an EWT cell or on both surfaces for a double-junction EWT cell. Next, a dielectric layer is either grown (SiO_2) or deposited (Si_3N_4) on both surfaces. The n-type grooves and vias are next scribed and drilled with a laser; ideally, the grooves and vias are formed in a single step to ensure good alignment. The grooves and vias are subsequently etched, heavily diffused with phosphorus, and filled with metal by a selective process. For the selective metallization, buried-contact cells typically use electroless nickel sintered in forming gas for low contact resistance followed by electroless copper or electroplated silver for good conductance. The dielectric layer serves several functions in the buried-contact cell sequence: an etch stop during the groove etching, a diffusion mask during the groove diffusion, a plating mask during the metallization step, and the antireflection coating and surface passivation in the finished cell.

Several options exist for forming the interdigitated grid on the back to contact the p-type substrate. One option is to perform a patterned-aluminum alloy, possibly using an aligned screen-printed aluminum paste fired through the dielectric layer. A second option is to use a laser to scribe a second set of grooves and diffuse the grooves with boron. Note that the p-type aluminum alloy or boron diffusion could be performed either before or after the phosphorus groove diffusion. The p-type grid is plated with metal for low resistance at the same time as the n-type grooves and vias.

The high performance and potential cost effectiveness of the buried-contact cell arises from the following features: separate emitter and contact diffusions for high emitter efficiency, self alignment of the metallization with the groove diffusion, high aspect ratio for the gridline due to the groove, and to the several functions served by the dielectric layer [5]. The only difference in equipment between the EWT and buried-contact cells is the laser system; the laser system must be capable of drilling vias aligned to the scribed grooves with a minimum throughput of one 100-cm^2 sample per minute. For a typical via spacing of 1 mm and 10,000 vias per sample, the desired throughput corresponds to a drilling and sample (or laser beam) translation time less than 6 ms per via. We have identified commercial laser systems that are capable of drilling holes in silicon in a single pulse with a repetition rate greater than 1 kHz. The grooves can be scribed at the same time as the via drilling with a second laser collinear with the drilling laser or the grooves can be mechanically scribed in a separate step. In any case, commercial laser systems are available that meet our minimum throughput requirements.

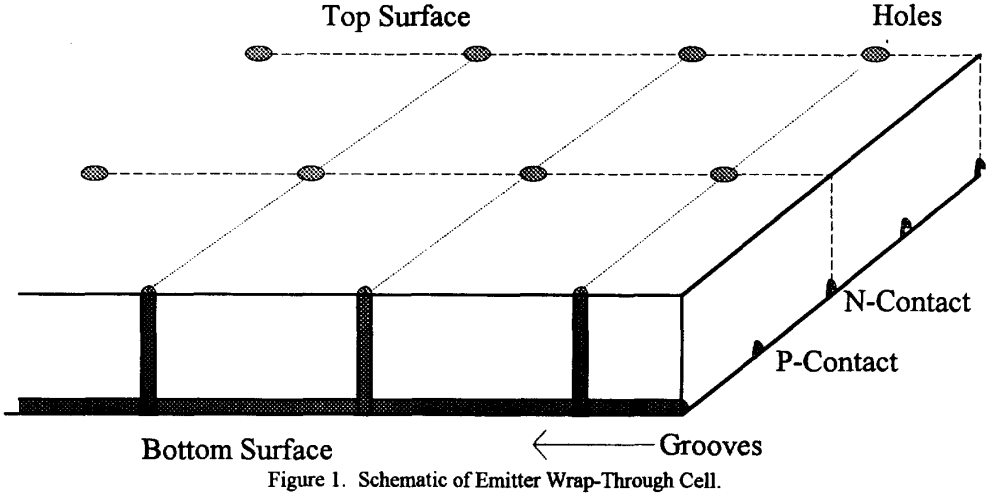

Figure 1. Schematic of Emitter Wrap-Through Cell.

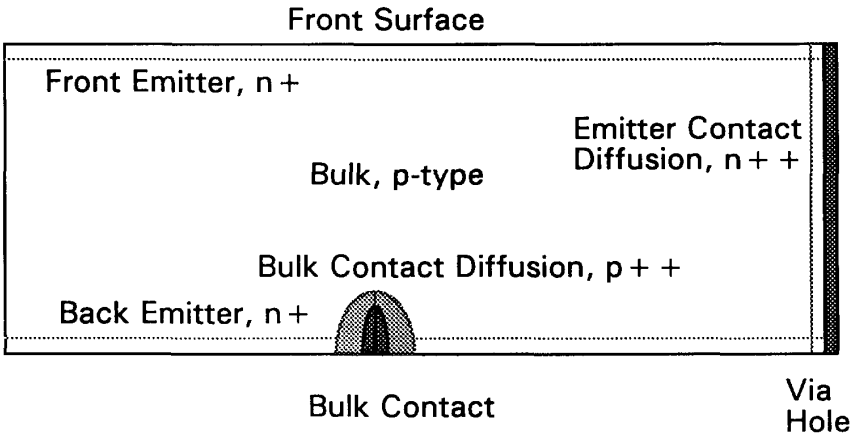

Figure 2. Schematic (side view) of Double-Junction Emitter Wrap-Through Cell

CELL DESIGN

We first develop a model for the series resistance of an EWT cell; the series resistance model is required for cell design and for device models to estimate EWT cell performance. Important resistance terms include emitter resistance (including spreading resistance as the current converges into the vias), via resistance (transport of current through the vias to the back surface), grid resistance, and base resistance. Important design parameters for series resistance include emitter sheet resistance, via diameter, groove and via spacing, and groove cross-sectional area. The important optimization parameter is the via and groove spacing; reducing the spacing reduces the series resistance but increases the time required for laser scribing and drilling.

We developed a model for the series resistance by dividing the cell geometry into regions with one-dimensional current flows. For calculation of the emitter spreading resistance, the model divides the emitter into circular "unit cells" with an area equivalent to the square collection area of each via [3]. Similarly, the model separates current flow in the base into regions of linear and cylindrical flow [9]. The grid resistance depends upon the geometry of the busbars. Figure 3 presents two possible configurations for the busbars with interdigitated back contacts. Adding more busbars reduces the grid resistance at the expense of increased complexity in the module assembly. Table 1 presents expressions for the series resistance components of an EWT cell.

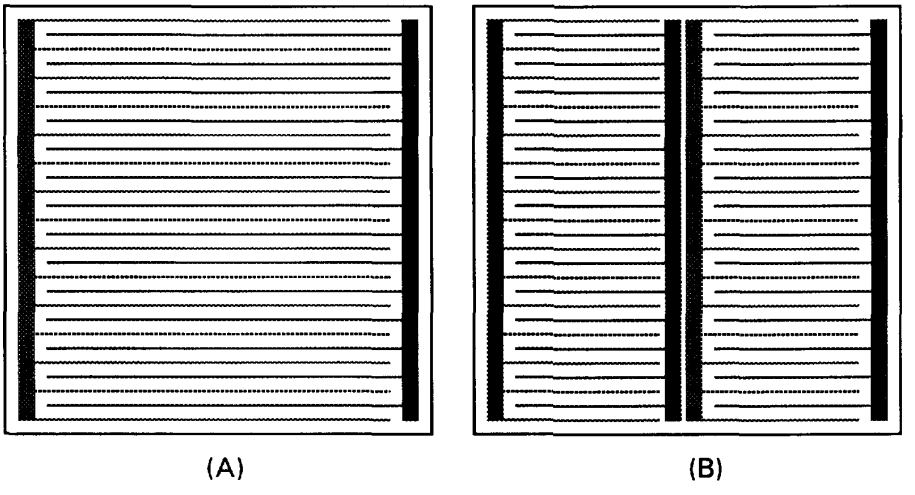

Figure 3. Two possible busbar arrangements for an interdigitated back-contact cell. (A) has a single busbar for each polarity on each end of the cell. Module assembly using this cell would be easy. (B) has an additional set of busbars in the center of the cell, which reduces the grid resistance by a factor of four compared to (A) at the expense of more complex module assembly.

$$R_e = \frac{\rho_e S^2}{2\pi}\left[\frac{1}{4}\left(1-r_c^4\right)-\left(1-r_c^2\right)-\ln(r_c)\right]$$

$$R_g = \frac{\rho_g S L^2}{3A_g}$$

$$R_b = \rho_b W\left[1+\frac{S}{W\pi}\left(\ln\left(\frac{S}{r_{bc}\pi}\right)-1\right)\right]$$

Table 1. Expressions for emitter, grid, and base resistance components (R_e, R_g, and R_b) in Ωcm^2 of an EWT cell. S is the groove and via spacing, L is the device length, ρ_e is the emitter sheet resistance, ρ_g is the grid resistivity, ρ_b is the base resistivity, A_g is the cross-sectional area of the gridline, W is the device width, r_c is the radius of the via divided by the radius of the unit cell, and r_{bc} is the radius of the p-type contact. The terms in backets for R_e and R_b represent the effect of current crowding in the emitter and 2-dimensional current flow in the base, respectively.

We calculated the series resistance of a 100-cm^2 EWT cell as a function of via diameter, via and groove spacing, and emitter sheet resistance. We used a cross-sectional area for the grid of 10,000 μm^2, a resistivity of 2 $\mu\Omega cm$ for the metal, a busbar at each end of the cell, and a base resistivity of 1 Ωcm. Figure 4 presents an example of these calculations. The two largest components of series resistance are due to the grid and the emitter. The emitter resistance is relatively high due to current crowding as the current converges on the via hole, so that the via diameter is an important parameter in the cell design. Note that the grid resistance would be negligible if we either assumed a larger cross-sectional area for the grid or used additional busbars in the design. A range of values for spacing, sheet resistance, and via diameter yield a series resistance of less than our target of 0.3 Ωcm^2.

We used a numerical one-dimensional semiconductor device modeling code (PC-1D) with a series resistance of 0.25 Ωcm^2 to estimate the cell performance of a 100-cm^2 EWT cell [10]. We used material parameters (e.g., base doping, lifetime, width, and surface type) appropriate for high-quality solar-grade Cz and multicrystalline silicon. Table 2 presents results of our calculations. The calculations show that efficiencies in excess of 21 and 18% are possible with solar-grade Cz and multicrystalline silicon EWT cells, respectively. The double-junction cell provides a performance enhancement of nearly 1% absolute for both materials compared to the front-junction cell. Note that these calculations overestimate the open-circuit voltage slightly because the one-dimensional device simulation ignored the contribution to recombination current of the diffused grooves on the rear surface.

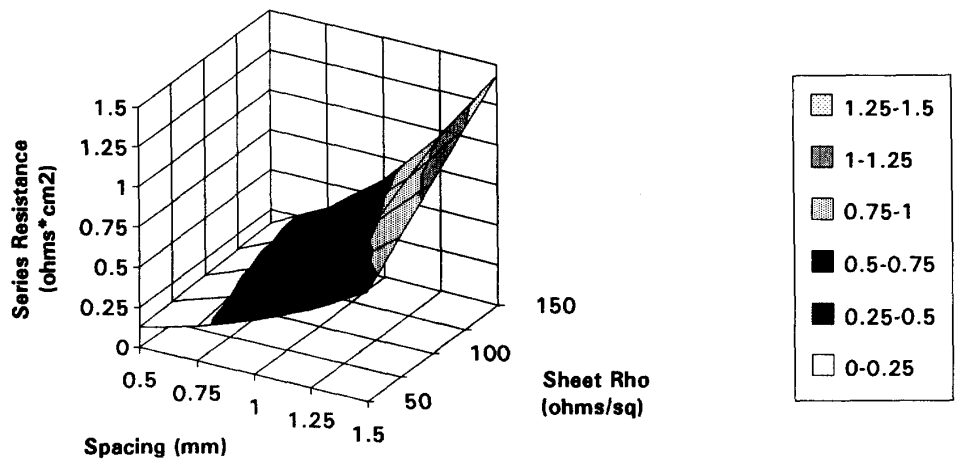

Figure 4. Calculated series resistance of EWT cell with a via diameter of 100 μm as a function of via and groove spacing and of emitter sheet resistance.

Parameter	Solar-Grade Cz		Multicrystalline	
	Front	Double	Front	Double
J_{sc} (mA/cm^2)	39.13	41.10	34.76	36.25
V_{oc} (mV)	636.0	638.6	608.3	607.9
FF	0.822	0.823	0.817	0.827
η (%)	20.5	21.6	17.3	18.0
τ_h (μs)	30		15	
ρ_h (Ωcm)	0.8		1.5	
Width (mm)	300		250	

Table 2. Results of EWT cell simulations using a series resistance of 0.25 Ωcm^2 and material parameters appropriate for solar-grade mono- and multicrystalline silicon. We used a textured surface with a fixed reflectance of 2% for simulations of the Cz cell and a planar surface with the modeled reflectance of a single-layer antireflection coating for simulations of the multicrystalline cell.

PROCESS DEVELOPMENT

Most of the processes required for fabrication of an EWT cell (e.g., multiple uses of a dielectric, groove formation, groove diffusion, metalization, etc.) have already been demonstrated by other groups for fabrication of buried-contact silicon solar cells. The new processes required for fabrication of an EWT cell include the following: laser drilling of the vias aligned to a laser-scribed groove, diffusion of phosphorus through the vias with low electrical resistance, and incorporation of boron diffusion or patterned aluminum alloy into the process sequence. Note that the EWT cell requires at least one alignment in the process sequence for the interdigitated n-type and p-type grids.

We have a pulsed (Q-switch) Nd:YAG (1.064 μm) laser-scribe system, which we have upgraded with a four-axis (x, y, z, and θ) sample stage and a computer-based control system [11]. The control system uses files from a CADD program for easy adjustment of patterns. Our laser system drills a via in less than 100 ms using a pulse energy of 0.5 mJ, a pulse width of 25 ns, and a pulse rate of 1 kHz. (Our laser has a low throughput for hole drilling because it does not have the appropriate pulse width and energy for drilling holes in a single pulse.) The grooves are scribed in one pass and the vias are drilled in a subsequent pass in immediate succession, so that the groove and vias are always aligned.

We also modified our system to accomodate alignment of different patterns. We found that mechanical alignment was not sufficient for alignment of the n-type and the p-type interdigitated grooves. The problem with mechanical alignment was rotational accuracy; the two patterns must be rotationally accurate to less than 0.6° for spacing of 1 mm and cell length of 10 cm. However, we found that we could manually align patterns with the aid of a HeNe alignment laser beam that is collinear with the laser-scribe beam.

We successfully demonstrated diffusion of phosphorus using PH_3 in the vias. We confirmed, by measuring the electrical resistance of the diffused vias, that the walls of the vias have approximately the same sheet resistance as the diffusion on a horizontal surface. This result means that the resistance of the vias, even without plating of metal into the vias, is negligible for an EWT cell. We have also found that metal (electroless nickel and electroplated silver) readily plates into and mostly fills the vias, which further reduces the via resistance.

A boron diffusion or an aluminum alloy is required for low contact resistance of the sintered nickel to the p-type base because solar-grade silicon typically has a resistivity of only about 1 Ωcm. A boron diffusion or aluminum-alloyed junction is also required for the double-junction EWT cell to counter dope the phosphorus emitter diffusion (Figure 2). We have demonstrated that evaporated aluminum can be alloyed through silicon nitride in a tube furnace at 1000°C in our laboratory. However, we are concentrating on developing an EWT process sequence with a boron diffusion and aligned interdigitated groove because we do not presently have a means in our laboratory to pattern evaporated aluminum over a grooved back surface.

Integration of boron diffusion into the process requires demonstration of several process-related items: the boron diffusion must be compatible with the silicon nitride, the boron diffusion in the grooves must be protected from the phosphorus groove diffusion, and the boron diffusion must be compatible with the metalization. (We use silicon nitride rather than silicon dioxide for the dielectric because silicon nitride is a better anti-reflection coating (higher refractive index), does not require a long furnace oxidation, is a better diffusion barrier, and is more easily integrated into the process due to compatibility with chemicals used for deglazing the diffusion glasses (HF) and for etching the grooves (KOH).) We have demonstrated all the boron-diffusion items individually. Boron diffusion using diborane gas (B_2H_6) does not interact strongly with silicon nitride, although there appears to be an interaction of the boron and phosphorus diffusions together with the silicon nitride. We confirmed that a 200-nm CVD oxide protects the boron diffusion from the phosphorus groove diffusion. We also demonstrated plating to boron-diffused grooves, although we have not yet measured the contact resistance. Table 3 presents our process sequence using a boron diffusion. We expect to have the full process integrated for fabrication of an EWT cell by the end of 1993.

Table 3. Process sequence for EWT cell.

Phosphorus emitter diffusion (100 Ω/sq).
Si_3N_4 deposition by LPCVD (100 nm).
Groove p-type grid.
KOH etch grooves.
B_2H_6 boron diffusion (approximately 50 Ω/sq).
CVD oxide (200 nm) on back surface.
Groove and drill n-type grid.
KOH etch grooves and vias.
PH_3 phosphorus diffusion to (approximately 10 Ω/sq).
Deglaze grooves and tune nitride to ARC.
Electroless nickel.
Sinter in forming gas, 500°C.
Electroplate silver.
Forming gas anneal, 400°C.

CONCLUSIONS

We described a new cell concept (EWT) that has the performance advantages of a back-contact cell, that can use materials with short diffusion lengths, and that uses a potentially cost-effective process sequence. We have demonstrated all the individual processes required for fabrication of an EWT cell. From our modeling, we believe that the EWT cell is capable of achieving efficiencies of 18 and 21% on large-area (100 cm^2) multi- and monocrystalline solar-grade silicon substrates, respectively.

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