ATtiny84A Ultra-36

Pure Software Bank Switching with Data Bus Interface

Left Pins		Right Pins	
(POWER) **VCC**	1	14	**GND** (GROUND)
(Data Bus D4) **PB0**	2	13	**PA0** (A15 - Bit 0)
($D700 Trap) **PB1**	3	12	**PA1** (A16 - Bit 1)
(RESET Sense) **PB3**	4	11	**PA2** (A17 - Bit 2)
(JiffyDOS Toggle) **PB2**	5	10	**PA3** (A18 - Bit 3)
(Data Bus D0) **PA7**	6	9	**PA4** (Data Bus D3)
(Data Bus D1) **PA6**	7	8	**PA5** (Data Bus D2)

Legend: Power · Ground · Bank Output · Control Input · Data Bus · Programming
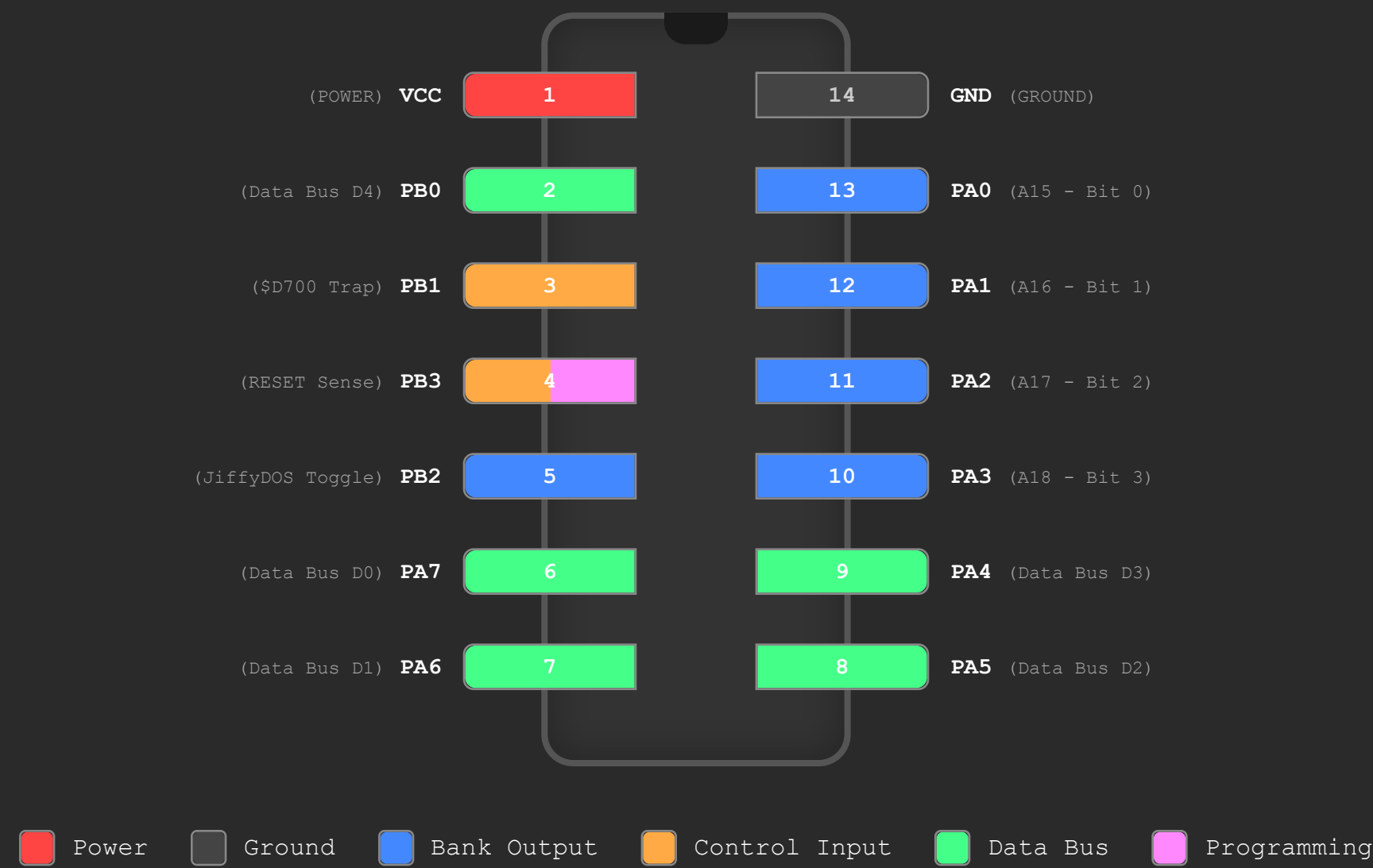
Flash Memory Support

SST39SF020A: 256KB = 8 banks (uses A15-A17, A18 unused)
SST39SF040: 512KB = 16 banks (uses A15-A18)
Bank Detection: Menu program determines flash type automatically
Data Protocol: D0-D3 = Bank (0-15), D4 = JiffyDOS enable

External Connections

$D700 Trap: Pin 3 (PB1) connects to U3 Pin 12
Reset Monitor: Pin 4 (PB3) connects to System Reset
Data Bus: Pins 2,6,7,8,9 connect to U36 socket D0-D4
JiffyDOS Control: Pin 5 (PB2) controls JiffyDOS enable

ISP Programming (if needed)

VCC: Pin 1 - Power (3.3V or 5V)
GND: Pin 14 - Ground
RESET: Pin 4 (PB3) - Reset/Programming enable
Note: Data bus pins can be used for programming when not in normal operation