

# NLAS4684

## Analog Switch, Dual SPDT, Ultra-Low Resistance

The NLAS4684 is an advanced CMOS analog switch fabricated in Sub-micron silicon gate CMOS technology. The device is a dual Independent Single Pole Double Throw (SPDT) switch featuring Ultra-Low  $R_{ON}$  of  $0.5\ \Omega$ , for the Normally Closed (NC) switch, and  $0.8\ \Omega$  for the Normally Opened switch (NO) at 2.7 V.

The part also features guaranteed Break Before Make switching, assuring the switches never short the driver.

The NLAS4684 is available in a 2.0 x 1.5 mm bumped die array. The pitch of the solder bumps is 0.5 mm for easy handling.

### Features

- Ultra-Low  $R_{ON}$ ,  $< 0.5\ \Omega$  at 2.7 V
- Threshold Adjusted to Function with 1.8 V Control at  $V_{CC} = 2.7\text{--}3.3\text{ V}$
- Single Supply Operation from 1.8–5.5 V
- Tiny 2 x 1.5 mm Bumped Die
- Low Crosstalk,  $< 83\text{ dB}$  at 100 kHz
- Full  $0\text{--}V_{CC}$  Signal Handling Capability
- High Isolation,  $-65\text{ dB}$  at 100 kHz
- Low Standby Current,  $< 50\text{ nA}$
- Low Distortion,  $< 0.14\%$  THD
- $R_{ON}$  Flatness of  $0.15\ \Omega$
- Pin for Pin Replacement for MAX4684
- High Continuous Current Capability  
 $\pm 300\text{ mA}$  Through Each Switch
- Large Current Clamping Diodes at Analog Inputs  
 $\pm 300\text{ mA}$  Continuous Current Capability
- Pb-Free Packages are Available

### Applications

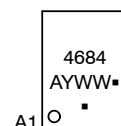
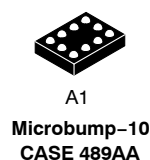
- Cell Phone
- Speaker Switching
- Power Switching
- Modems
- Automotive



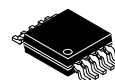
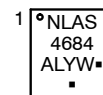
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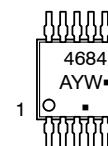
### MARKING DIAGRAMS



DFN10  
CASE 485C



Micro10  
CASE 846B



A = Assembly Location  
L = Wafer Lot  
Y = Year  
WW, W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

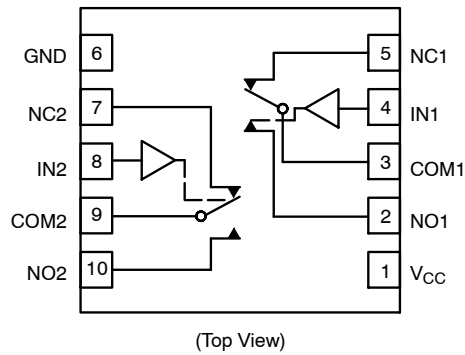
### FUNCTION TABLE

IN 1, 2	NO 1, 2	NC 1, 2
0	OFF	ON
1	ON	OFF

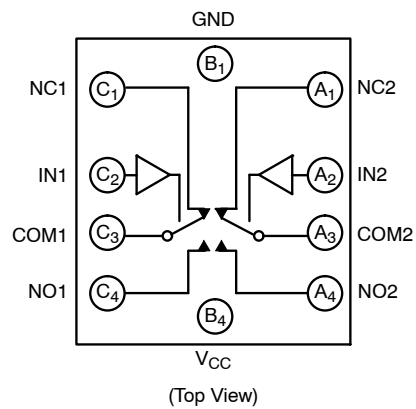
### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

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**Figure 1. Pin Connections and Logic Diagram (DFN10 and Micro10)**



**Figure 2. Pin Connections and Logic Diagram (Microbump-10)**

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### MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Positive DC Supply Voltage	$-0.5$ to $+7.0$	V
$V_{IS}$	Analog Input Voltage ( $V_{NO}$ , $V_{NC}$ , or $V_{COM}$ )	$-0.5 \leq V_{IS} \leq V_{CC} + 0.5$	V
$V_{IN}$	Digital Select Input Voltage	$-0.5 \leq V_I \leq +7.0$	V
$I_{anI1}$	Continuous DC Current from COM to NC/NO	$\pm 300$	mA
$I_{anI-pk\ 1}$	Peak Current from COM to NC/NO, 10 duty cycle (Note 1)	$\pm 500$	mA
$I_{clmp}$	Continuous DC Current into COM/NO/NC	$\pm 300$	mA
$I_{clmp\ 1}$	Peak Current into Input Clamp Diodes at COM/NC/NO	$\pm 500$	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Defined as 10% ON, 90% off duty cycle.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage	1.8	5.5	V
$V_{IN}$	Digital Select Input Voltage	GND	5.5	V
$V_{IS}$	Analog Input Voltage (NC, NO, COM)	GND	$V_{CC}$	V
$T_A$	Operating Temperature Range	$-55$	$+125$	$^{\circ}\text{C}$
$t_r, t_f$	Input Rise or Fall Time, SELECT $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$	0 0	100 20	ns/V
ESD	Human Body Model – All Pins		5	kV

### DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	$V_{CC} \pm 10\%$	Guaranteed Limit			Unit
				$-55^{\circ}\text{C}$ to $25^{\circ}\text{C}$	$<85^{\circ}\text{C}$	$<125^{\circ}\text{C}$	
$V_{IH}$	Minimum High-Level Input Voltage, Select Inputs (Figure 9)		2.0	1.4	1.4	1.4	V
			2.5	1.4	1.4	1.4	
			3.0	1.4	1.4	1.4	
			5.0	2.0	2.0	2.0	
$V_{IL}$	Maximum Low-Level Input Voltage, Select Inputs (Figure 9)		2.0	0.5	0.5	0.5	V
			2.5	0.5	0.5	0.5	
			3.0	0.5	0.5	0.5	
			5.0	0.8	0.8	0.8	
$I_{IN}$	Maximum Input Leakage Current, Select Inputs	$V_{IN} = 5.5\text{ V}$ or GND	5.5	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
$I_{OFF}$	Power Off Leakage Current	$V_{IN} = 5.5\text{ V}$ or GND	0	$\pm 10$	$\pm 10$	$\pm 10$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current (Note 2)	Select and $V_{IS} = V_{CC}$ or GND	5.5	$\pm 180$	$\pm 200$	$\pm 200$	nA

2. Guaranteed by design.

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## DC ELECTRICAL CHARACTERISTICS – Analog Section

Symbol	Parameter	Condition	V <sub>CC</sub> ± 10%	Guaranteed Maximum Limit						Unit
				–55°C to 25°C		< 85°C		< 125°C		
				Min	Max	Min	Max	Min	Max	
R <sub>ON</sub> (NC)	NC “ON” Resistance (Note 3)	V <sub>IN</sub> ≤ V <sub>IL</sub>	2.5		0.6		0.7		0.8	Ω
		V <sub>IS</sub> = GND to V <sub>CC</sub>	3.0		0.5		0.5		0.5	
		I <sub>IN</sub>   ≤ 100 mA	5.0		0.4		0.4		0.5	
R <sub>ON</sub> (NO)	NO “ON” Resistance (Note 3)	V <sub>IN</sub> ≥ V <sub>IH</sub>	2.5		1.0		1.0		1.0	Ω
		V <sub>IS</sub> = GND to V <sub>CC</sub>	3.0		0.8		0.8		1.0	
		I <sub>IN</sub>   ≤ 100 mA	5.0		0.8		0.8		0.9	
R <sub>FLAT</sub> (NC)	NC_On–Resistance Flatness (Notes 3, 5)	I <sub>COM</sub> = 100 mA	2.5		0.15		0.15		0.15	Ω
		V <sub>IS</sub> = 0 to V <sub>CC</sub>	3.0		0.15		0.15		0.15	
			5.0		0.15		0.15		0.15	
R <sub>FLAT</sub> (NO)	NO_On–Resistance Flatness (Notes 3, 5)	I <sub>COM</sub> = 100 mA	2.5		0.35		0.35		0.35	Ω
		V <sub>IS</sub> = 0 to V <sub>CC</sub>	3.0		0.35		0.35		0.35	
			5.0		0.35		0.35		0.35	
ΔR <sub>ON</sub>	On–Resistance Match Between Channels (Notes 3 and 4)	V <sub>IS</sub> = 1.3 V; I <sub>COM</sub> = 100 mA	2.5		0.18		0.18		0.18	Ω
		V <sub>IS</sub> = 1.5 V; I <sub>COM</sub> = 100 mA	3.0		0.06		0.06		0.06	
		V <sub>IS</sub> = 2.8 V; I <sub>COM</sub> = 100 mA	5.0		0.06		0.06		0.06	
I <sub>NC(OFF)</sub> I <sub>NO(OFF)</sub>	NC or NO Off Leakage Current (Figure 13) (Note 3)	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>NO</sub> or V <sub>NC</sub> = 1.0 V <sub>COM</sub> = 4.5 V	5.5	–1	1	–10	10	–100	100	nA
I <sub>COM(ON)</sub>	COM ON Leakage Current (Figure 13) (Note 3)	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>NO</sub> 1.0 V or 4.5 V with V <sub>NC</sub> floating or V <sub>NC</sub> 1.0 V or 4.5 V with V <sub>NO</sub> floating V <sub>COM</sub> = 1.0 V or 4.5 V	5.5	–2	2	–20	20	–200	200	nA

3. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.

4.  $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$  between NC1 and NC2 or between NO1 and NO2.

5. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

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### AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns) (Typical characteristics are at 25°C)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> (V)	V <sub>IS</sub> (V)	Guaranteed Maximum Limit						Unit	
					– 55°C to 25°C			< 85°C		< 125°C		
					Min	Typ	Max	Min	Max	Min		Max
t <sub>ON</sub>	Turn-On Time	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF (Figures 4 and 5)	2.5 3.0 5.0	1.3 1.5 2.8			60 50 30		70 60 35		70 60 35	ns
t <sub>OFF</sub>	Turn-Off Time	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF (Figures 4 and 5)	2.5 3.0 5.0	1.3 1.5 2.8			50 40 30		55 50 35		55 50 35	ns
t <sub>BBM</sub>	Minimum Break-Before-Make Time (Note 6)	V <sub>IS</sub> = 3.0 R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF (Figure 3)	3.0	1.5	2	15						ns

C <sub>NC</sub> Off C <sub>NO</sub> Off C <sub>NC</sub> On C <sub>NO</sub> On	NC Off Capacitance, f = 1 MHz NO Off Capacitance, f = 1 MHz NC On Capacitance, f = 1 MHz NO On Capacitance, f = 1 MHz	Typical @ 25, V <sub>CC</sub> = 5.0 V						pF
		102						
		104						
		322						
		330						

### ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Condition	$V_{CC}$ V	Typical	Unit
				25°C	
BW	Maximum On-Channel –3dB Bandwidth or Minimum Frequency Response	$V_{IN} = 0\ \text{dBm}$ NC	3.0	6.5	MHz
		$V_{IN}$ centered between $V_{CC}$ and GND (Figure 6) NO	3.0	9.5	
$V_{ONL}$	Maximum Feed-through On Loss	$V_{IN} = 0\ \text{dBm}$ @ 100 kHz to 50 MHz $V_{IN}$ centered between $V_{CC}$ and GND (Figure 6)	3.0	–0.05	dB
$V_{ISO}$	Off-Channel Isolation (Note 7)	$f = 100\ \text{kHz}$ ; $V_{IS} = 1\ \text{V RMS}$ ; $C_L = 5\ \text{nF}$ $V_{IN}$ centered between $V_{CC}$ and GND (Figure 6)	3.0	–65	dB
Q	Charge Injection Select Input to Common I/O (Figures 10 and 11)	$V_{IN} = V_{CC}$ to GND, $R_{IS} = 0\ \Omega$ , $C_L = 1\ \text{nF}$ $Q = C_L - \Delta V_{OUT}$ (Figure 7)	3.0	15	pC
THD	Total Harmonic Distortion THD + Noise (Figure 9)	$F_{IS} = 20\ \text{Hz}$ to 100 kHz, $R_L = R_{gen} = 600\ \Omega$ , $C_L = 50\ \text{pF}$ $V_{IS} = 1\ \text{V RMS}$	3.0	0.14	%
VCT	Channel-to-Channel Crosstalk	$f = 100\ \text{kHz}$ ; $V_{IS} = 1\ \text{V RMS}$ , $C_L = 5\ \text{pF}$ , $R_L = 50\ \Omega$ $V_{IN}$ centered between $V_{CC}$ and GND (Figure 6)	3.0	–83	dB

6. –55°C specifications are guaranteed by design.

7. Off-Channel Isolation =  $20\log_{10}(V_{com}/V_{no})$  (See Figure 6).

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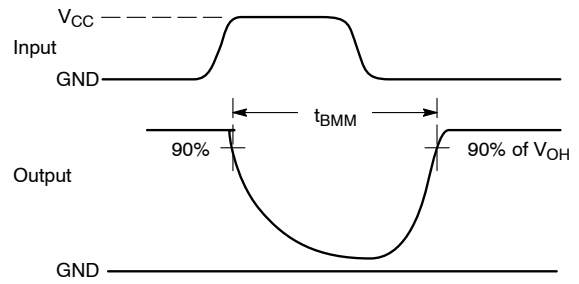
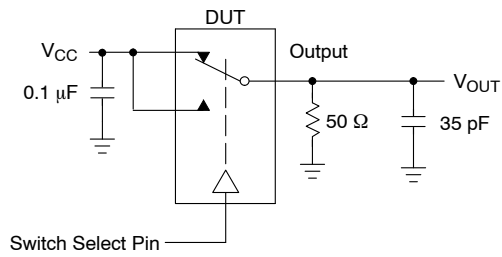


Figure 3.  $t_{BMM}$  (Time Break-Before-Make)

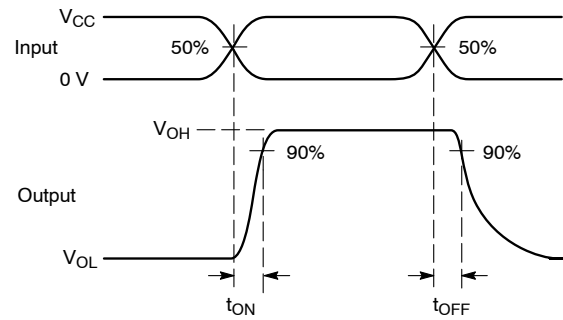
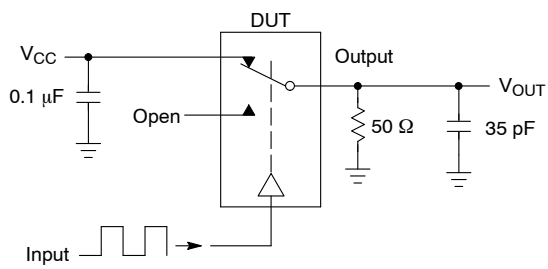


Figure 4.  $t_{ON}/t_{OFF}$

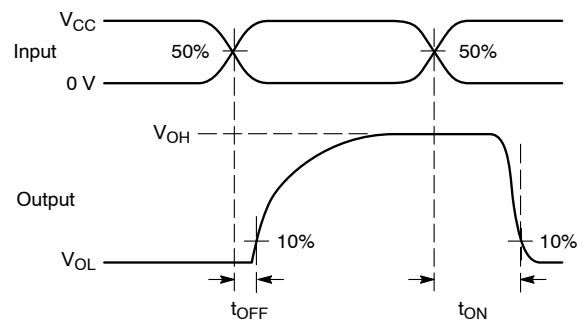
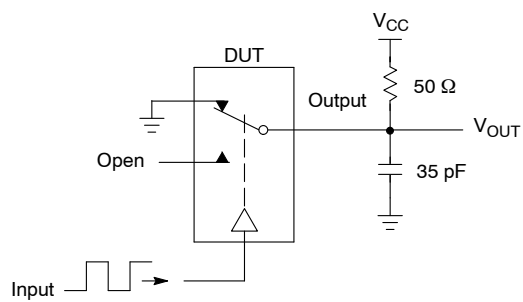
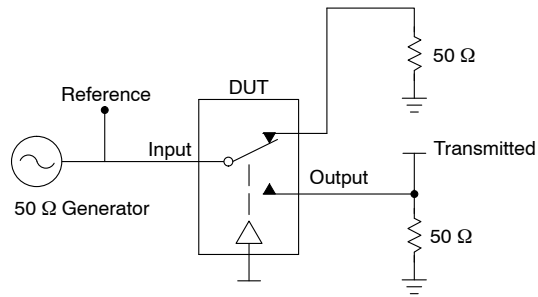


Figure 5.  $t_{ON}/t_{OFF}$

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Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch.  $V_{ISO}$ , Bandwidth and  $V_{ONL}$  are independent of the input signal direction.

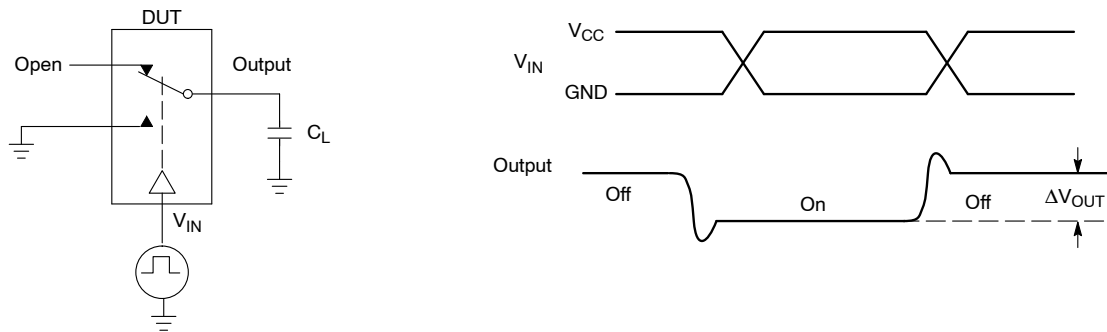
$$V_{ISO} = \text{Off Channel Isolation} = 20 \log \left( \frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \log \left( \frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

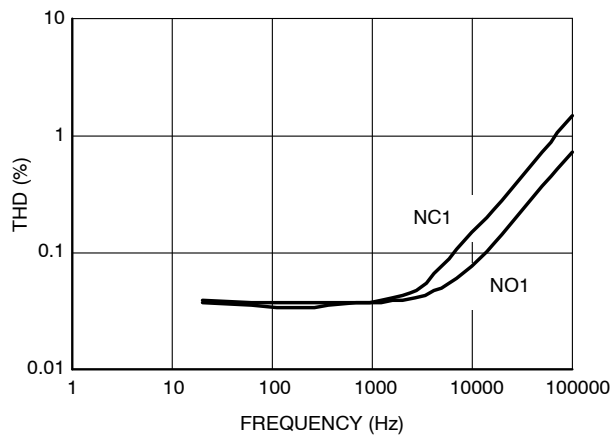
Bandwidth (BW) = the frequency 3 dB below  $V_{ONL}$

$V_{CT}$  = Use  $V_{ISO}$  setup and test to all other switch analog input/outputs terminated with 50 Ω

**Figure 6. Off Channel Isolation/On Channel Loss (BW)/Crosstalk  
(On Channel to Off Channel)/ $V_{ONL}$**



**Figure 7. Charge Injection: (Q)**



**Figure 8. Total Harmonic Distortion Plus Noise Versus Frequency**

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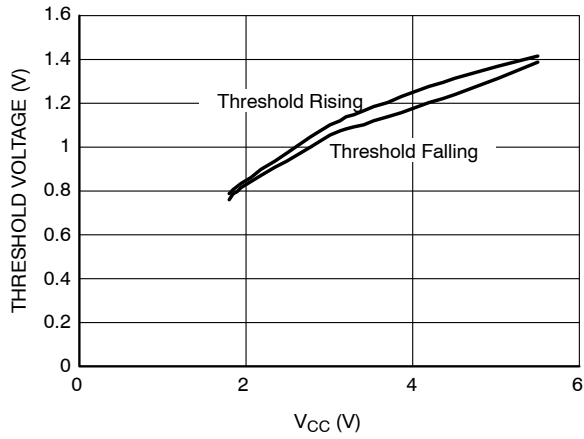


Figure 9. Voltage in Threshold on Logic Pins

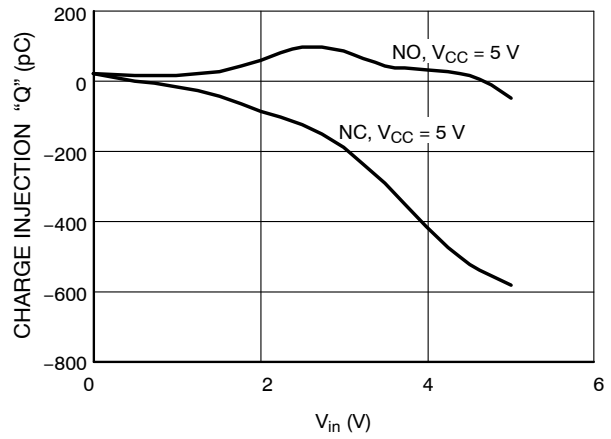


Figure 10. Charge Injection versus  $V_{IS}$

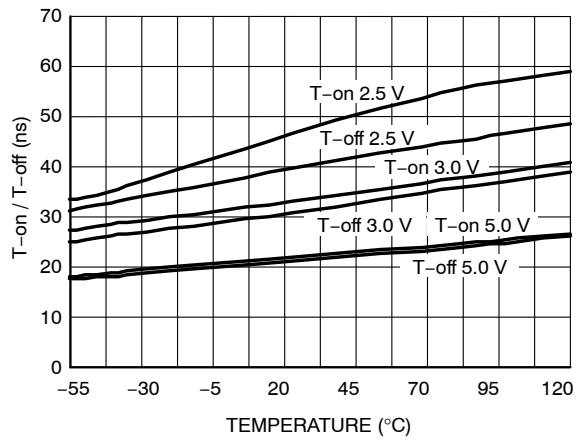


Figure 11. T-on / T-off Time versus Temperature

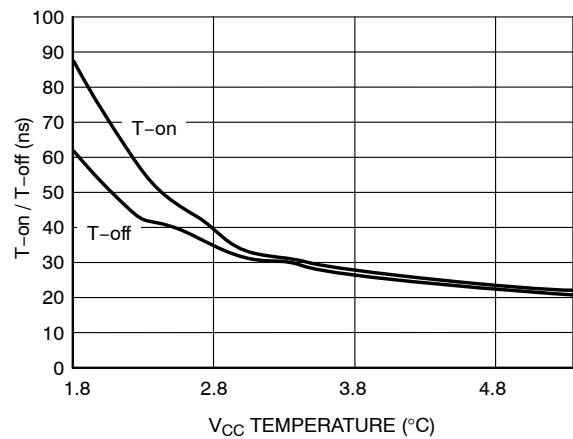


Figure 12. T-on / T-off Time versus Temperature

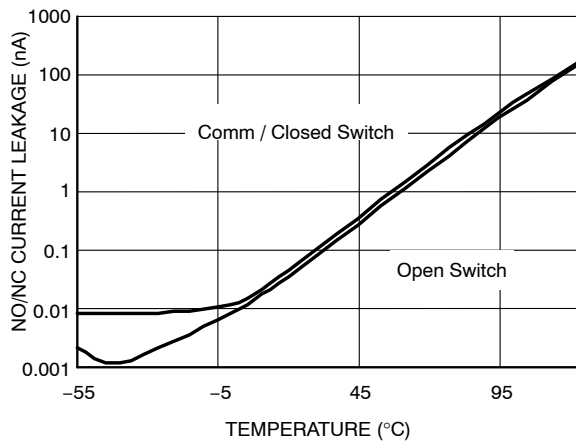


Figure 13. NO/NC Current Leakage Off and On,  $V_{CC} = 5 V$

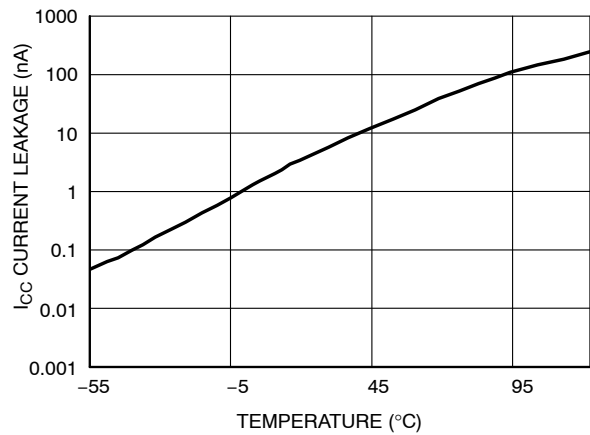


Figure 14.  $I_{CC}$  Current Leakage versus Temperature  $V_{CC} = 5.5 V$



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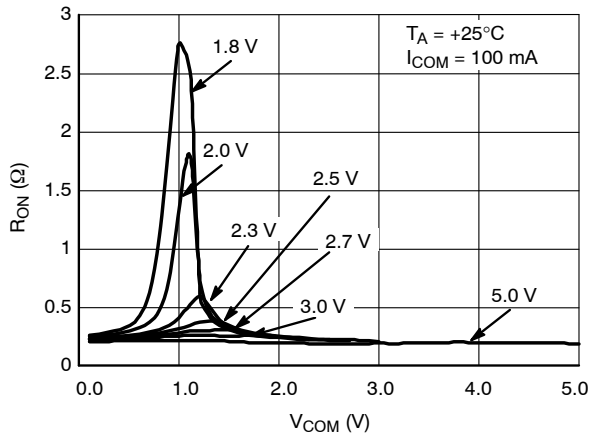


Figure 15. NC On-Resistance versus COM Voltage

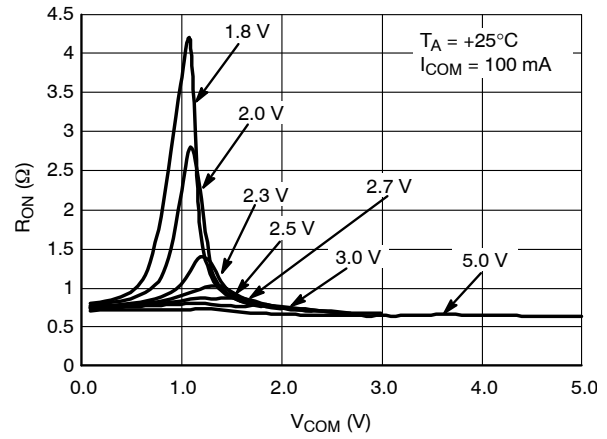


Figure 16. NO On-Resistance versus COM Voltage

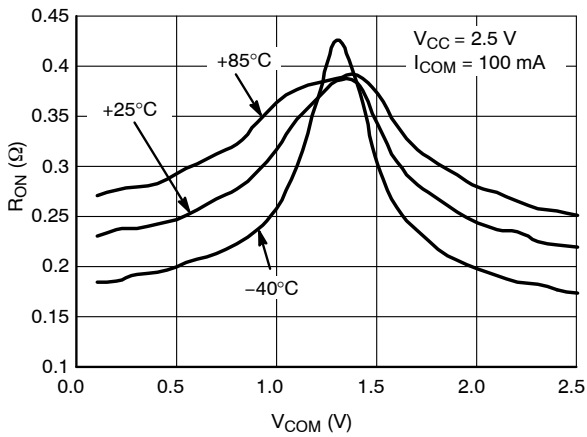


Figure 17. NC On-Resistance versus COM Voltage

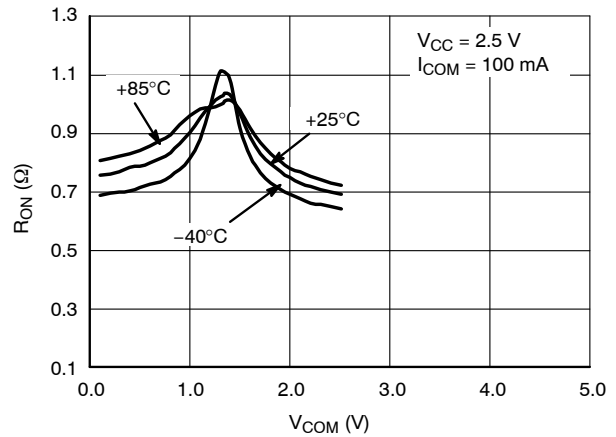


Figure 18. NO On-Resistance versus COM Voltage

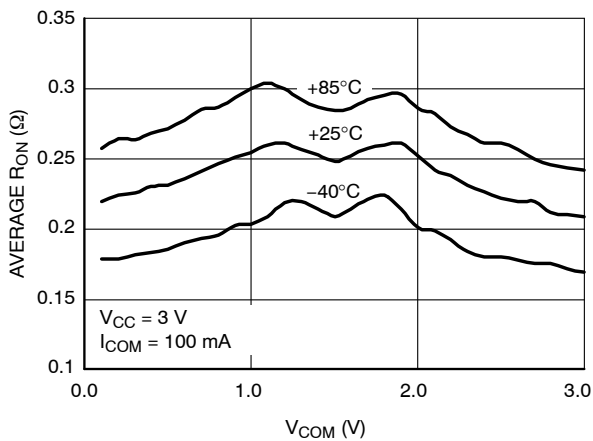


Figure 19. NC On-Resistance versus COM Voltage

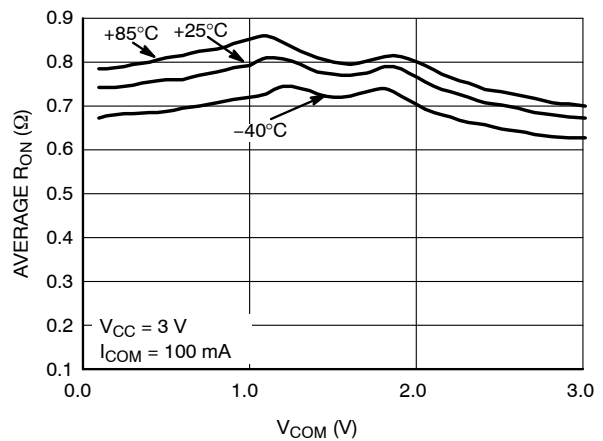
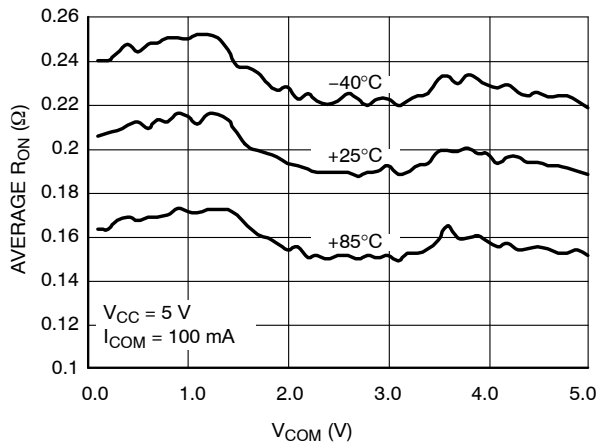
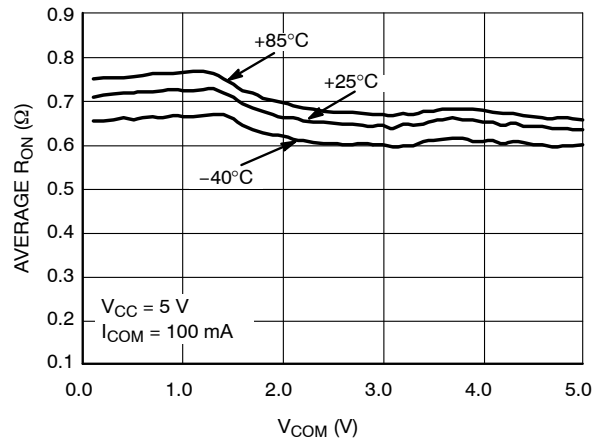


Figure 20. NC On-Resistance versus COM Voltage

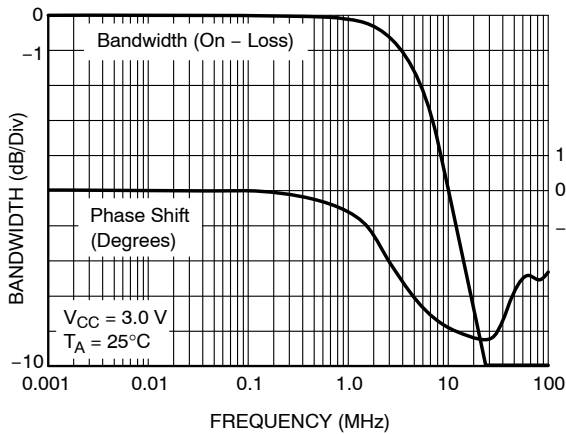
## NLAS4684



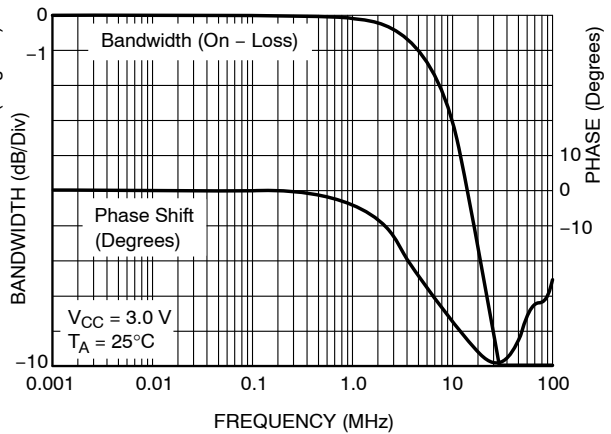
**Figure 21. NC On-Resistance versus COM Voltage**



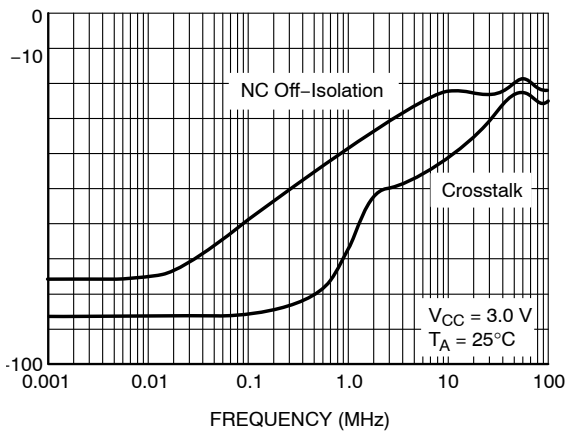
**Figure 22. NO On-Resistance versus COM Voltage**



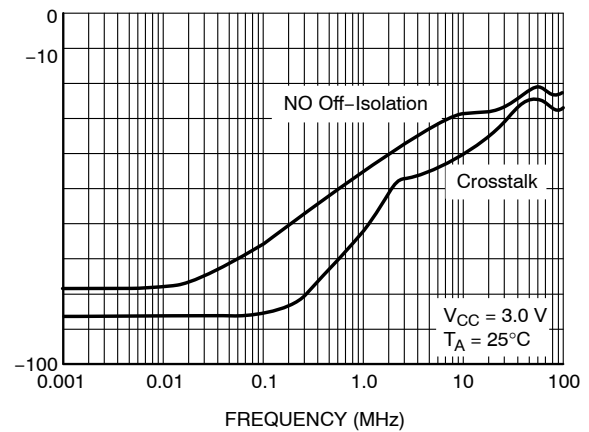
**Figure 23. NC Bandwidth and Phase Shift versus Frequency**



**Figure 24. NO Bandwidth and Phase Shift versus Frequency**



**Figure 25. NC Off Isolation and Crosstalk**



**Figure 26. NO Off Isolation and Crosstalk**

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### ORDERING INFORMATION

Device	Package	Shipping†
NLAS4684FCT1	Microbump-10	3000 / Tape & Reel
NLAS4684FCT1G	Microbump-10 (Pb-Free)	3000 / Tape & Reel
NLAS4684FCTCG	Microbump-10 (Pb-Free)	3000 / Tape & Reel
NLAS4684MNR2	DFN10	3000 / Tape & Reel
NLAS4684MNR2G	DFN10 (Pb-Free)	3000 / Tape & Reel
NLAS4684MR2	Micro10	4000 / Tape & Reel
NLAS4684MR2G	Micro10 (Pb-Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

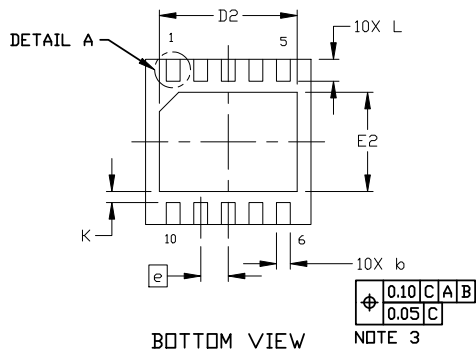
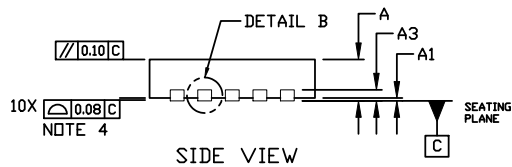
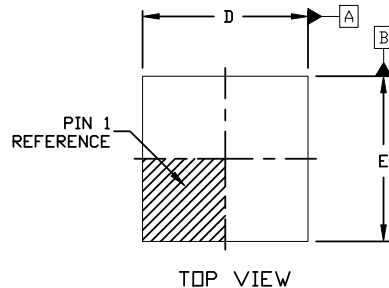
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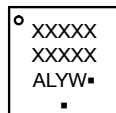
SCALE 2:1

DFN10, 3x3, 0.5P  
CASE 485C  
ISSUE F

DATE 16 DEC 2021



## GENERIC MARKING DIAGRAM\*



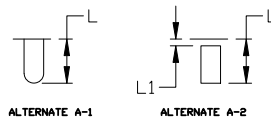
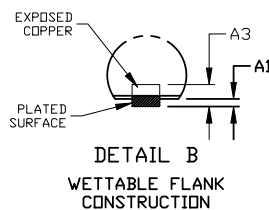
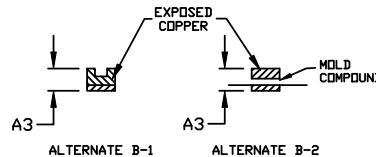
XXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

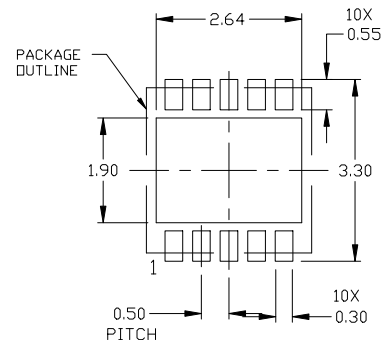
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

## NOTES:

1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION  $b$  APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL  $b$  MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3	0.20 REF		
b	0.18	0.23	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e	0.50 BSC		
K	0.20 REF		
L	0.30	0.40	0.50
L1	---	---	0.03



## RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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DESCRIPTION:	DFN10, 3X3 MM, 0.5 MM PITCH	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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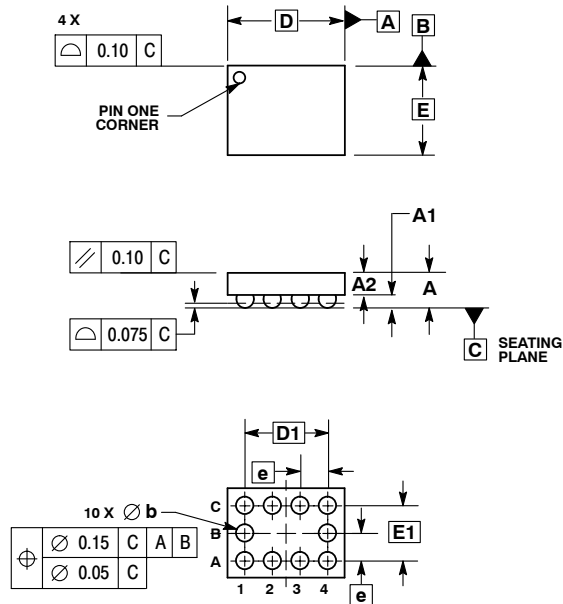


## 10 PIN FLIP-CHIP CASE 489AA-01 ISSUE A

DATE 04 MAY 2004



SCALE 4:1

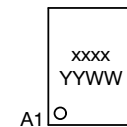


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS	
	MIN	MAX
A	---	0.650
A1	0.210	0.270
A2	0.280	0.380
D	1.965 BSC	
E	1.465 BSC	
b	0.250	0.350
e	0.500 BSC	
D1	1.500 BSC	
E1	1.000 BSC	

### GENERIC MARKING DIAGRAM\*



xxxx = Specific Device Code  
YY = Year  
WW = Work Week

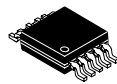
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DESCRIPTION:	10 PIN FLIP-CHIP	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

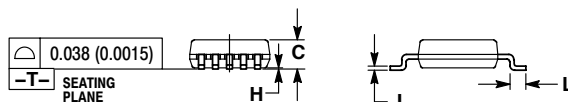
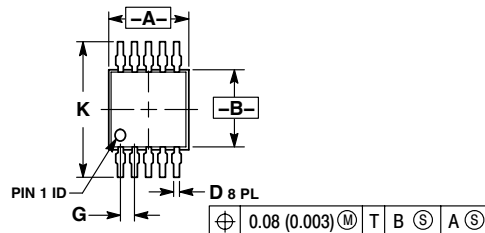
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SCALE 2:1

**Micro10**  
CASE 846B-03  
ISSUE D

DATE 07 DEC 2004

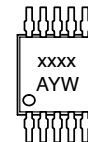


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846B-01 OBSOLETE. NEW STANDARD 846B-02

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.95	1.10	0.037	0.043
D	0.20	0.30	0.008	0.012
G	0.50 BSC		0.020 BSC	
H	0.05	0.15	0.002	0.006
J	0.10	0.21	0.004	0.008
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

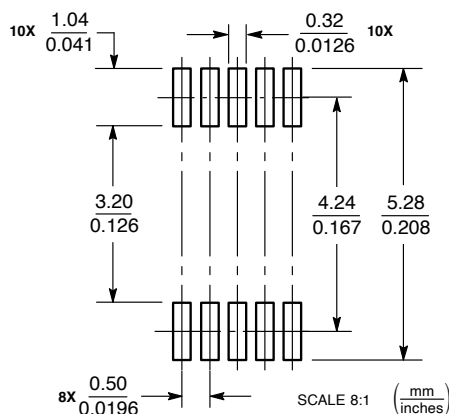
## GENERIC MARKING DIAGRAM\*



xxxx = Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.


## SOLDERING FOOTPRINT



Micro10

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STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	Micro10	PAGE 1 OF 2

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