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Improved VLSI architecture for triangular windowed sliding DFT based on CORDIC algorithm

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Abstract: This study presents a very-large-scale integration (VLSI) architecture for the triangular windowed sliding discrete Fourier transform (SDFT) based on COordinate rotation DIgital computer (CORDIC) algorithm. In the literature, the triangular windowed SDFT is obtained by direct cascading of two SDFT modules, whereas the idea of direct cascading leads to the error in the odd bins of the spectrum. The proposed architecture is modified to provide the correct outputs with a high-throughput rate compared to the existing designs. The SDFT has a recursive structure, and therefore it accumulates the error over iterations as the computation proceeds. A refreshing mechanism is utilised to limit the inaccuracy at the final output. The concept of generalised architecture as an area efficient implementation for obtaining more number of discrete Fourier transform (DFT) bins is introduced. An architecture is implemented using Verilog HDL on FPGA as well as in ASIC platform, and its arithmetic verification is performed in MATLAB.

1 Introduction

The discrete Fourier transform (DFT) is an indispensable tool known in the field of digital signal processing and is utilised to evaluate the spectrum of a finite discrete data sequence of real or complex numbers. For the real-time spectrum analysis, the sliding DFT (SDFT) estimates the spectrum recursively on a sample-by-sample basis; therefore it reacts to the instantaneous change in the incoming signal. The SDFT also provides economy in the computation of a DFT bin compared to other algorithms [1]. The SDFT may find its real-time applications in biomedical, speech recognition, communications, and so forth.

The SDFT leads to the computation of the DFT, in which the data window is intended to be sliding over a semi-infinite sequence. In the existing literature, we find two conventions of indexing the sequence while calculating the SDFT as depicted in Fig. 1, one with increasing time indices [1], and the other with decreasing time indices [2, 3]. The former method is the most standard one. For simplicity, we call the former method as type-1 sliding windowing, and the other as type-2 sliding windowing. On comparing, we find that the type-1 and the type-2 sliding window transforms have equal magnitude with different phases. The SDFT algorithms described in this paper are of type-1 unless otherwise stated.

The problem occurs if the input signal frequency does not exactly lie in the fixed frequency bins of the DFT spectrum, the signal power will spread over the adjacent bins, and this causes the spectral leakage. This means that there should be complete cycles of the input signal within the observation window to have leakage free spectrum. However, it is impossible to know a priori the exact frequency and the phase of the captured window of a real-time signal, and hence spectral leakage is unavoidable [4]. The windowing (by some known non-rectangular functions) is the remedy to reduce leakage to some extent. There are different types of window functions like triangular, Hann, Hamming, Blackman, and so on. By applying these windows, the main-lobe width of the spectrum increases, and the side-lobes get reduced [5]. In the existing literature, there are methods for implementing windows in the time domain [6–8], as well as in the frequency domain [1, 9]. Recently, we have presented an SDFT design integrated with the Hann windowing based on COordinate rotation DIgital computer (CORDIC) algorithm in [10].

Jacobson and Lyons [1] reported a sliding Goertzel DFT algorithm of type-1 with less computational workload than the SDFT algorithm. Duda [11] presented a modulated SDFT (mSDFT) algorithm of type-1 with more accuracy and stability than the SDFT algorithm. Gudovskiy and Chu [12] also reported a cascaded integrator-comb (CIC)-SDFT based on the mSDFT algorithm and the CIC filter. Recently, a CORDIC-based high throughput SDFT design based on the mSDFT algorithm of type-1 is proposed in [13].

Park [14] proposed the hopping SDFT (HDFT) to reduce the computational workload by calculating the spectrum after every L input samples. Wang *et al.* [15] proposed a modulated HDFT algorithm to reduce the computational workload further. Juang *et al.* [16] proposed the recursive HDFT algorithm based on the recursive implementation of update vector transform (UVT) inside HDFT to reduce the complexity. The feedback structure of these hopping algorithms contains L delays, and therefore the process of spectrum calculation is slow. Further, Park [17, 18] proposed

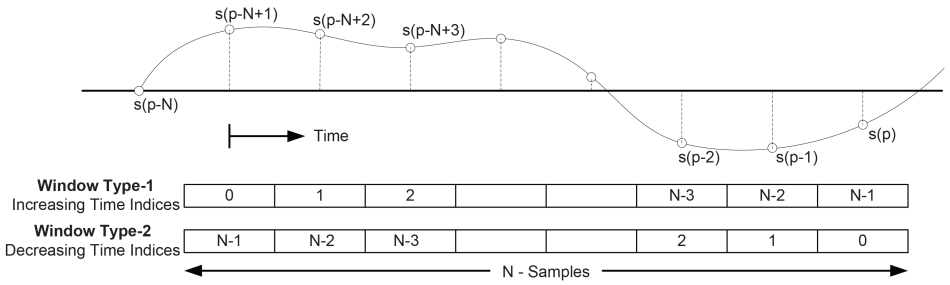

Fig. 1 *Different conventions of time indices for sliding windows containing N-samples of a real-time sequence*

generalised versions of HDFT as generalised SDFT (gSDFT) and optimal SDFT (oSDFT) algorithms. The problem with the gSDFT and the oSDFT is that for a single bin also these algorithms need to compute all the butterflies of its UVT related to the particular output bin, which is not required in other SDFT algorithms.

In the SDFT algorithm, the truncation error is involved in the fixed-point arithmetic, and therefore, the design accumulates error in the recursive architecture as the computation proceeds. Farhang-Boroujeny [2] developed the non-recursive architectures for the type-2 SDFT expression. In fact, a refreshing mechanism is expected in the recursive SDFT designs, which can limit the accumulation of truncation error [19].

Gronczynski [3] developed the type-2 SDFT algorithm with integrated triangular windowing using two component filters in cascade. Arneson [20] proposed the type-1 SDFT structure integrated with triangular windowing by direct cascading two SDFT structures. Gudovskiy and Chu [12] also reported a CIC-SDFT filter structure with integrated windowing by cascading two SDFT structures. We find that the direct cascading of two SDFT blocks does not provide the exact triangular windowed SDFT transfer function and this introduces error in the evaluation of all the odd bins in the spectrum. Wang [21] proposed an algorithm to evaluate time-dependent Fourier transform with generalised triangular function including Bartlett and Welch windows. The digital filter thus proposed in [21] is type-1 and marginally stable.

In this paper, we have derived the algorithm for triangular windowed SDFT based on the data-window of type-1 with growing time indices. We have applied the modulation property over the second-order recursive transfer function of triangular windowed SDFT and proposed the desired design with less error. To get the bounded error accumulation, we have implemented a refreshing mechanism. The existing methods are developed to get a single bin output, whereas the proposed architecture may evaluate several spectral bins.

The rest of the paper is organised as follows. In Section 2, we explain the theory of two different cases of the SDFT algorithms and accordingly triangular windowing is integrated with the SDFT structures. The four types of the triangular windowed SDFT designs are compared. The best design is chosen among these four structures and is proposed based on CORDIC with the refreshing mechanism, and its timing diagram is provided in Section 3. In Section 4, the truncation error of the proposed architecture is evaluated. Section 5 presents the simulation and the synthesis results based on FPGA and ASIC implementation; and finally, Section 6 concludes this paper.

2 Theory

In this section, we will explain the derivation of the SDFT and the corresponding triangular windowed SDFT based on two philosophies as defined in the previous section. The problem of odd bin evaluation in the SDFT spectrum is discussed, and the circular CORDIC is defined to utilise it further.

2.1 Sliding DFT

Consider a digital sequence $s(n)$ with $n \in [p-N+1, p]$ at pth time instant which is drawn in Fig. 1. The window slides over the samples of the signal. The N-point DFT of type-1 sliding window for kth bin is given by

$$D1_p(k) = \sum_{n=0}^{N-1} s(p-N+1+n)\mathrm{e}^{-j(2\pi kn/N)}. \tag{1}$$

At the next time instant $(p+1)$, the type-1 SDFT can be recursively expressed as

$$D1_{p+1}(k) = \left[D1_p(k) + s(p+1) - s(p-N+1)\right]\mathrm{e}^{\mathrm{j}(2\pi k/N)}, \tag{2}$$

and the type-1 SDFT expression in z-domain is [1]

$$H^k_{SDFT1}(z) = \frac{\mathrm{e}^{\mathrm{j}(2\pi k/N)}\left[1-z^{-N}\right]}{\left(1-\mathrm{e}^{\mathrm{j}(2\pi k/N)}z^{-1}\right)}. \tag{3}$$

Whereas, the N-point DFT of type-2 sliding window is

$$D2_p(k) = \sum_{n=0}^{N-1} s(p-n)\mathrm{e}^{-\mathrm{j}(2\pi kn/N)}. \tag{4}$$

The type-2 SDFT may be expressed as

$$D2_{p+1}(k) = D2_p(k)\mathrm{e}^{-\mathrm{j}(2\pi k/N)} + s(p+1) - s(p-N+1), \tag{5}$$

and the z-domain expression is given by [2]

$$H^k_{\mathrm{SDFT2}}(z) = \frac{\left[1-z^{-N}\right]}{\left(1-\mathrm{e}^{-\mathrm{j}(2\pi k/N)}z^{-1}\right)}. \tag{6}$$

2.2 Triangular windowed SDFT algorithm

The time-domain triangular window weights are given by [4]

$$w(n) = \begin{cases} \dfrac{n}{N/2}, & n \in \left[0, \dfrac{N}{2}\right] \\ \dfrac{N-n}{N/2}, & n \in \left[\dfrac{N}{2}+1, N-1\right] \end{cases}, \tag{7}$$

The triangular windowed DFT for type-1 sliding window of kth bin is

$$T1_p(k) = \sum_{n=0}^{N-1} s(p-N+1+n)w(n)\mathrm{e}^{-\mathrm{j}(2\pi kn/N)}, \tag{8}$$

whose expression in z-domain is given by

$$H^k_{\mathrm{TWSDFT1}}(z) = \frac{2}{N}\frac{\mathrm{e}^{\mathrm{j}(2\pi k/N)}\left[1-(-1)^k z^{-(N/2)}\right]^2}{\left(1-\mathrm{e}^{\mathrm{j}(2\pi k/N)}z^{-1}\right)^2}. \tag{9}$$

In a similar way, the triangular windowed DFT for type-2 sliding window is

$$T2_p(k) = \sum_{n=0}^{N-1} s(p-n)w(n)\mathrm{e}^{-\mathrm{j}(2\pi kn/N)}. \tag{10}$$

whose expression in z-domain is

$$H^k_{\mathrm{TWSDFT2}}(z) = \frac{2}{N}\frac{\mathrm{e}^{-\mathrm{j}(2\pi k/N)}z^{-1}\left[1-(-1)^k z^{-(N/2)}\right]^2}{\left(1-\mathrm{e}^{-\mathrm{j}(2\pi k/N)}z^{-1}\right)^2}, \tag{11}$$

We may note that these two types of windows in (9) and (11) provide the same magnitude with the different phase in the output. Following type-1 sliding window in (8), consider the desired spectrum $S_p(k)$ equal to $T1_p(k)$ and it can be expanded in the time domain as

$$S_p(k) = \mathrm{e}^{\mathrm{j}(2\pi k/N)}\left[2S_{p-1}(k) - \mathrm{e}^{\mathrm{j}(2\pi k/N)}S_{p-2}(k) + \frac{1}{N}r(p)\right], \tag{12}$$

where

$$r(p) = 2s(p) - 4(-1)^k s\left(p-\frac{N}{2}\right) + 2s(p-N). \tag{13}$$

Fig. 2*a* shows the block diagram of the type-1 triangular windowed SDFT as per (12) and (13), where (12) corresponds to the feedback structure (FBS-A) and (13) corresponds to the feedforward structure (FFS). Now, we may apply modulation property over the

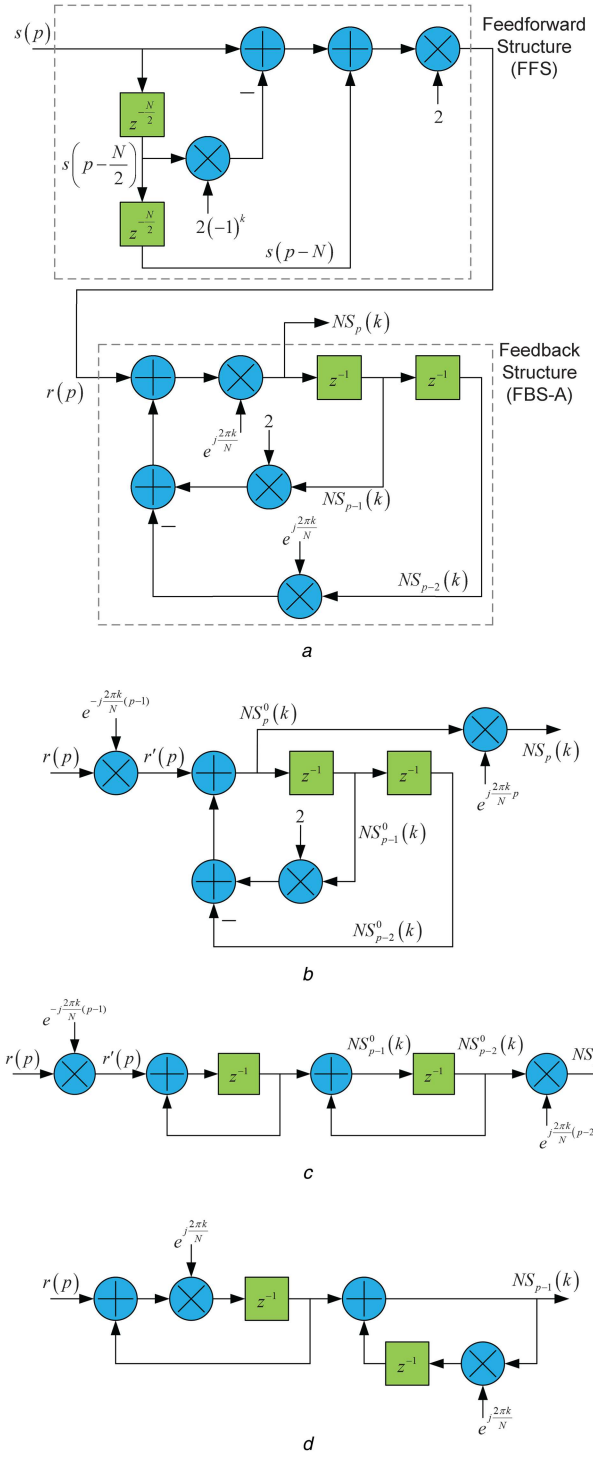

Fig. 2 *Type-1 triangular windowed SDFT design*
(a) Full block diagram of the design with feedback structure-A (FBS-A), ***(b)*** Feedback structure-B (FBS-B), ***(c)*** Feedback structure-C (FBS-C), ***(d)*** Feedback structure-D (FBS-D)

time-domain expression in (12), by assuming another variable, $S_p^0(k)$, such that

$$S_p(k) = e^{j(2\pi kp/N)} S_p^0(k), \tag{14}$$

By substituting $S_p(k)$ from (14) in (12), we have

$$NS_p^0(k) = 2NS_{p-1}^0(k) - NS_{p-2}^0(k) + r'(p). \tag{15}$$

where $r'(p) = e^{-j(2\pi k/N)(p-1)} r(p)$. Fig. 2*b* shows the corresponding feedback structure (FBS-B) for the expression in (15). Taking z-transform of (15), we have

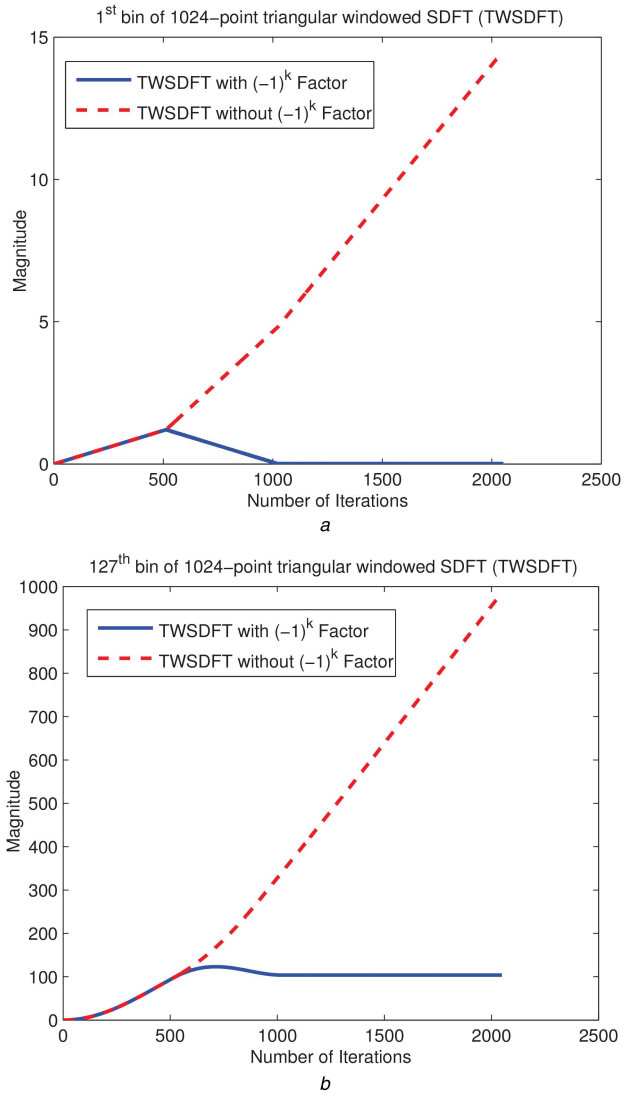

Fig. 3 *Evaluation of odd bins in the spectrum of 1024-point triangular windowed SDFT (assuming sinusoidal input is fixed at 128th bin)*
(a) Comparison of 1st bin in the spectrum, ***(b)*** Comparison of 127th bin in the spectrum

$$NS_k^0(z) = 2NS_k^0(z)z^{-1} - NS_k^0(z)z^{-2} + R'(z). \tag{16}$$

We can further rearrange (16) to get

$$\frac{NS_k^0(z)z^{-2}}{R'(z)} = \frac{z^{-2}}{\left(1 - z^{-1}\right)^2}. \tag{17}$$

The corresponding feedback structure (FBS-C) for the expression in (17) is shown in Fig. 2*c*. The output of FBS-C is $NS_{p-2}(k)$, which is just the time delayed output of $NS_p(k)$. We can also get another feedback structure for the triangular windowed SDFT by taking z-transform of (12)

$$NS_k(z) = 2e^{j(2\pi k/N)} NS_k(z)z^{-1} - e^{j(4\pi k/N)} NS_k(z)z^{-2} + e^{j(2\pi k/N)} R(z). \tag{18}$$

and rearranging (18), we get

$$\frac{NS_k(z)z^{-1}}{R(z)} = \frac{e^{j(2\pi k/N)} z^{-1}}{\left(1 - e^{j(2\pi k/N)} z^{-1}\right)^2}. \tag{19}$$

Fig. 2*d* shows the corresponding feedback structure (FBS-D) for the expression in (19). The output of this feedback structure is $NS_{p-1}(k)$, or the one clock cycle delayed $NS_p(k)$. All the four

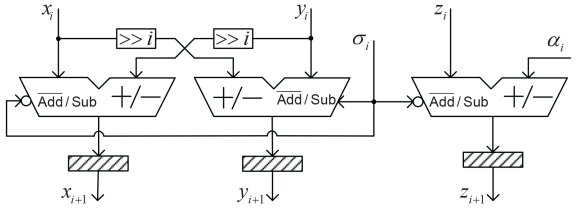

Fig. 4 *ith-stage of the pipelined circular CORDIC*

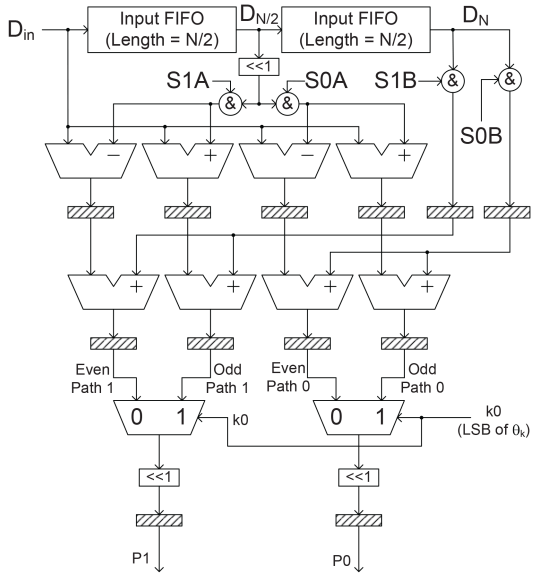

Fig. 5 *FFS of the proposed architecture*

feedback structures accumulate error as the iteration progresses. The second-order structures, FBS-A and FBS-B, are not stable due to high loop gain. Other two structures, FBS-C and FBS-D, have two loops in cascade and can be implemented in fixed-point arithmetic with refreshing mechanism. We have compared the triangular windowed SDFT performance using FBS-C and FBS-D in Section 5, and found that FBS-C does have less error accumulation. The FFS, which we have not shown in other three cases in Figs. 2*b*–*d*, is the same as has been shown in Fig. 2*a*.

2.3 Evaluation of odd bins in the spectrum of triangular windowed SDFT

As we have mentioned earlier, the triangular windowed SDFT cannot be directly obtained by cascading the two SDFT, and this error is due to not associating $(-1)^k$-factor in the exact transfer function provided in (9) and (11). In this section, we have compared the MATLAB models based on the exact transfer function and the transfer function without considering $(-1)^k$-factor. The exact transfer function of type-1 triangular windowed SDFT is provided in (9). The transform length (N) is kept 1024, and we have simulated the models for 2048 iterations. The applied sinusoidal input is fixed at 128th bin of the spectrum. The comparison is shown for the odd bins, which are noted for the 1st bin near to DC and 127th bin near to input signal frequency, is shown in Figs. 3*a* and *b*, respectively. The solid curve corresponds to the exact transfer function, which converges to a final value; whereas, the dotted curve corresponds to the transfer function without considering $(-1)^k$-factor, which is increasing as the iteration progresses and providing the inaccurate odd DFT bins.

2.4 Circular CORDIC algorithm

Before going into the details of the proposed architecture, we would like to give a brief introduction to circular CORDIC, which is being used in the design. Assume $[x_0, y_0]^T$ be the input vector to an n-stage pipelined circular CORDIC and is rotated with a target angle α. The output vector is given by

$$\begin{bmatrix} x_n \\ y_n \end{bmatrix} = K_n \begin{bmatrix} \cos\alpha & -\sin\alpha \\ \sin\alpha & \cos\alpha \end{bmatrix} \begin{bmatrix} x_0 \\ y_0 \end{bmatrix}. \tag{20}$$

where K_n is the scale factor equal to 1.6467602. To achieve this, we adopt a simple mechanism in which a single stage (as shown in Fig. 4) is defined as [22]

$$\begin{aligned} x_{i+1} &= x_i - \sigma_i 2^{-i} y_i, \\ y_{i+1} &= \sigma_i 2^{-i} x_i + y_i, \\ z_{i+1} &= z_i - \sigma_i \alpha_i. \end{aligned} \tag{21}$$

where the elementary angles $\alpha_i = \tan^{-1}(2^{-i})$, and the sign sequence σ_i equal to $\text{sign}(z_i)$ for rotational mode and $-\text{sign}(x_i y_i)$ for vectoring mode. In this way, the factors $\tan\alpha_i$ are reduced to only shift operations in digital hardware. The range of the initial angle of the rotational CORDIC is limited to $[-\pi/2, \pi/2]$. Therefore, to make further rotation outside this range, we usually pre-rotate the initial vector by π (simply by changing the sign of the x and y components), so that the remaining rotation angle belongs to the standard range [13].

In vectoring mode, we try to make y-component (y_n) reduced to zero so that the x-component (x_n) will provide magnitude as $(\text{sign}\{x_0\}K_n\sqrt{x_0^2 + y_0^2})$ and z-component (z_n) will provide the phase as $\tan^{-1}(y_0/x_0)$, if the initial angle (z_0) supplied to it is zero. A 2's complement stage is also required to get positive magnitude of the final output.

3 Hardware implementation

The FFS of the proposed architecture is depicted in Fig. 5. FFS block contains two first-in, first-out (FIFO) of length $N/2$ for the transform length N. Here, we have provided symbols 0 and 1 corresponding to two time-interleaved paths. The symbol '&' signifies the bitwise ANDing operation with the input. The architecture resets its values after $2N$ iterations, and both path-0 and path-1 provide the outputs in a time-interleaved fashion. After each refreshing, $D_{N/2}$ provides output earlier than D_N, and the functionality of the architecture remains intact. The corresponding control signals (*S*0*A*, *S*1*A*, *S*0*B*, and *S*1*B*) are generated for controlling $D_{N/2}$ and D_N. The remaining feedback structure (FBS) is based on FBS-C as shown in Fig. 2*c*. The full architecture is shown in Fig. 6*a* and its timing diagram is shown in Fig. 6*b*. The architecture requires two FFS blocks for real as well as imaginary input data. As shown in the timing diagram, the refreshing time for *S*0*A* and *S*1*A* is for $N/2$ sample periods only, whereas for *S*0*B* and *S*1*B*, the refreshing time is for N sample periods. An angle generator circuit is added to generate the angles θ_k corresponding to the desired M bins. The even or odd bin in the architecture is selected with $k0$, the LSB of the input rotation angle θ_k corresponding to kth bin. It is important since the even and odd bins may be evaluated within the same sample period.

The rotational CORDIC is subdivided into two parts, XY-pipe and Z-pipe to make the design area efficient [10]. In this way, a single Z-pipe is able to provide the inputs to other XY-pipes simultaneously. The length of the remaining FIFOs depends on the calculable number of bins (M) of the architecture. After the upper rotational CORDIC XY-pipe, FIFO-A and FIFO-B of length $(M - n)$ are added to retain the output of these CORDIC within a single sampling period. After FIFO-A and FIFO-B, the design has a feedback loop with a single adder with control signals *SF*0*A* and *SF*1*A*. Similarly, for the next loop, the control signals *SF*0*B* and *SF*1*B* are delayed version of *SF*0*A* and *SF*1*A*, respectively. We can note that within one sample period, intermediate calculations of M frequency bins are saved in the FIFOs of length M.

The design operates with two clocks, one is the sampling clock used for the input FIFOs, and the rest of the design utilises the internal clock. The internal clock frequency is M-times the sampling clock frequency, where M is the number of DFT bins which is required to be evaluated from the design. The control

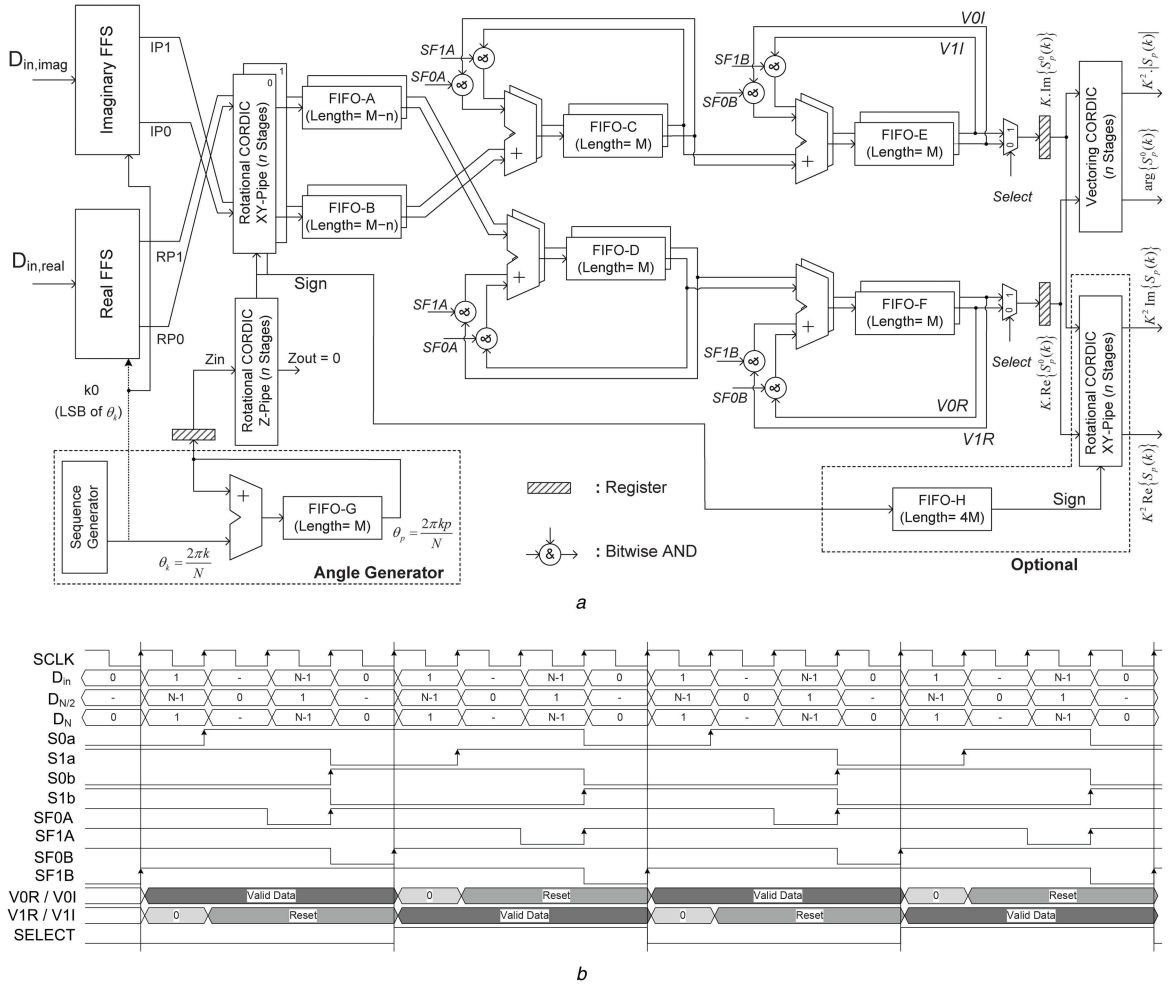

Fig. 6 *Proposed CORDIC-based triangular windowed SDFT design with refreshing mechanism*
(a) Proposed architecture, ***(b)*** Timing diagram

input *Select* is low or high for choosing the corresponding valid data at the output. The latency of the proposed architecture is five sampling clock cycles. *V0R*/*V1R* and *V0I*/*V1I* are the real and the imaginary outputs, respectively, before the output multiplexers. We have added a vectoring CORDIC to get the magnitude of the spectrum. An optional structure in the proposed architecture has also been added to get the real and imaginary output of the spectrum, if they are needed individually.

4 Worst-case truncation error for fixed-point arithmetic

In this section, we will evaluate the worst-case truncation error for the proposed architecture described in the last section. The truncation error corrupts the output of the design from the least significant bit (LSB). In the worst-case scenario, the *n*-stage pipelined architecture has $\lceil \log_2 n \rceil$ corrupted LSBs [22]. This also holds true for *n* iterations of a loop containing a single adder unit.

In the proposed architecture as depicted in Fig. 6*a*, an *n*-stage rotational CORDIC can accumulate maximum $E_1 = \lceil \log_2 n \rceil$ error bits. The recursive loop (which contains FIFO-A and FIFO-B) has additional $\lceil \log_2 m \rceil$ corrupted LSBs for *m* iterations. Hence, the total corrupted LSBs are $E_2 = (\lceil \log_2 m \rceil + E_1)$ up to the output of the first loop.

Now, another $\lceil \log_2 m \rceil$ LSBs will corrupt in the next recusive loop (which contains FIFO-C and FIFO-D) for *m* iterations. Therefore, at the output of this loop, we have $E_3 = (\lceil \log_2 m \rceil + E_2)$ corrupted LSBs. After this stage, we have *n*-stage CORDIC unit, which again will corrupt $\lceil \log_2 n \rceil$ in addition to E_3 corrupted LSBs. Thus, the truncation error of the proposed architecture (based on FBS-C) is $(\lceil \log_2 n \rceil + E_3)$, i.e. $(2\lceil \log_2 n \rceil + 2\lceil \log_2 m \rceil)$ bits. Similarly, for the design containing FBS-D structure, the truncation error is also equal to $(2\lceil \log_2 n \rceil + 2\lceil \log_2 m \rceil)$ bits.

The proposed architecture has 32 bit-width of the internal arithmetic (hence $n = 32$), and it works for $2N$ iterations before reset ($m = 2N$), where *N* is the transform length. Therefore, the maximum truncation error of the proposed architecture (in Fig. 6*a*) is $(2\lceil \log_2 n \rceil + 2\lceil \log_2 2N \rceil)$ bits.

5 Results and discussion

The proposed triangular windowed SDFT architecture is described in Verilog HDL, and the simulation results are obtained using ModelSim simulator. The bit-width of the internal arithmetic is 32 bits, in which 16 bits are assigned for the fractional part (*f*), 15 bits for the integer part, and 1 bit for sign. Another model is reproduced in MATLAB to verify the register transfer level simulation results. The input test signal to the model is a real-valued sampled sinusoidal, $s(p) = \text{floor}\left[2^f \cos(2\pi bp/N)\right]/2^f$, where floor($x$) is the largest integer smaller than or equal to x, and b is the signal bin [10]. We have compared the error accumulation within the bandwidth (from 0th bin to $(N/2-1)$th bin) of CORDIC-based architectures of triangular windowed SDFT using FBS-C and FBS-D in Figs. 7*a* and *b* for 1024- and 2048-point DFT, respectively. The proposed architecture is based on FBS-C, and it is having the minimum error with the additional refreshing mechanism. We have also simulated the CORDIC-based triangular windowed SDFT using second-order structures (FBS-A and FBS-B), and we found that these architectures are not stable and its error increases rapidly as the iteration count grows.

The Verilog code is synthesised using Xilinx ISE tool, and the FPGA Virtex-6 device is utilised. The device utilisation summary is shown in Table 1, and a comparison is made with the CORDIC-

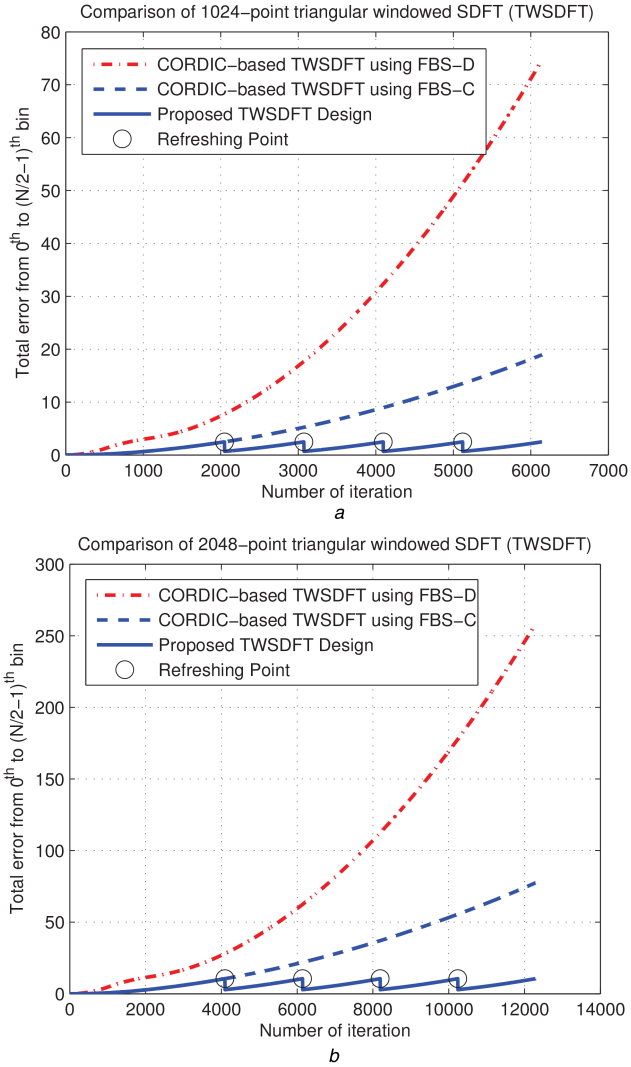

Fig. 7 *Comparison of total error for 32-bit CORDIC-based architectures (assuming fractional part of 16 bits)*
(a) 1024-point triangular windowed SDFT, ***(b)*** 2048-point triangular windowed SDFT

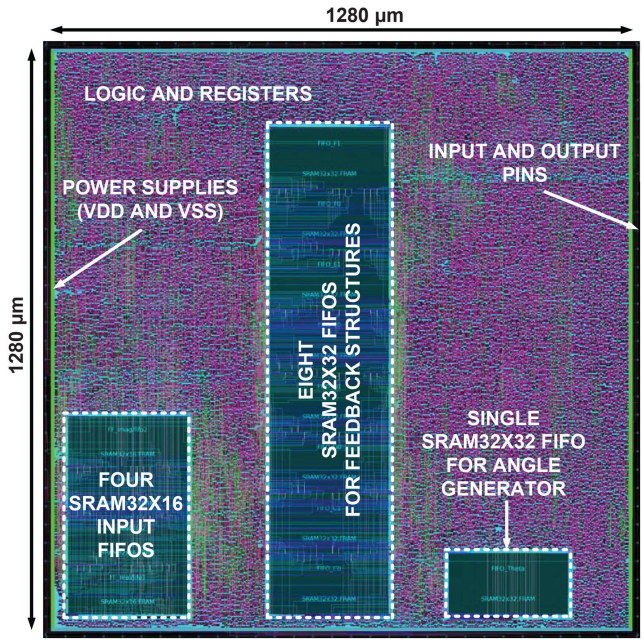

Fig. 8 *Chip layout of the proposed 32-point triangular windowed SDFT architecture with refreshing mechanism*

Table 1 Comparison of FPGA post-route result for 32-bit wordlength of internal arithmetic

Architecture[a]	Hann windowed SDFT with refreshing [10]	Proposed triangular windowed SDFT with refreshing (for $M = 1$)	(for $M = 32$)	(for $M = 64$)
DFT length (N)	64–2048	32–2048	32	64–2048
no. of bins (M)	64	1	32	64
word-length (n)	32 bits	32 bits	32 bits	32 bits
no. of slices (approx.)	11–11.2k (29%)	2.5–3.0k (7–8%)	2.5k (7%)	2.5–3.0k (7–8%)
no. of LUTs (approx.)	39–39.7k (26%)	8–10k (5–7%)	8k (5%)	8–10k (5–7%)
no. of DFF (approx.)	39–39.3k (13%)	8–10k (3%)	8k (3%)	8–10k (3%)
no. of block RAM [size]	2 [N × 32-bit]	4 [(N/2) × 32-bit]	4 [16 × 32-bit]	4 [(N/2) × 32-bit]
	4 [32 × 32-bit]		9 [32 × 32-bit]	4 [32 × 32-bit]
				9 [64 × 32-bit]
max. internal freq., f_{in}	239 MHz	239 MHz	239 MHz	239 MHz
max. sampling freq., f_s	3.73 MHz	239 MHz	7.46 MHz	3.73 MHz
highest side lobe level of DTFT[b]	–32 dB	–27 dB	–27 dB	–27 dB
side lobe fall off of DTFT[b]	–18 dB/ Octave	–12 dB/ Octave	–12 dB/ Octave	–12 dB/ Octave

[a]Virtex-6 FPGA device XC6VLX240T-FF1759.
[b]Corresponding to the respective discrete-time Fourier transform (DTFT) of the finite windowed data sequence.

Table 2 ASIC post-layout result of the proposed 32-bit triangular windowed SDFT architecture with refreshing mechanism

Parameters	Specification
technology library	SAED 90 nm standard cell
DFT length (N)	32
DFT bins (M)	32
bit-width	32 bits
leakage power	3.7981 mW
dynamic power[a]	49.2794 mW
logic area	1,196,961 µm^2
SRAM area	441,439 µm^2 (four SRAM32 × 16 and nine SRAM32 × 32)
total area	1,638,400 µm^2
chip area	1,782,225 µm^2
max. internal freq., f_{in}	200 MHz
max. sampling freq., f_s	6.25 MHz

[a]Power estimated at 1.2 V supply with 160 MHz clock rate.

based Hann windowed SDFT architecture proposed in [10]. The proposed architecture has the maximum internal frequency of 239 MHz, and it can deliver the output at the same rate for a single bin evaluation. Therefore, the proposed architecture is also able to provide high throughput for spectrum analysis.

All the architectures are made for 32-bit internal word length. Therefore, we have used 32-stage pipelined CORDIC inside these architectures. In the case of the proposed architecture, the scale factor compensation for CORDIC is not required. In the Hann windowed SDFT proposed in [10], the CORDIC is inside the loop; therefore, the scale factor compensation is needed. Also, the number of slices of the proposed architecture is less than the design

Table 3 Hardware comparison of *N*-point triangular windowed SDFT architectures for the internal wordlength of *n*-bits

Architecture	Window type	No. of DFT bins	Input type	No. of multipliers	No. of CORDIC	No. of adders	FIFO required (length)
[3]	type-2	1 bin	real	3 (complex)	0	4 (complex)	2 input FIFOs ($N/2$)
		M bins	real	3*M* (complex)	0	4*M* (complex)	2*M* input FIFOs ($N/2$)
[12]	type-1	1 bin	complex	2 (complex)	0	4 (complex)	4 FIFOs ($N/2R$)[a]
		M bins	complex	2*M* (complex)	0	4*M* (complex)	4*M* FIFOs ($N/2R$)[a]
[20]	type-1	1 bin	real	2 (complex)	0	4 (complex)	2 FIFOs ($N/2$)
		M bins	real	2*M* (complex)	0	4*M* (complex)	2 FIFOs ($N/2$)
[21]	type-1	1 bin	complex	5 (complex)	0	4 (complex)	4 input FIFO ($N/2$)
proposed design	type-1	1 bin	complex	0	2 rotational + 1 vectoring	25 (real)	4 input FIFOs ($N/2$)
		M bins	complex	0	2 rotational + 1 vectoring	25 (real)	4 input FIFOs ($N/2$) + 4 FIFOs ($M-n$) + 9 FIFOs (*M*)

[a]R is the decimation factor of corresponding CIC filter.

Table 4 Accuracy comparison with the existing triangular windowed SDFT architectures

Architecture	Feedback structure	Error limiting feature	Maximum possible truncation error at *m*th iteration[a]	Observations
[3]	FBS-D (type-2)	no	$(2\log_2 l + 2\log_2 m)$ bits	unbounded error accumulation and accurate transfer function
[12]	FBS-C (type-1)	no	$(2\log_2 l + 2\log_2 m)$ bits	unbounded error accumulation and problem of odd bins evaluation
[20]	FBS-C (type-1)	no	$(2\log_2 l + 2\log_2 m)$ bits	unbounded error accumulation and problem of odd bins evaluation
[21]	FBS-A (type-1)	no	unstable	unstable design based on FBS-A and accurate transfer function
proposed design	FBS-C (type-1)	yes	$(2\log_2 n + 2\log_2 2N)$ bits	CORDIC-based design with accurate transfer function and bounded error accumulation with refreshing

[a]Assuming each multiplier in the existing architecture contains *l*-stages.

proposed in [10]. We have used the dual-port RAM to implement the FIFOs.

The proposed architecture has been synthesised using the design compiler with SAED 90 nm standard cell library. The netlist generated from the design compiler is processed in IC compiler for placement and routing. The layout of the proposed 32-point triangular windowed SDFT architecture is shown in Fig. 8. The FIFOs of the architecture are synthesised using SRAM32 × 16 and SRAM32 × 32 provided in the SAED 90 nm library. Table 2 shows the ASIC post-layout results of the proposed architecture. It consumes 53 mW of power at 1.2 V supply with 160 MHz clock rate.

The hardware comparison is shown in Table 3 with the existing architectures. The transform length of all the designs is *N*, and we have compared these architectures for evaluation of a single bin and in general, *M* bins out of overall *N* frequency bins. We find that the use of CORDIC inside the proposed architecture reduces the hardware requirement with increasing *M*. The total number of arithmetic blocks is fixed in the proposed design. In Table 4, we have presented the accuracy comparison of the proposed architecture with the existing designs. We have assumed that all the multipliers used in the existing designs contain *l*-stages, which can accumulate the truncation error of $\log_2 l$ bits. It is evident that the maximum error in the proposed architecture does not depend on the iteration count (m), whereas the truncation error of the existing designs depends on m. The proposed design is based on the feedback structure FBS-C with the refreshing mechanism, which gives a stable performance as shown in Fig. 7.

6 Conclusion

We have proposed a very-large-scale integration (VLSI) architecture for a triangular windowed SDFT based on CORDIC. The problem of calculating the odd bins in the DFT spectrum can be solved by accurately determining the transfer function for the triangular windowed SDFT. Again, we have shown the two possibilities for selecting the data window. We have selected the sliding window with increasing time indices since the majority of works are based on the same. The error accumulation in the second-order feedback structures grows exponentially; thus we have selected the feedback structures with the single order in cascade. The architecture has the time-interleaved refreshing mechanism, and therefore it can further limit the error accumulation which is the main bottleneck of the SDFT designs. The proposed architecture is scalable with the calculable number of bins. We have also presented the possible worst-case truncation error of the architecture. The proposed architecture utilises the re-timing scheme and has a high throughput rate of 239 MHz on Xilinx Virtex-6 platform for calculating a single bin.

7 References

[1] Jacobsen, E., Lyons, R.: 'Sliding spectrum analysis', in Lyons, R.G. (Ed.): '*Streamlining digital signal processing: A tricks of the trade guidebook*' (Wiley-IEEE Press, New Jersey, USA, 2012, 2nd edn.), pp. 175–188

[2] Farhang-Boroujeny, B.: '*Adaptive filters: theory and applications*' (John Wiley & Sons, West Sussex, UK, 2013, 2nd edn.)

[3] Gronczynski, J.: 'Recursive Fourier transform algorithms with integrated windowing', *Signal Process.*, 2007, **87**, (5), pp. 1003–1013

[4] Lyons, R.G.: '*Understanding digital signal processing*' (Prentice Hall, New Jersey, USA, 2012, 3rd edn.)

[5] Rapuano, S., Harris, F.J.: 'An introduction to FFT and time domain windows', *IEEE Instrum. Meas. Mag.*, 2007, **10**, (6), pp. 32–44

[6] Ray, K.C., Dhar, A.S.: 'CORDIC-based unified VLSI architecture for implementing window functions for real-time spectral analysis', *IEE Proc. Circuits Devices Syst.*, 2006, **153**, (6), pp. 539–544

[7] Aggarwal, S., Khare, K.: 'CORDIC-based window implementation to minimise area and pipeline depth', *IET Signal Process.*, 2013, **7**, (5), pp. 427–435

[8] Kumar, V., Ray, K.C., Kumar, P.: 'CORDIC-based VLSI architecture for real-time implementation of flat top window', *Microprocess. Microsyst.*, 2014, **38**, (8), pp. 1063–1071

[9] Tan, J., Wen, B., Tian, Y., *et al.*: 'Frequency convolution for implementing window functions in spectral analysis', *Circuits Syst. Signal Process.*, 2017, **36**, (5), pp. 2198–2208

[10] Kulshreshtha, T., Dhar, A.S.: 'CORDIC-based Hann windowed sliding DFT architecture for real-time spectrum analysis with bounded error accumulation', *IET Circuits Devices Syst.*, 2017, **11**, (5), pp. 487–495
[11] Duda, K.: 'Accurate, guaranteed-stable, sliding DFT', in Lyons, R.G. (Ed.): '*Streamlining digital signal processing: A tricks of the trade guidebook*' (Wiley-IEEE Press, New Jersey, USA, 2012, 2nd edn.), pp. 207–214
[12] Gudovskiy, D.A., Chu, L.: 'An accurate and stable sliding DFT computed by a modified CIC filter', *IEEE Signal Process. Mag.*, 2017, **34**, (1), pp. 89–93
[13] Kulshreshtha, T., Dhar, A.S.: 'CORDIC-based high throughput sliding DFT architecture with reduced error-accumulation', *Circuits Syst. Signal Process.*, 2018, **37**, (11), pp. 5101–5126
[14] Park, C.S.: 'The hopping discrete Fourier transform', *IEEE Signal Process. Mag.*, 2014, **31**, (2), pp. 135–139
[15] Wang, Q., Yan, X., Qin, K.: 'High-precision, permanently stable, modulated hopping discrete Fourier transform', *IEEE Signal Process. Lett.*, 2015, **22**, (6), pp. 748–751
[16] Juang, W.H., Lai, S.C., Chen, K.H.*, et al.*: 'Low-complexity hopping DFT design based on a compact recursive structure', *Electron. Lett.*, 2017, **53**, (1), pp. 25–27
[17] Park, C.S.: 'Fast, accurate, and guaranteed stable sliding discrete Fourier transform', *IEEE Signal Process. Mag.*, 2015, **32**, (4), pp. 145–156
[18] Park, C.S.: 'Guaranteed-stable sliding DFT algorithm with minimal computational requirements', *IEEE Trans. Signal Process.*, 2017, **65**, (20), pp. 5281–5288
[19] Ray, K.C., Dhar, A.S.: 'CORDIC-based VLSI architectures of running DFT with refreshing mechanism', *J. Signal Process. Syst.*, 2018, pp. 1–12, doi: 10.1007/s11265-018-1362-y
[20] Arnesen, D.M.: 'Sliding-window transform with integrated windowing'. U.S. Patent No. 7,020,218 B2, March 2006
[21] Wang, P.H.: 'Sliding Fourier transform with generalized triangular windows'. IEEE Int. Conf. Consumer Electron., Taiwan, Taipei, 2015, pp. 250–251
[22] Hu, Y.H.: 'The quantization effects of the CORDIC algorithm', *IEEE Trans. Signal Process.*, 1992, **40**, (4), pp. 834–844