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Microprocessor-Based Design
Due: 1/19/16

# Pre-Lab 1

## Number Systems

Pre 1.1) What is the binary, hex equivalent of the following decimal numbers:
a. $327_{10}$ = 0x147 = 0b101000111
b. $10_{10}$ = 0x0A = 0b1010
c. $100_{10}$ = 0x64 = 0b1100100

Pre 1.2) What is the decimal equivalent of the following hexadecimal numbers:
a. 0xA5 = $165_{10}$
b. 0x10 = $16_{10}$

Pre 1.3) What is the decimal and hex equivalent of the following binary numbers:
a. 0b00000010 = $2_{10}$ = 0x02
b. 0b00000100 = $4_{10}$ = 0x04
c. 0b01011111 = $95_{10}$ = 0x5F

Pre 1.4) Using bit operators in C only, how do you clear the 3rd bit without affecting other bits?

```
unsigned char bitClear3(unsigned char c)
{
    /* Bitwise AND with all ones except zero in 3rd position */
    c &= ~(1<<3);
    return c;
}
```

Pre 1.5) Using bit operators in C only, how do you set the 7th bit without affecting other bits?

```
unsigned char bitSet7(unsigned char c)
{
    /* Bitwise OR with all zeros except one in 7th position */
    c |= (1<<7);
    return c;
}
```

## Zynq-7000 Architecture and General Purpose I/Os

Pre 1.6) How many processor cores does the Zynq have in the PS side?
Answer: 2

Pre 1.7) What is the Instruction Set Architecture (ISA) of the processor cores in the Zynq's PS side?
Answer: ARM

Pre 1.8) How many GPIO signals does the PS have and how are they configured?

Answer: The PS has up to 54 GPIO signals for device pins routed through the MIO, and 192 GPIO signals between the PS and PL via the EMIO.

Pre 1.9) How do the “Direction Mode” register, and the “Output Enable” register have to be configured to configure one pin (assume the one associated with the LSB) as an output?
Answer: The “Direction Mode” register should be set to 1 at bit 0, and the “Output Enable” register should be set to 1 at bit 0.

Pre 1.10) By default are the pins associated with the GPIO bank 0 configured as output or as input? What is the reason for choosing this as the default?
Answer: By default, the pins associated with GPIO bank 0 are configured as input. This is the default because generating an output waveform requires software to repeatedly write to the target GPIOs. This is a more costly procedure, making input the natural default state.

Pre 1.11) Which register has to be read to see the input value of GPIO bank 2?
Answer: The inputs can be read from the DATA_RO register when the DIRM register is set to 0.

Pre 1.12) Which register has to be written to modify the output value of GPIO bank 2?
Answer: The output value is programmed using the DATA, MASK_DATA_LSW, and MASK_DATA_MSW registers. The DIRM register must be set to 1 to modify the output value.

Pre 1.13) Assume a device uses BANK2 to interface with LEDs and the complete port is already configured as an output. Please write C-code that sets the second output bit to high.
Answer:

```
/* Setup code, main function, etc. not included */
#ifndef DATA_2
#define DATA_2   (0x00000048)
#endif

/* Where bit position 1 is the LSB */
#define BIT_POSITION_2 (1<<1)

volatile unsigned int *data_reg = (unsigned int*) DATA_2;
*data_reg |= BIT_POSITION_2;
```

**Zynq-7000 Programmable Logic**

Pre 1.14)
a. The left most LED is mapped to pin 0 of bank 2(assuming left most LED is LD0).
b. The up button is mapped to pin 20 of bank 2.
c. Switch 2 is mapped to pin 10 of bank 2.

**Application Questions**

Pre 1.15) What is the formula to convert a temperature in degrees Fahrenheit to degrees Celsius?
Answer: °C = (°F – 32) * (5 / 9)