DHTM: Durable Hardware Transactional Memory

Arpit Joshi, *Vijay Nagarajan, Marcelo Cintra, Stratis Viglas*

ISCA 2018

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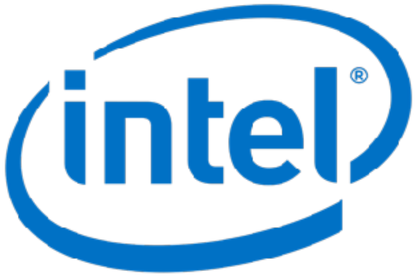

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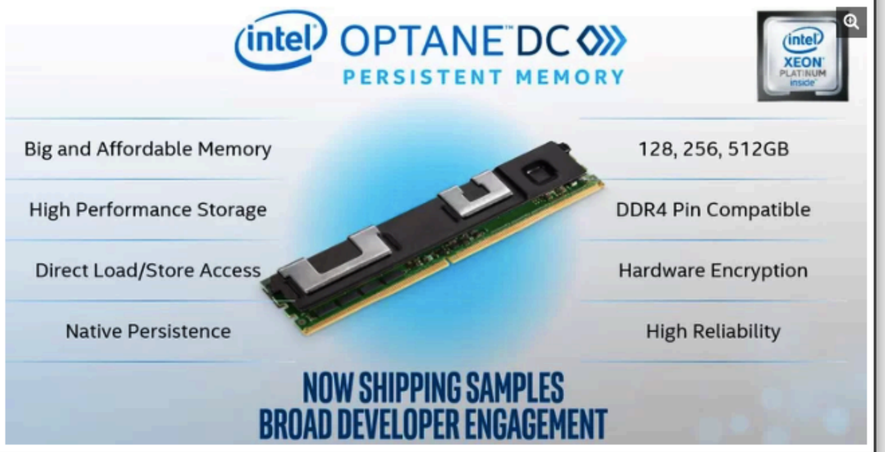
Persistent Memory is here…

Persistent Memory is here…

Intel Displays 512GB Optane DC Persistent Memory DIMMs

by Paul Alcorn May 31, 2018 at 2:02 AM

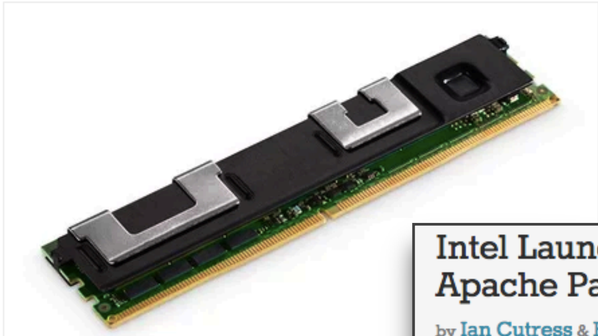
Intel held its Memory and Storage day today at its Santa Clara headquarters to announce its Optane DC Persistent Memory DIMMs. The new DIMMs slot into the DRAM interface, just like a normal stick of RAM, but come in three capacities of 128, 256, and 512GB. That's a massive capacity increase compared to the industry-leading 128GB DDR4 memory sticks. Intel designed the DIMMs to bridge both the performance and pricing gap between storage and memory, so the new DIMMs should land at much lower price points than typical DRAM.



Intel teases Optane DIMMS, but you may need a new Xeon first

128GB, 256GB and 512GB modules offered as new storage tier below RAM, above SSD

By Simon Sharwood, APAC Editor 31 May 2018 at 03:50 5 SHARE ▼



Intel's new Optane DC persistent memory DIMM. (C

Intel Launches Optane DIMMs Up To 512GB: Apache Pass Is Here!

60 Comments

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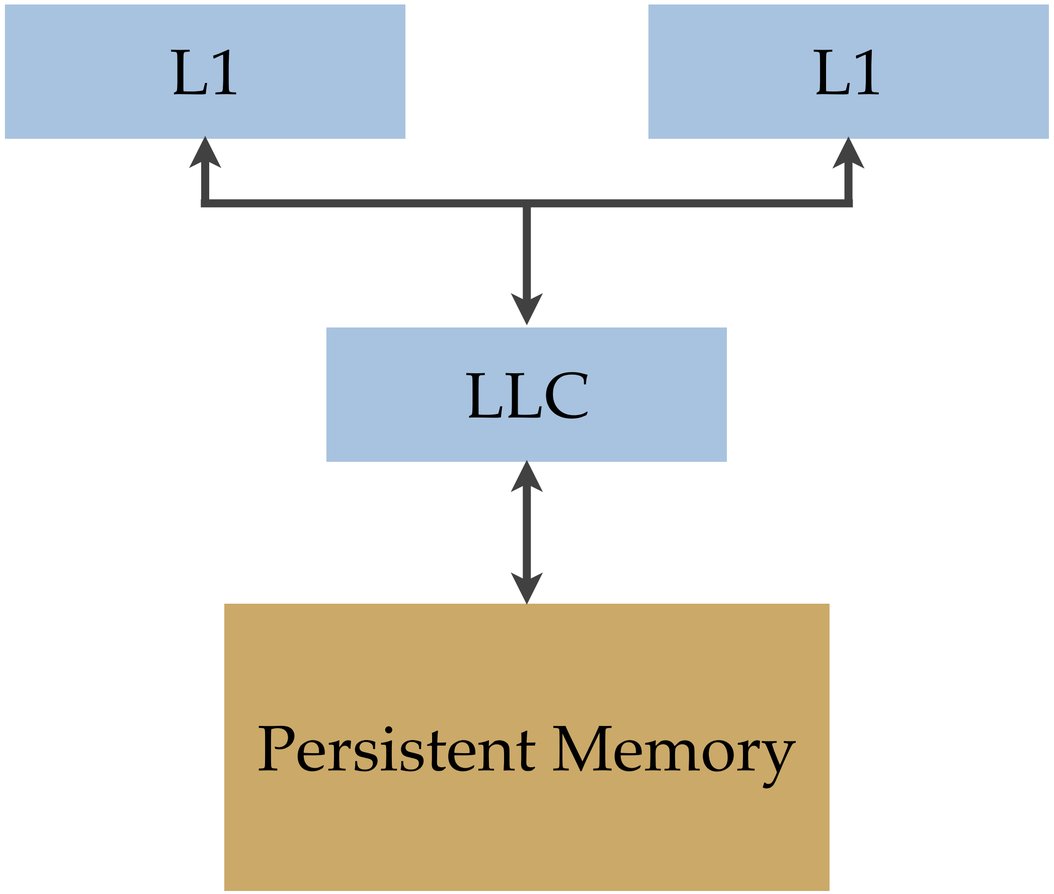
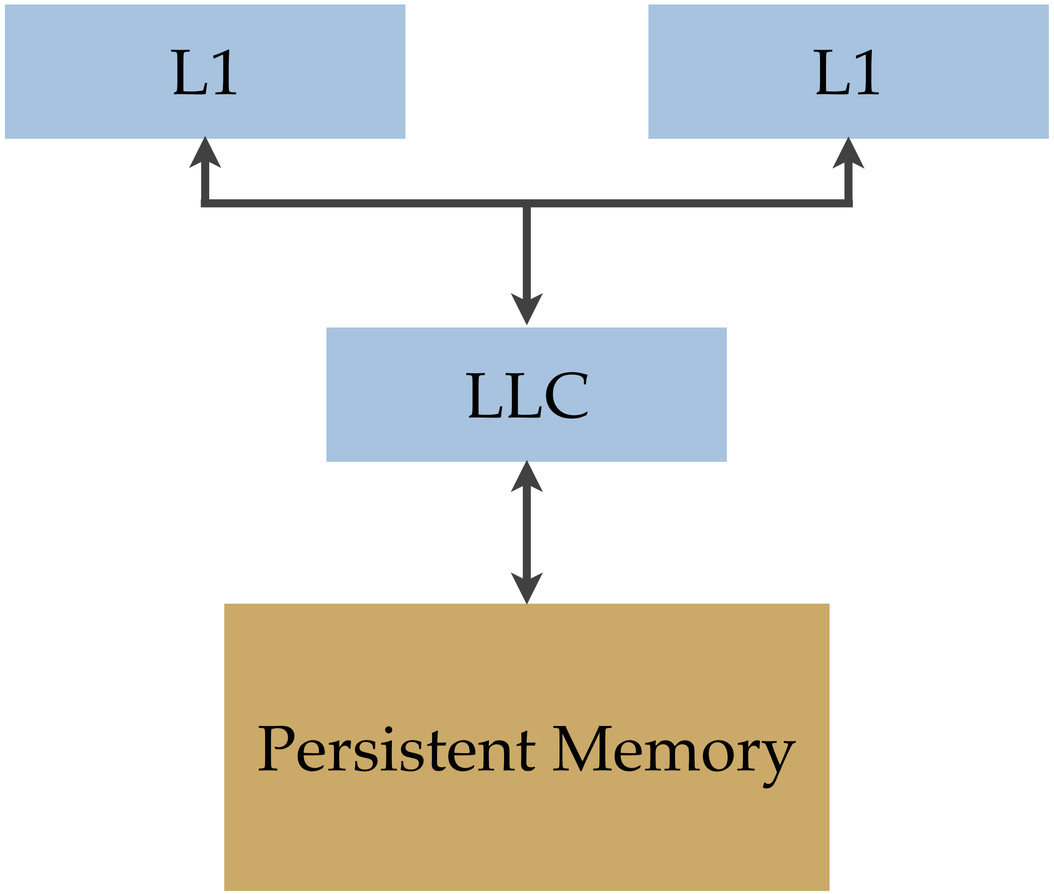
by Ian Cutress & Billy Tallis on May 30, 2018 2:15 PM EST

Posted in Intel DDR4 3D XPoint Optane NVDIMM Persistent Memory

Persistent Memory Systems



Persistent Memory Systems



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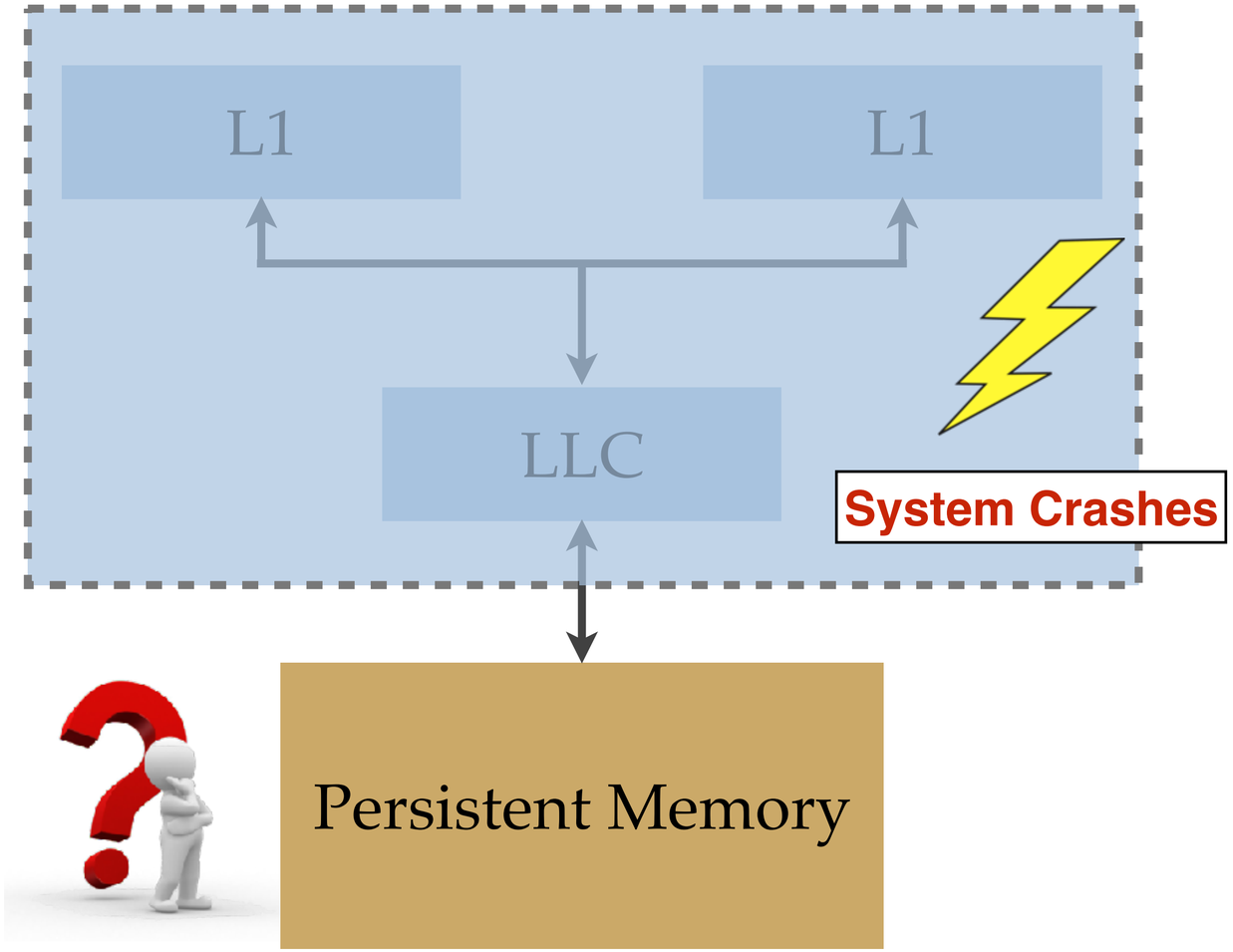
  - Non-volatility over the memory bus
  - Load/Store interface to persistent data

Persistent Memory Systems



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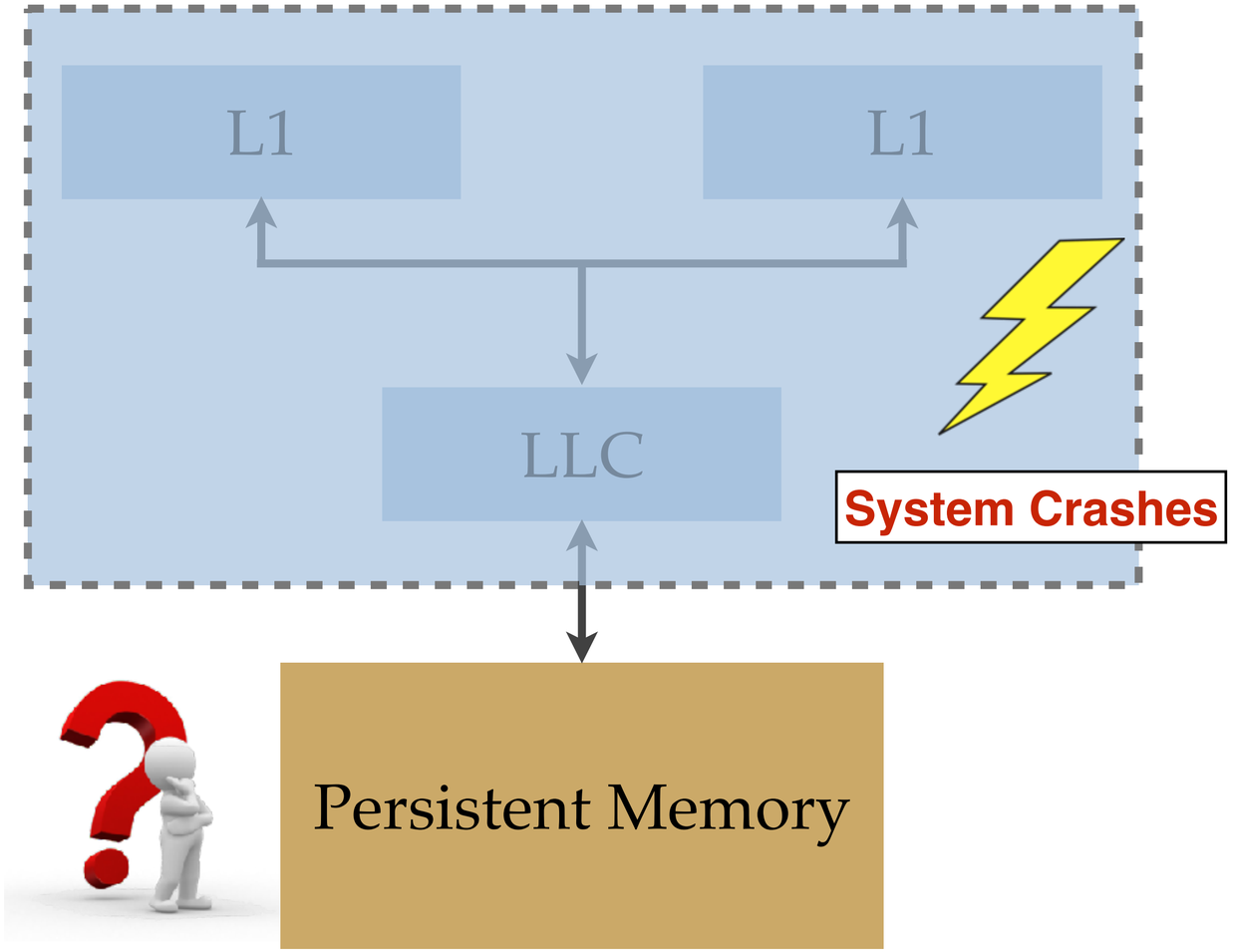

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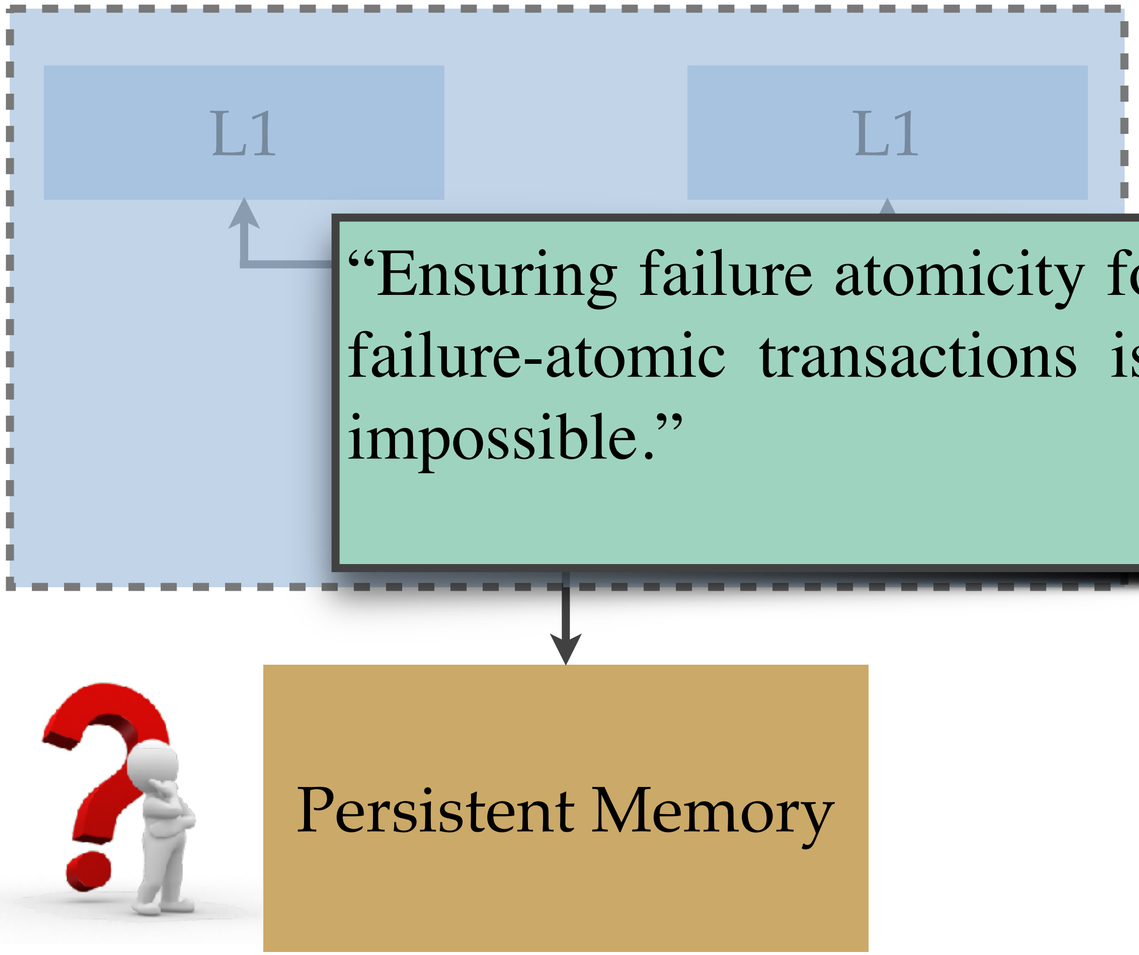
- **Crash Consistency**
  - Is the persistent state consistent?
  - Programming Model: ACID Transactions

Persistent Memory Systems



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Marathe et al. [HotStorage'17]

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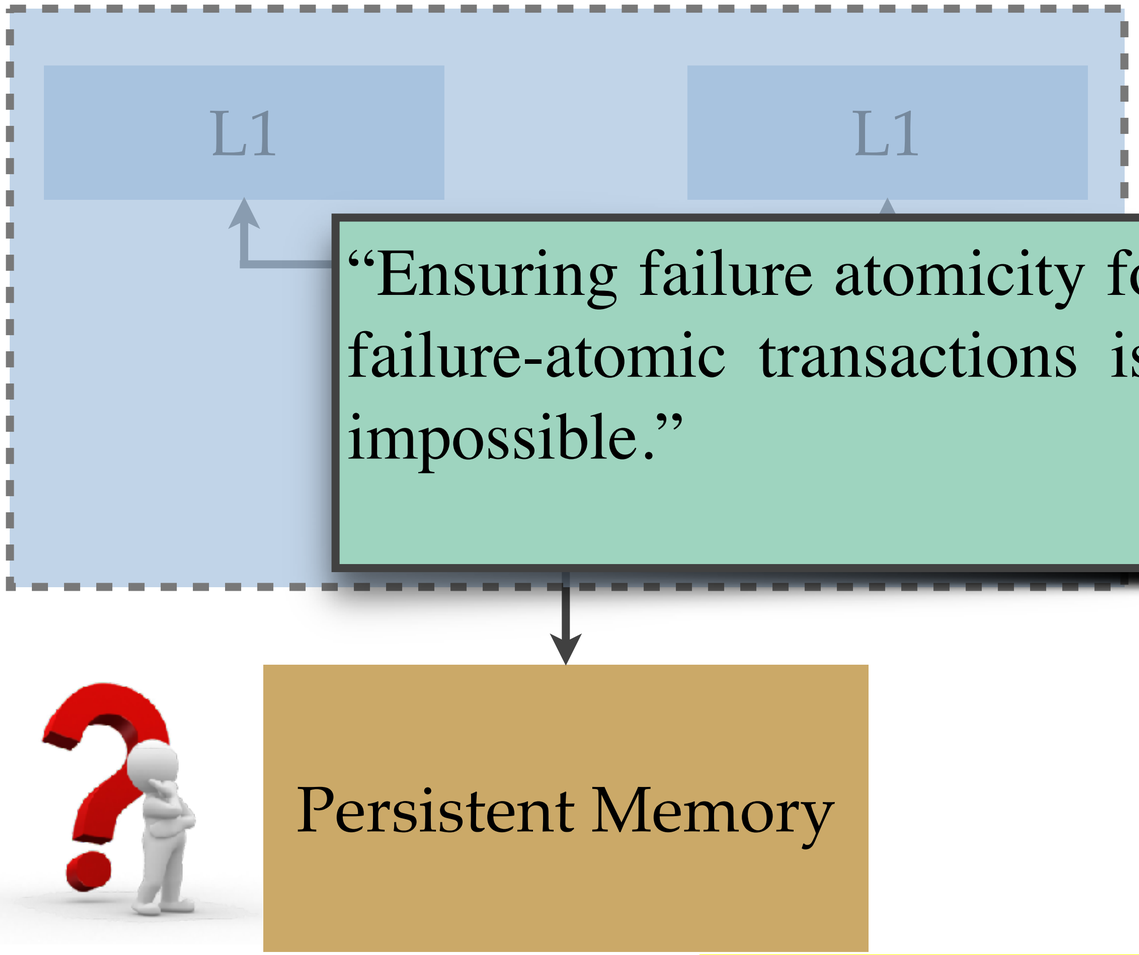

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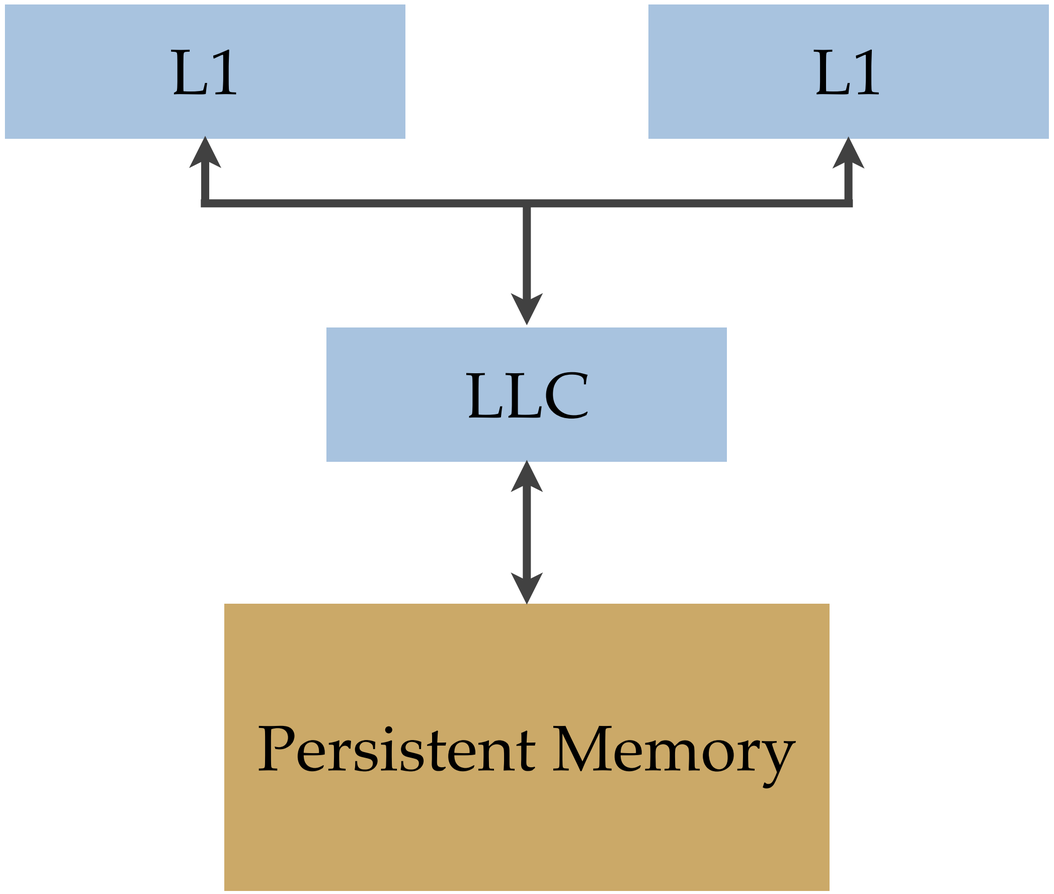
How fast can we support ACID?

ACID Transactions



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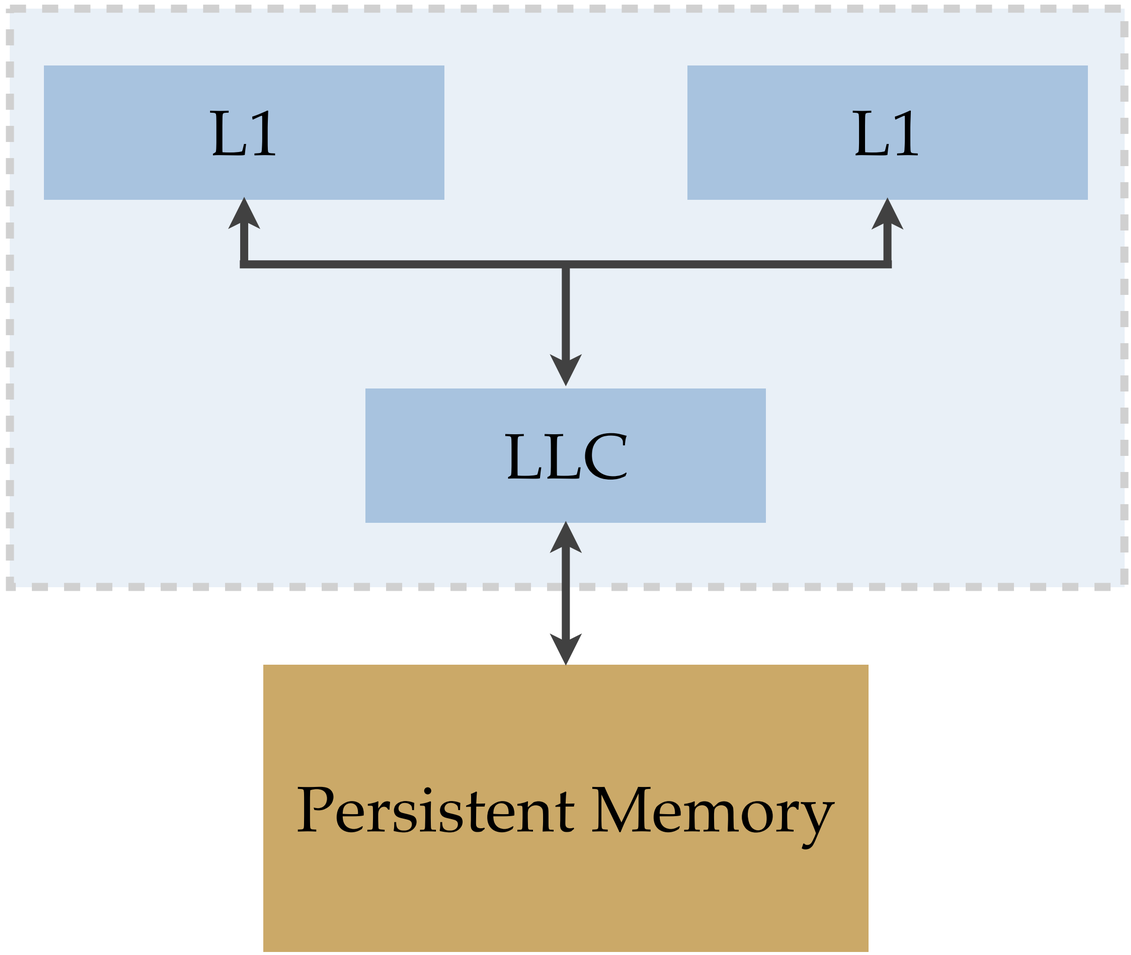
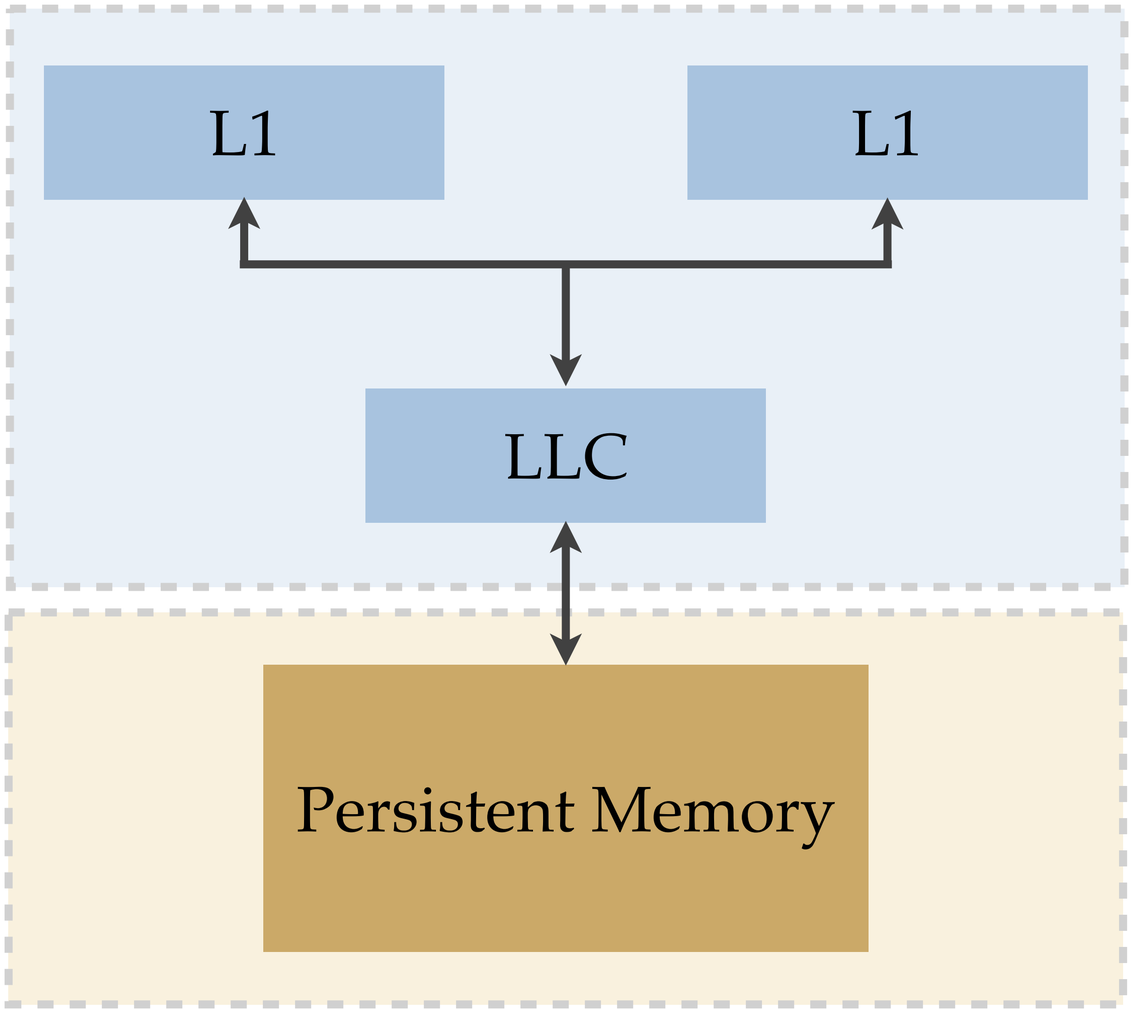


Atomic Visibility

ACID Transactions



Atomic Visibility

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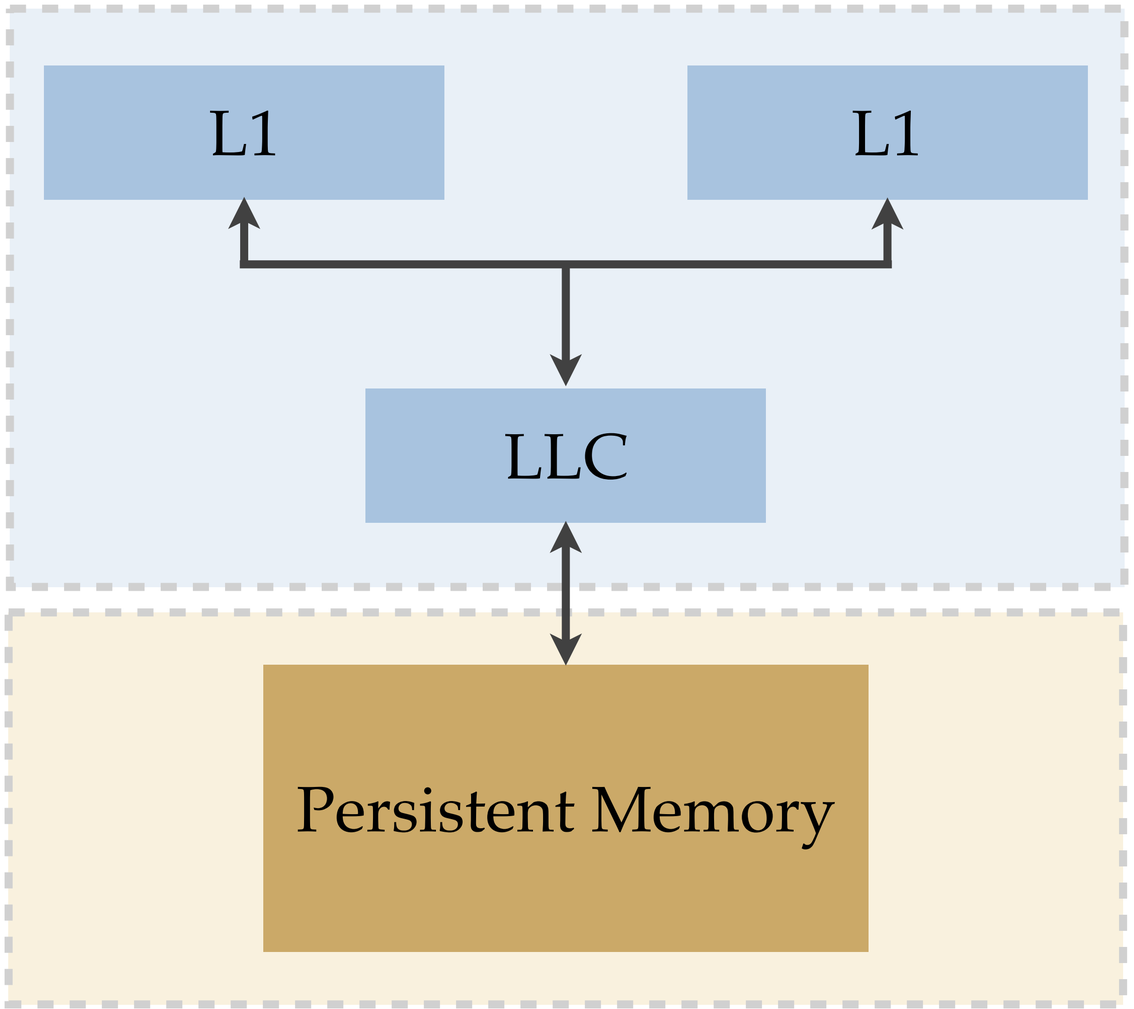

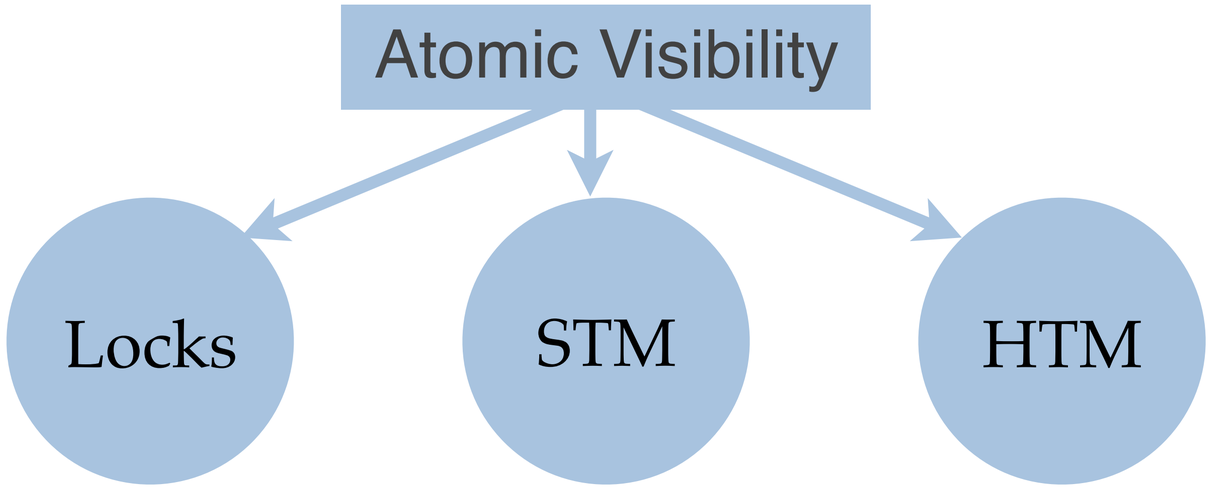

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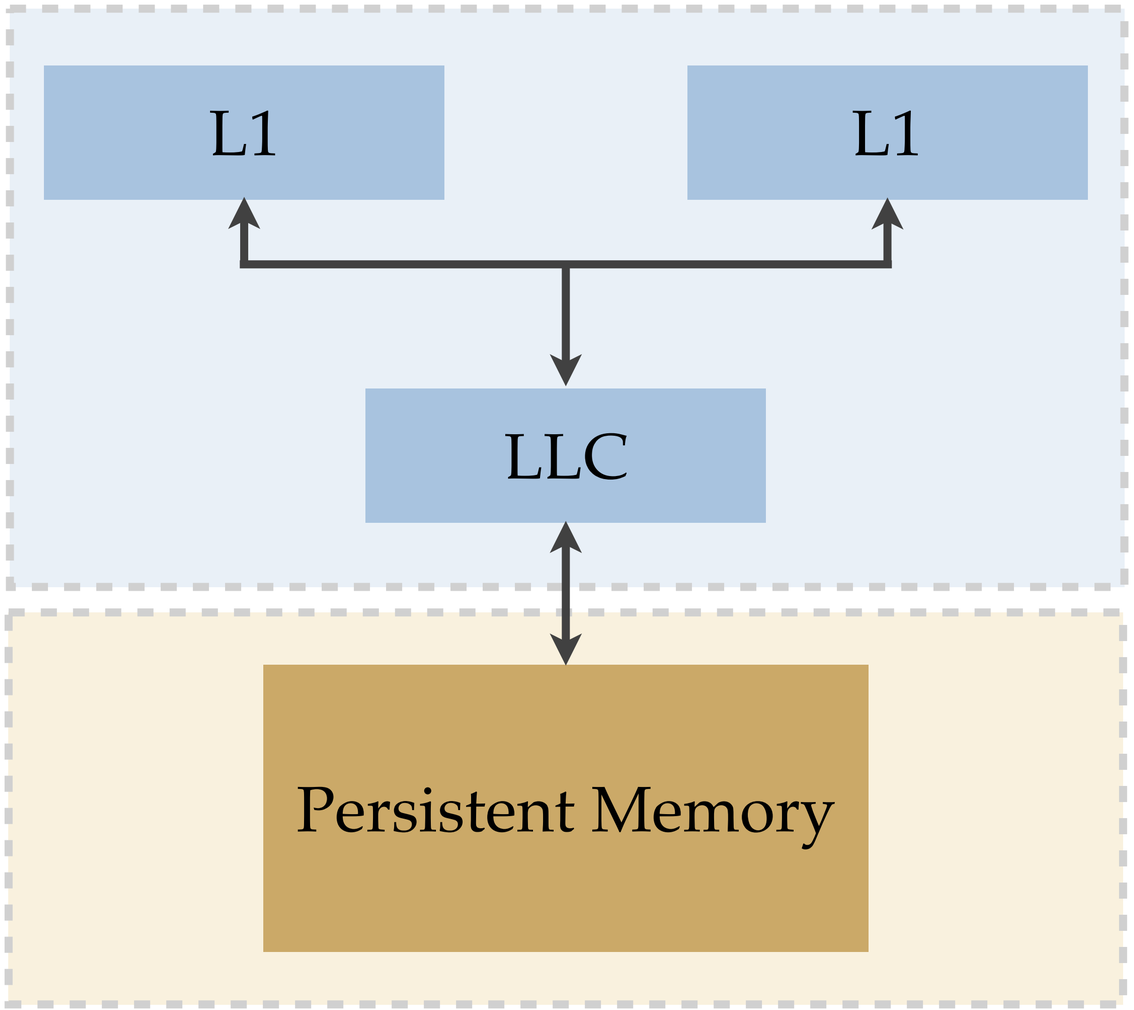

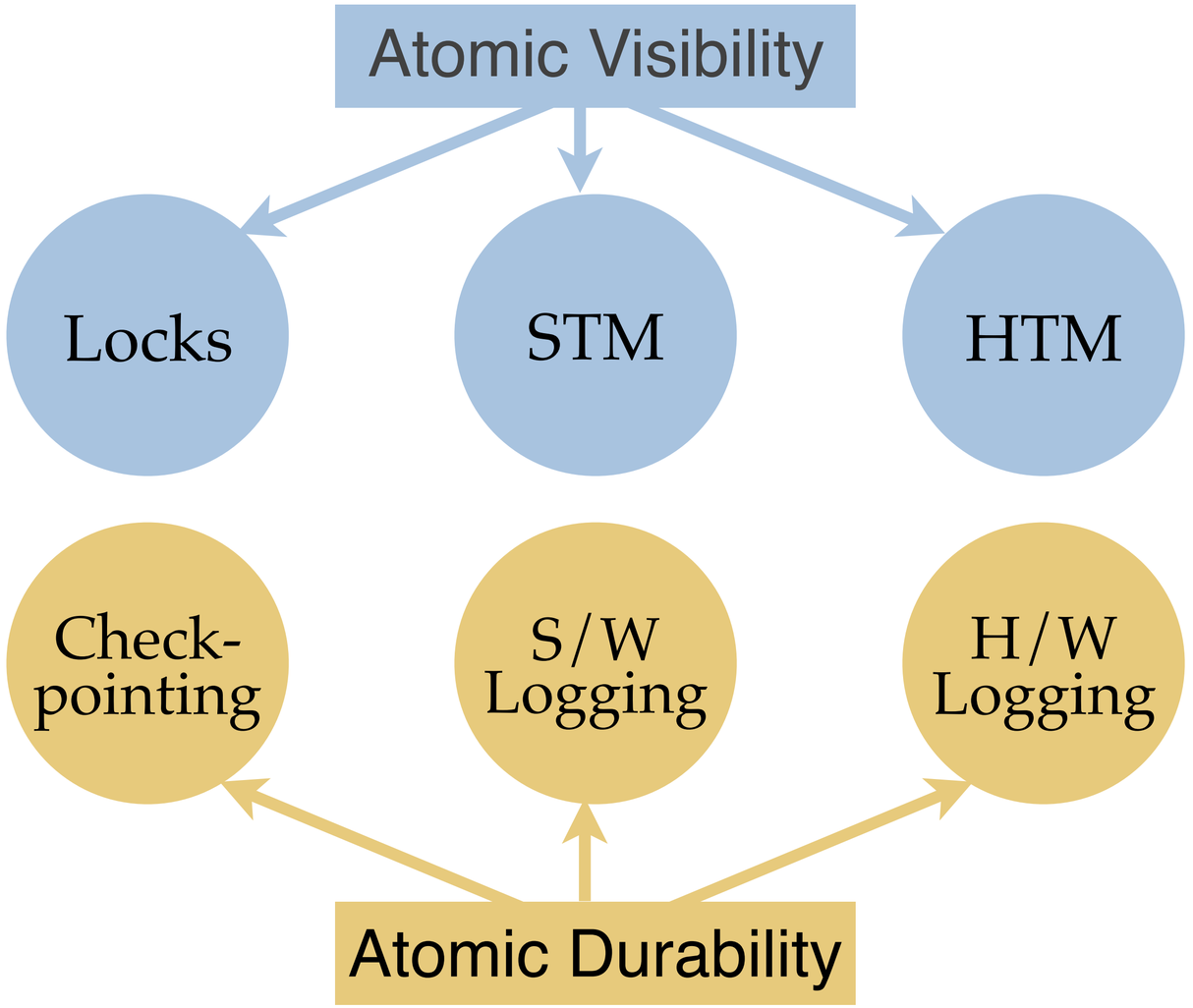

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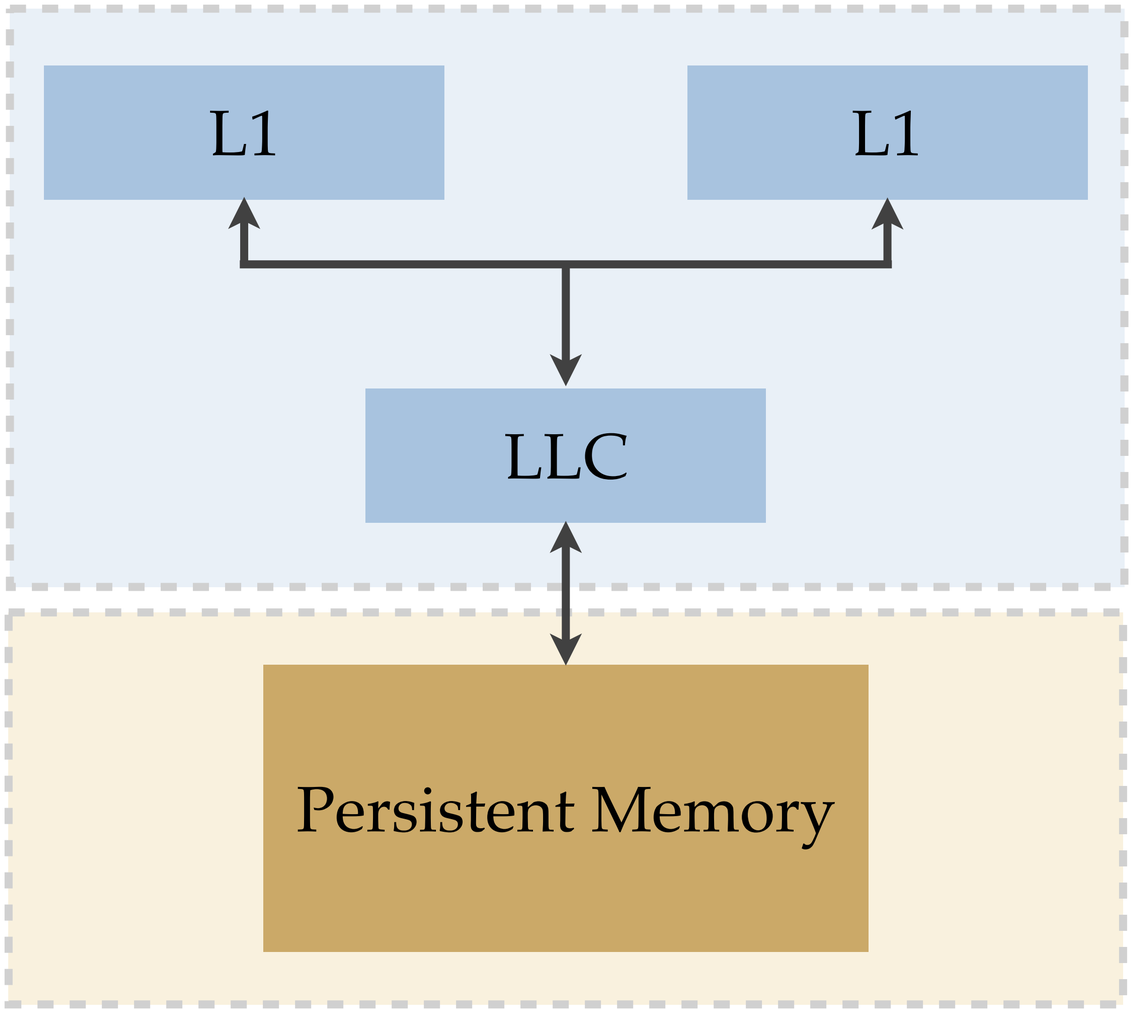

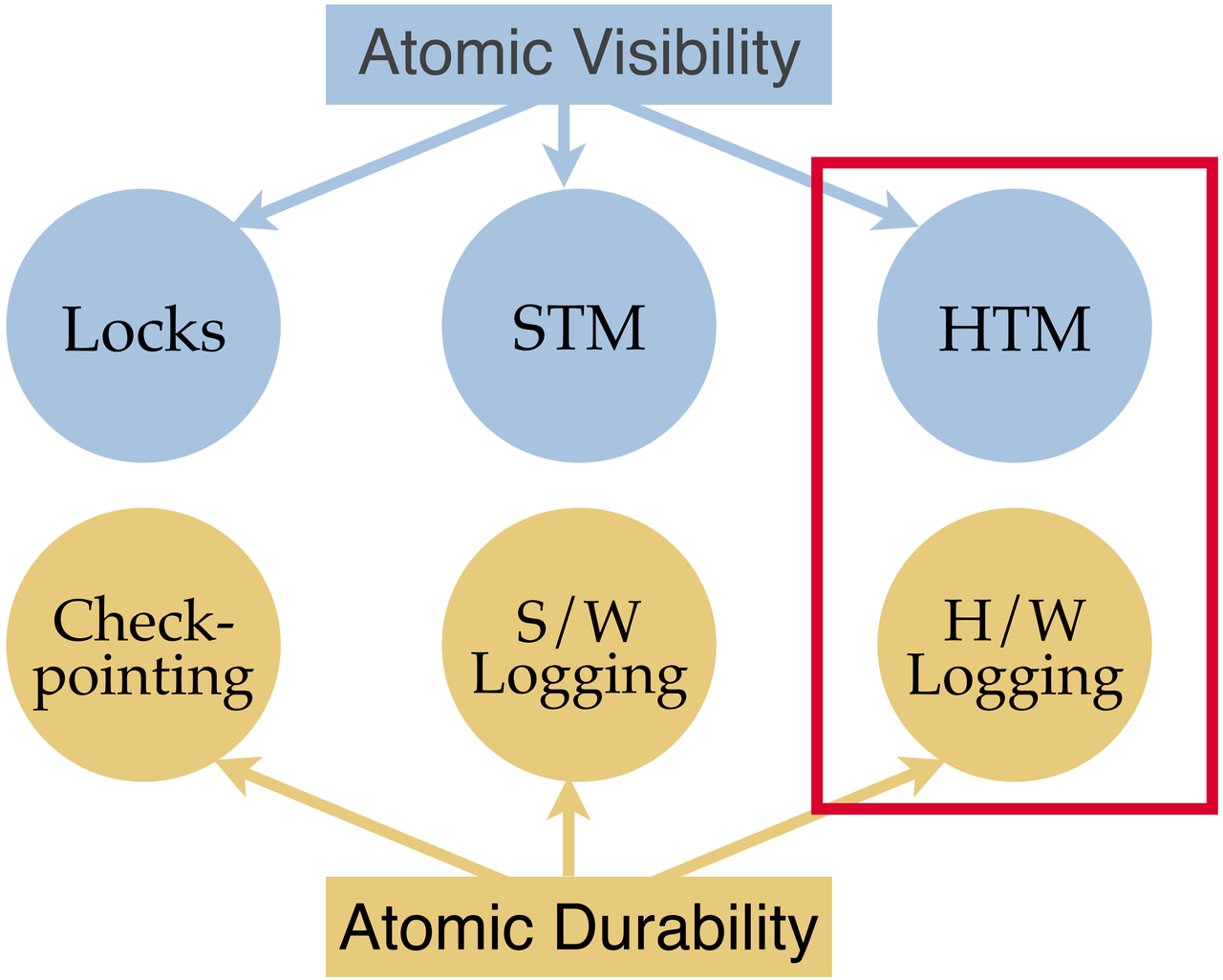

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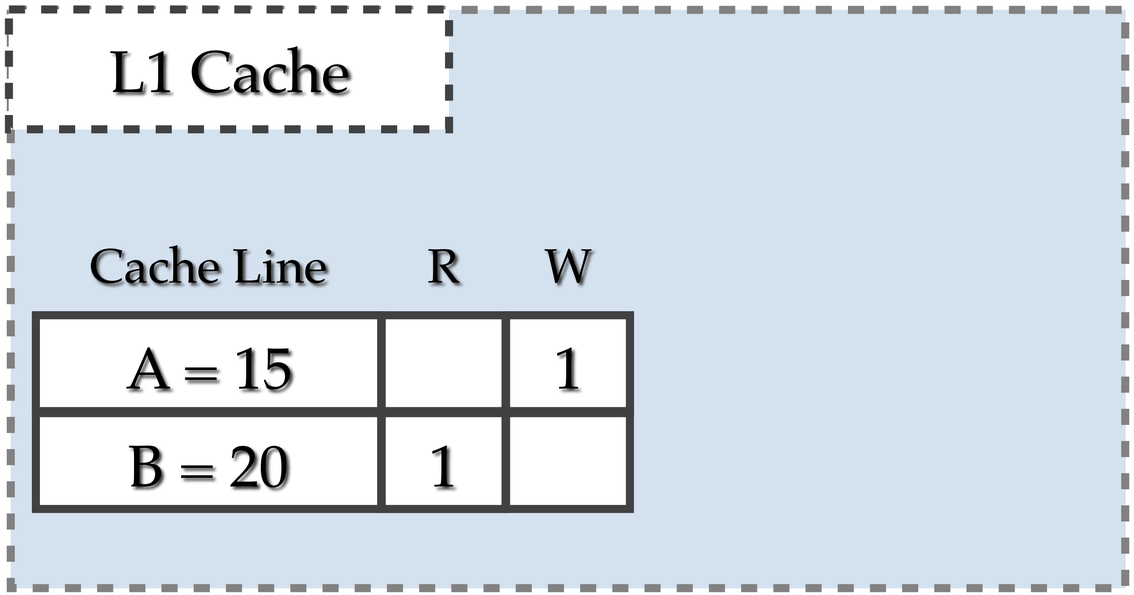

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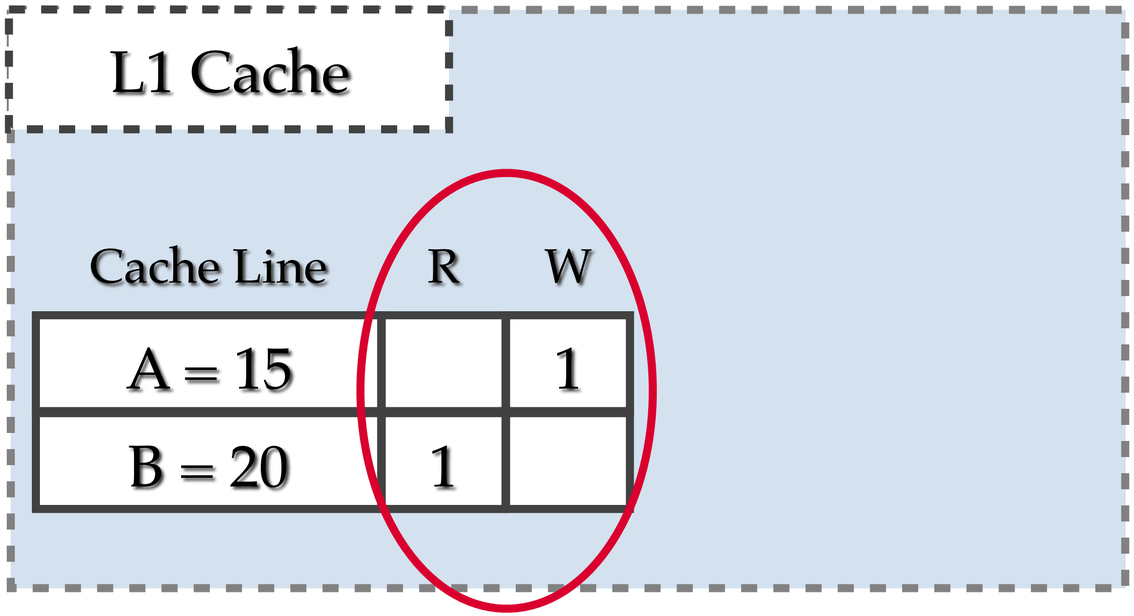

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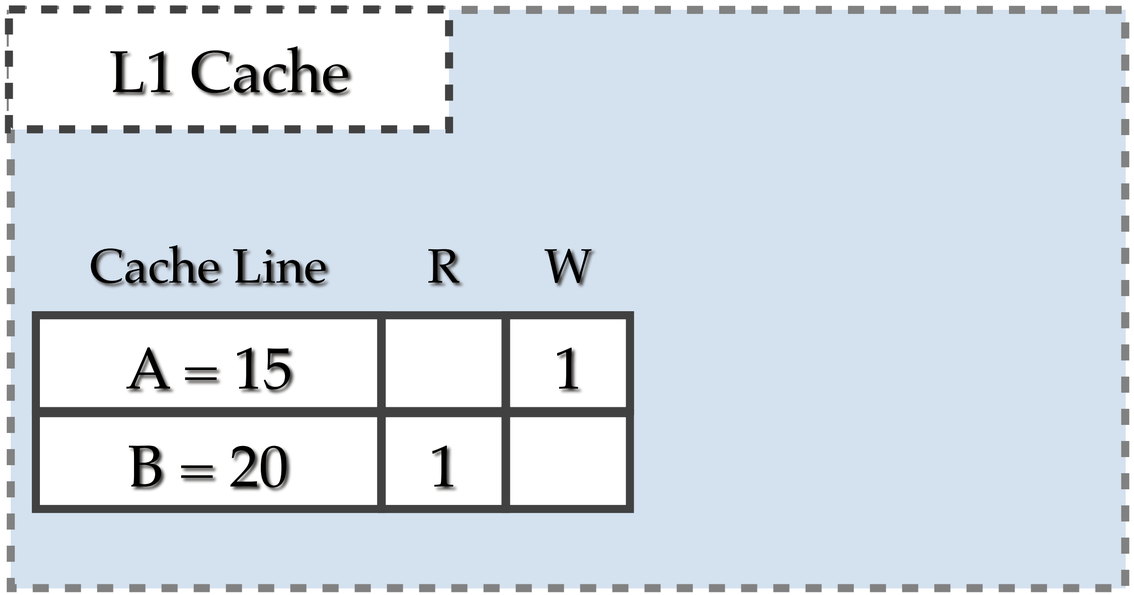

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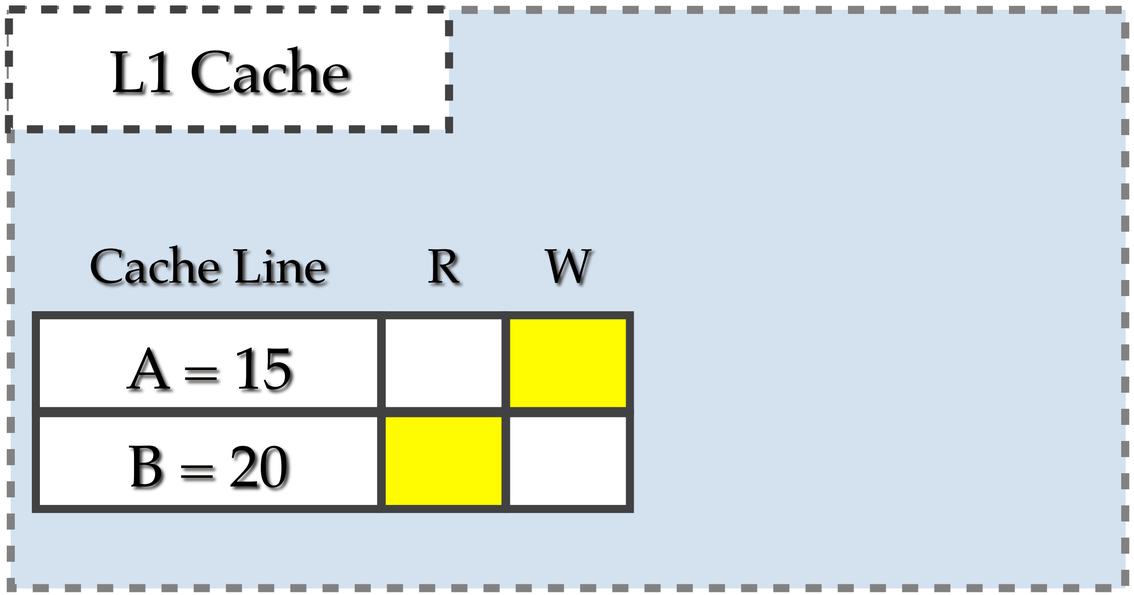

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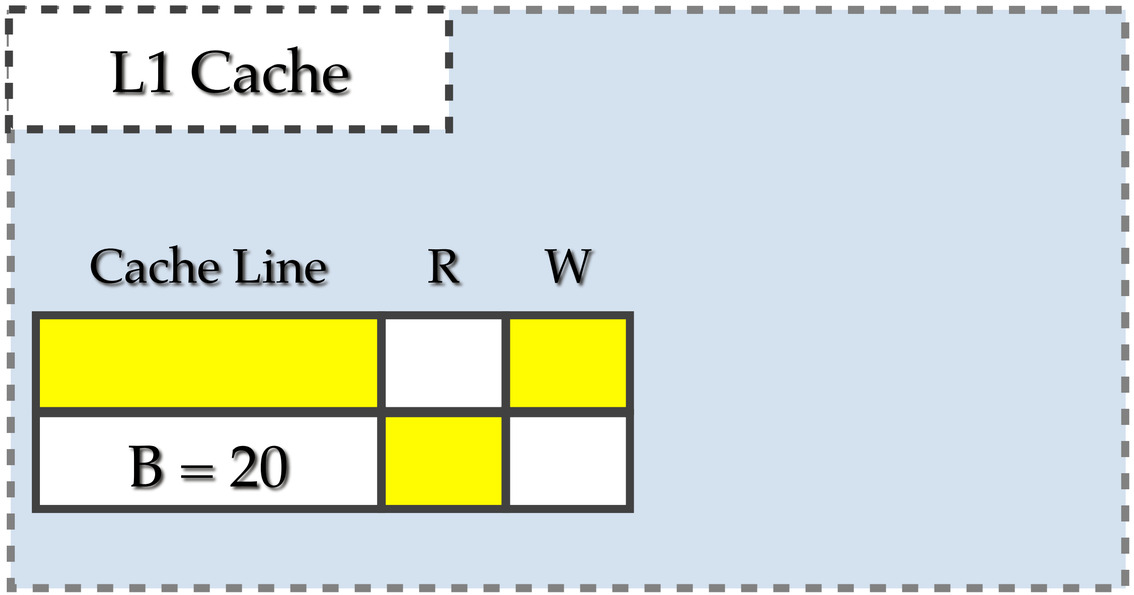

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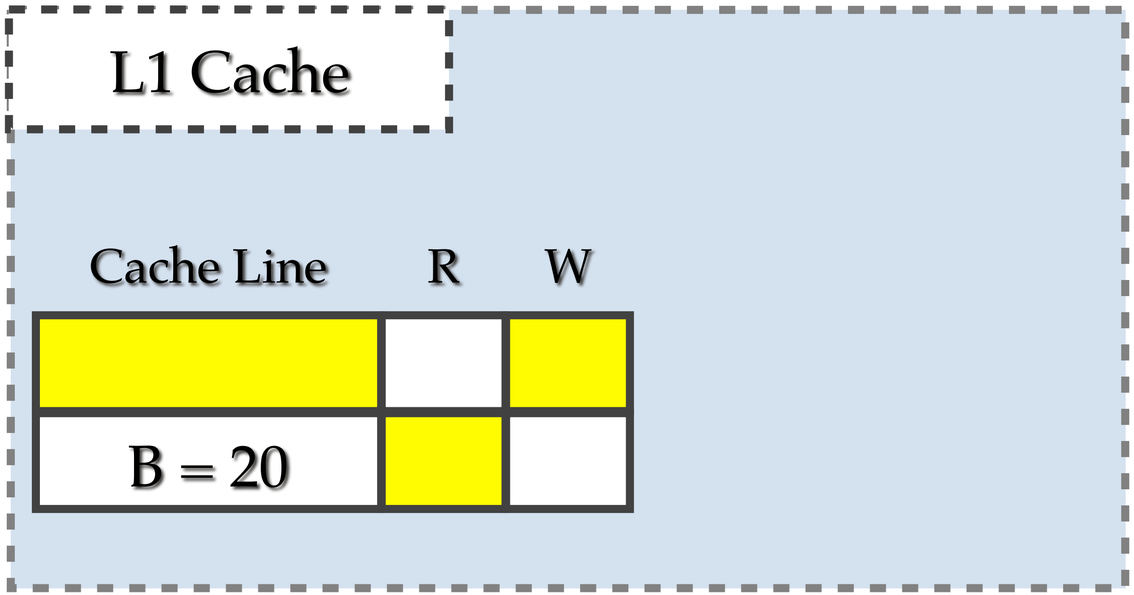

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✗ **Write-sets in commercial HTMs limited by the size of the L1 cache.**

Atomic Durability: Logging

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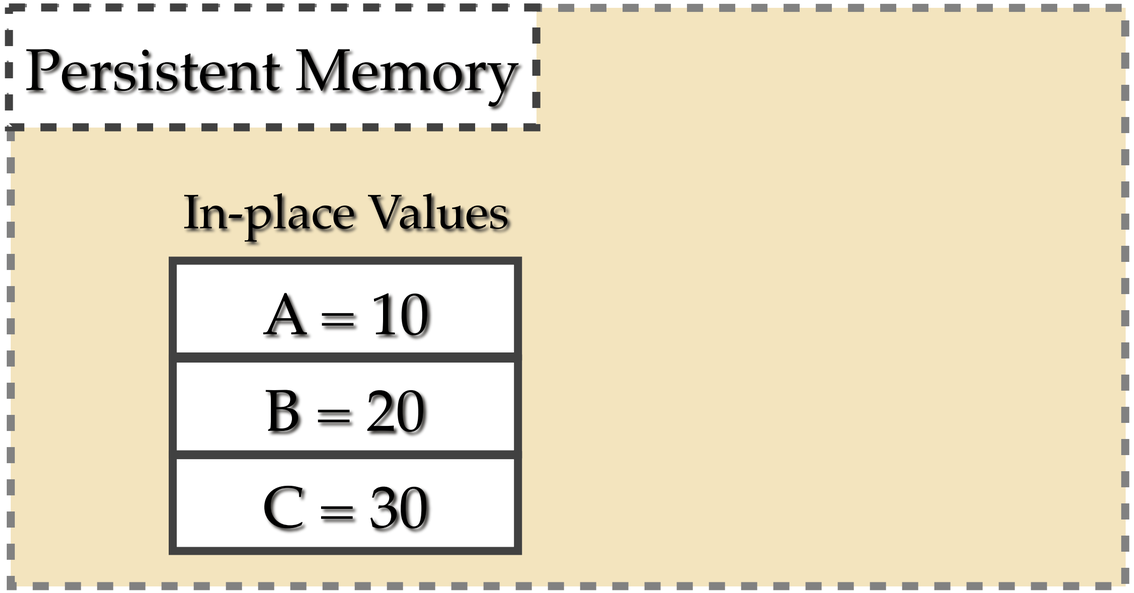

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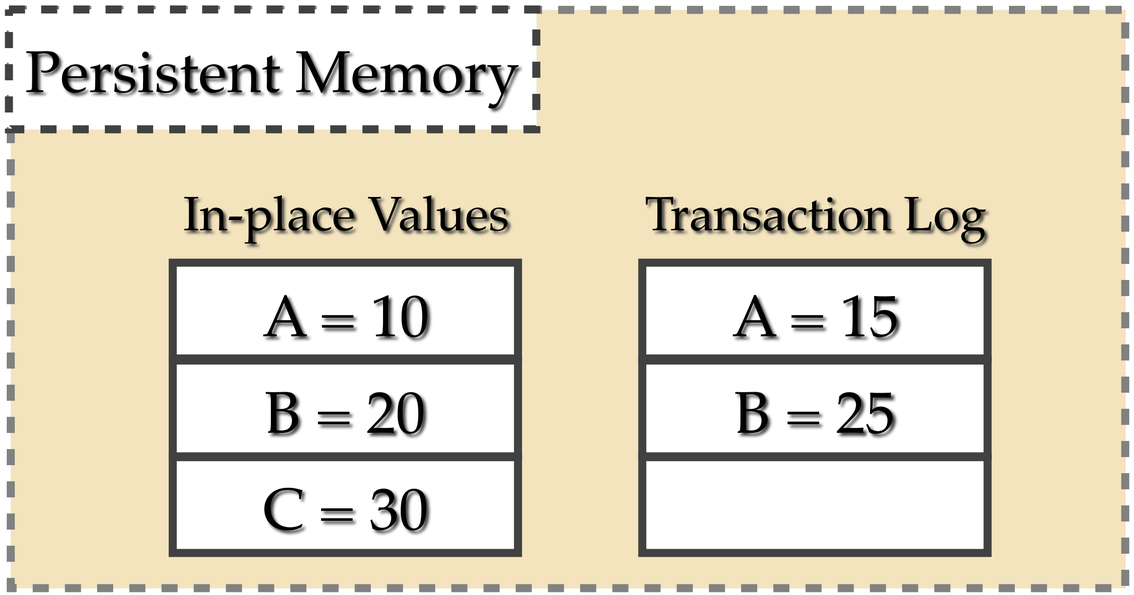

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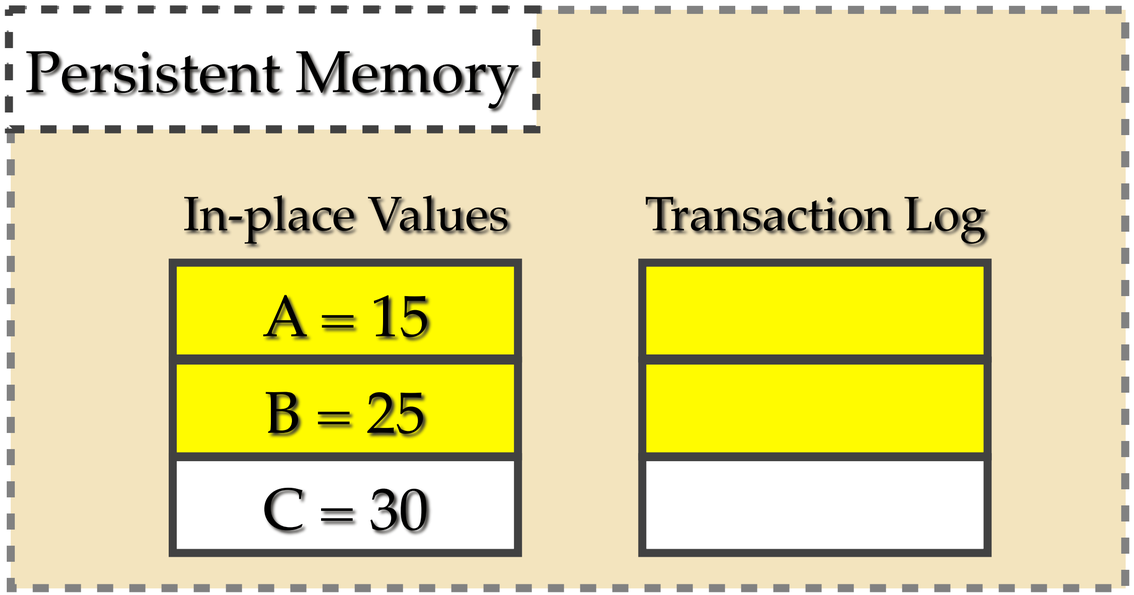

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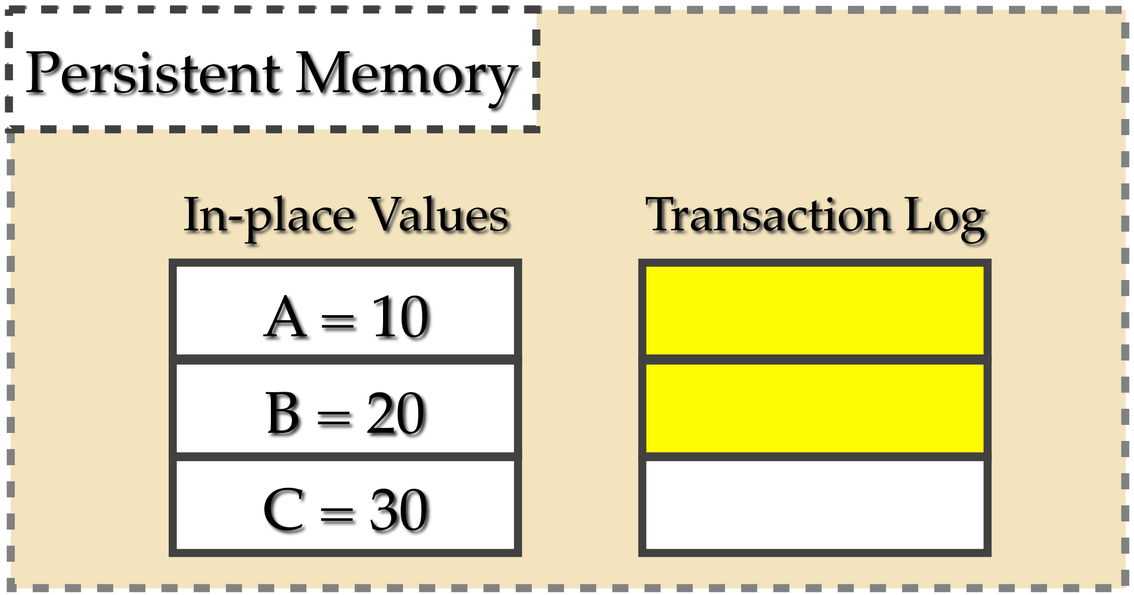

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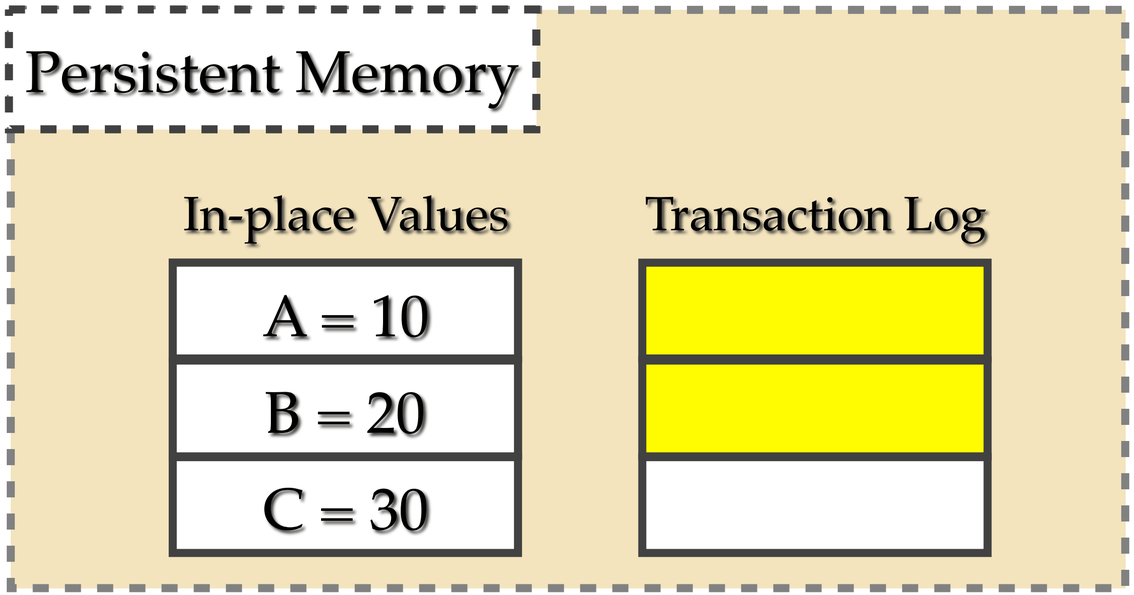

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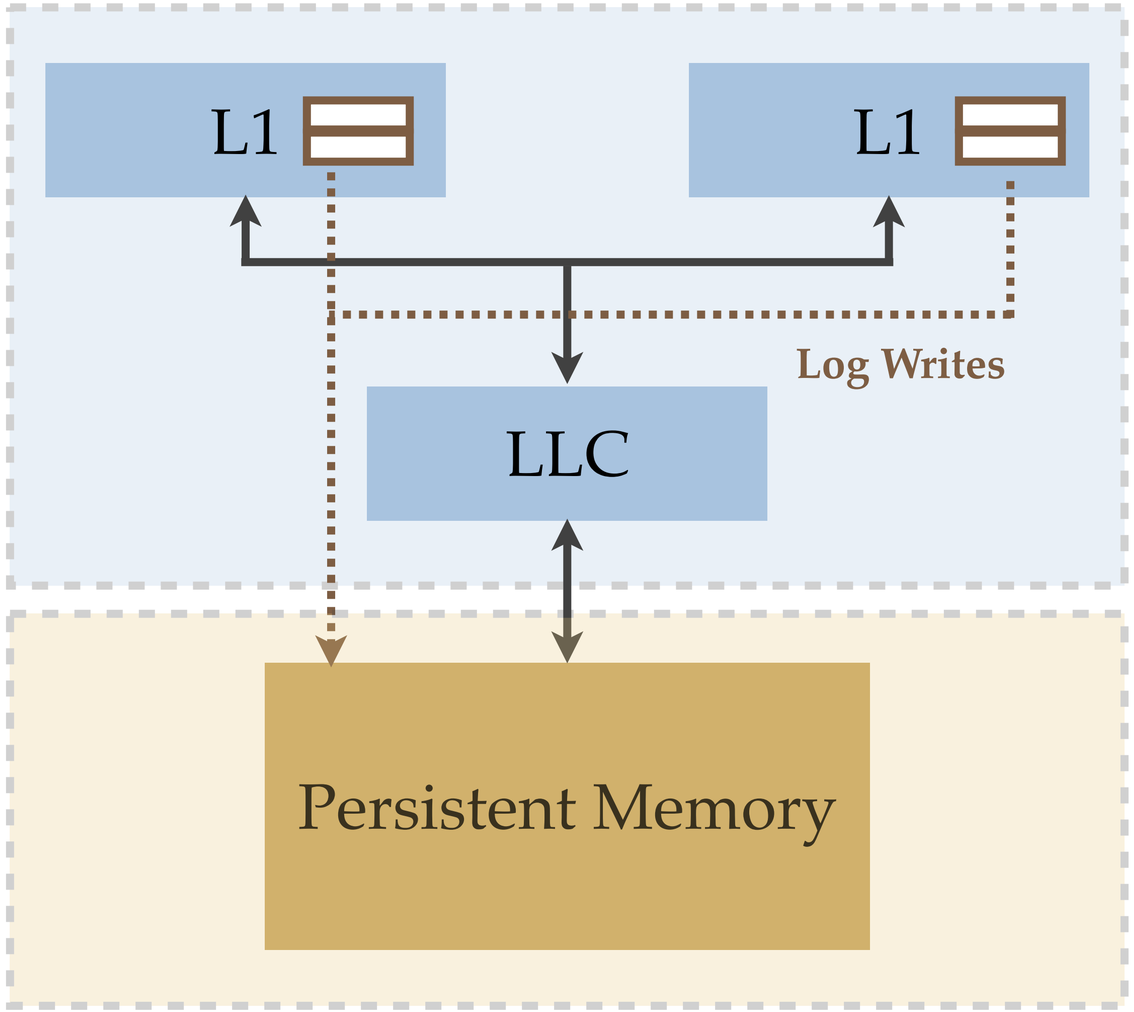
✗ In-place updates in the critical path of commit
✗ High memory write bandwidth requirement

ACID = HTM + Logging

Goals:

- Support fast commits
- Minimise memory bandwidth consumption
- Extend the supported transaction size
- Maintain the simplicity of commercial HTMs

DHTM: Durable Hardware Transactional Memory



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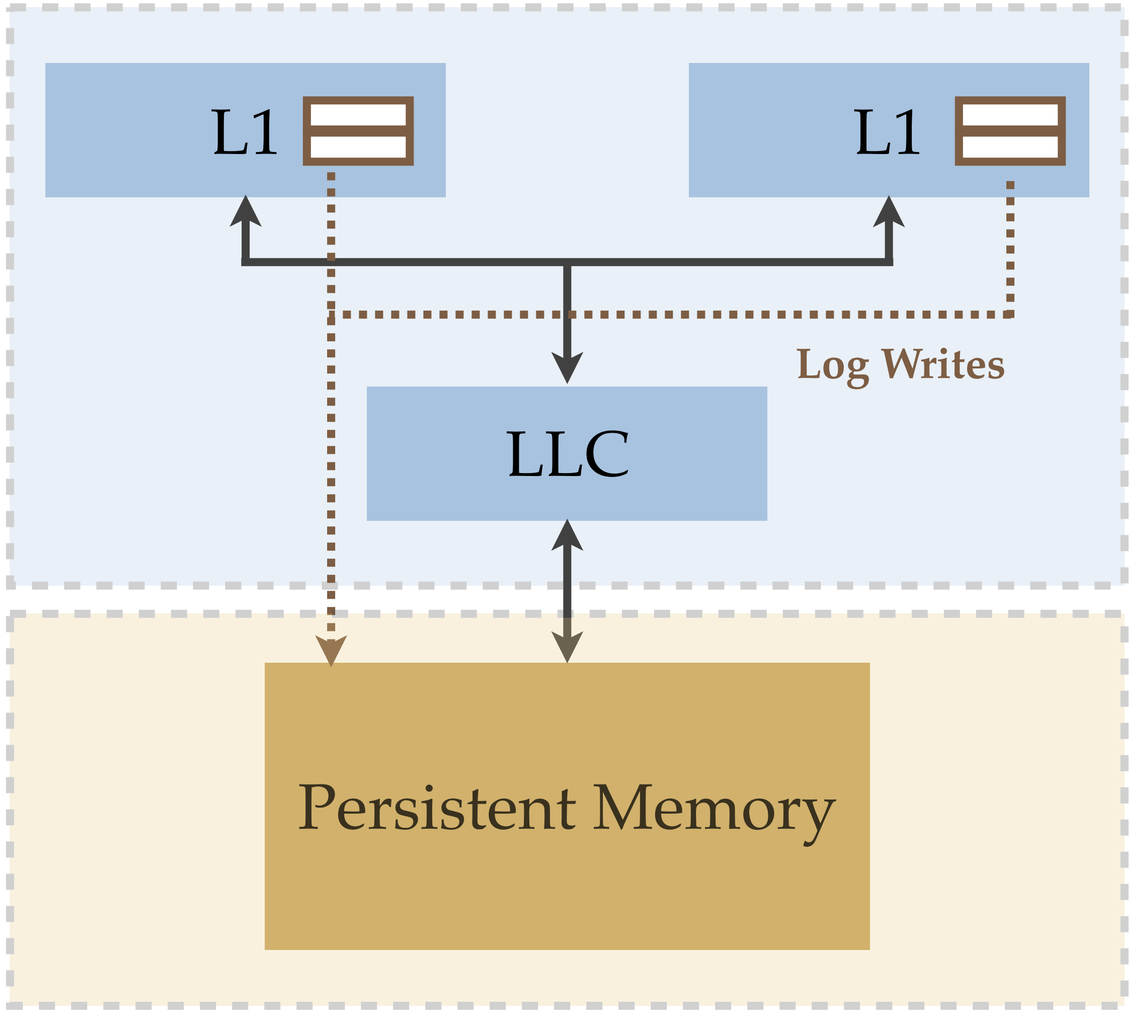

Commercial HTM + Hardware Redo Log

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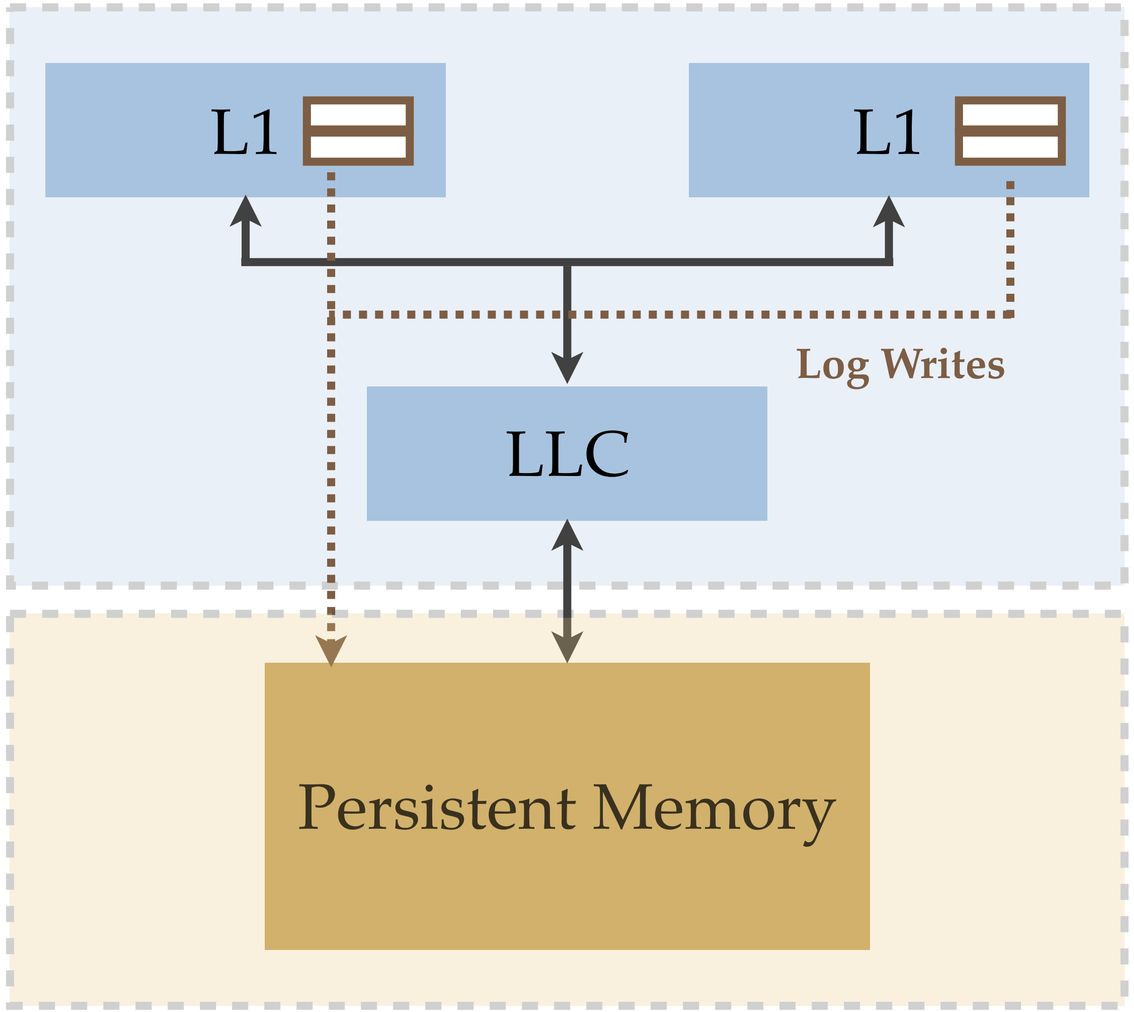

Commercial HTM + **Hardware Redo Log**

- H/W Redo Log + Log Buffer
  - ✓ Reduced memory bandwidth
  - ✓ Fast commits

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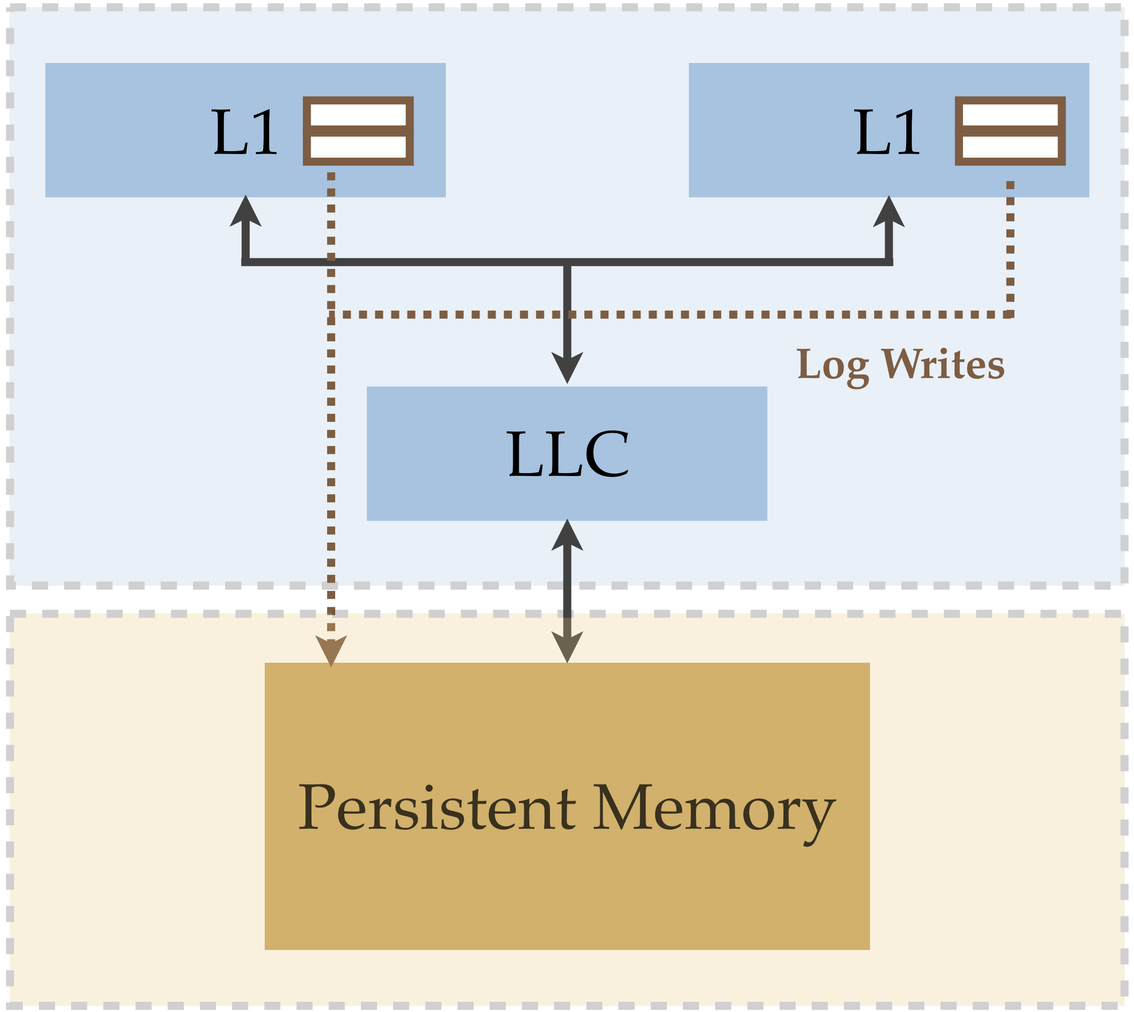
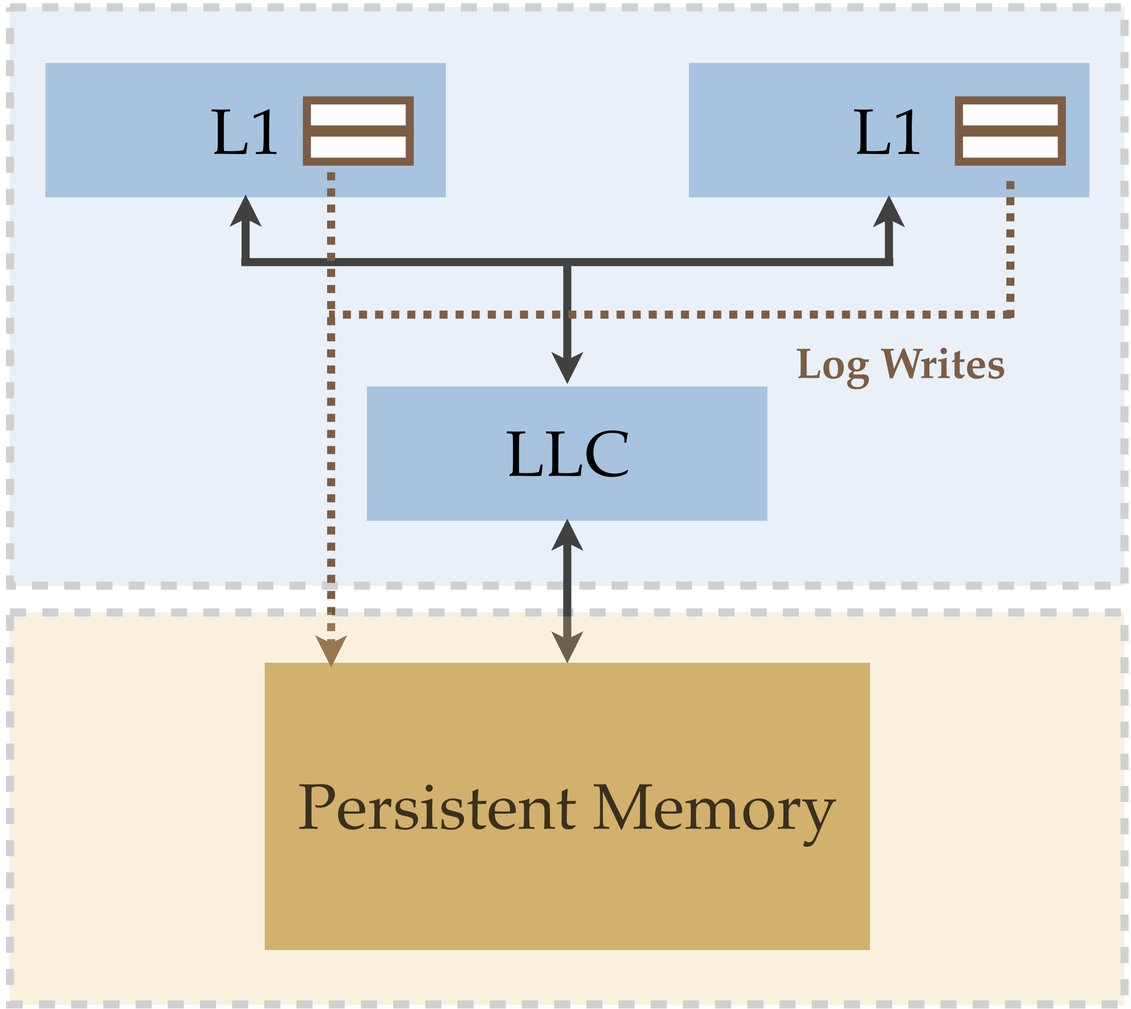


Commercial HTM + **Hardware Redo Log**

- H/W Redo Log + Log Buffer
  - ✓ Reduced memory bandwidth
  - ✓ Fast commits
- H/W Log + Sticky State
  - ✓ Extended transaction size to the LLC
  - ✓ Simplicity of commercial HTM

DHTM: Log Buffer



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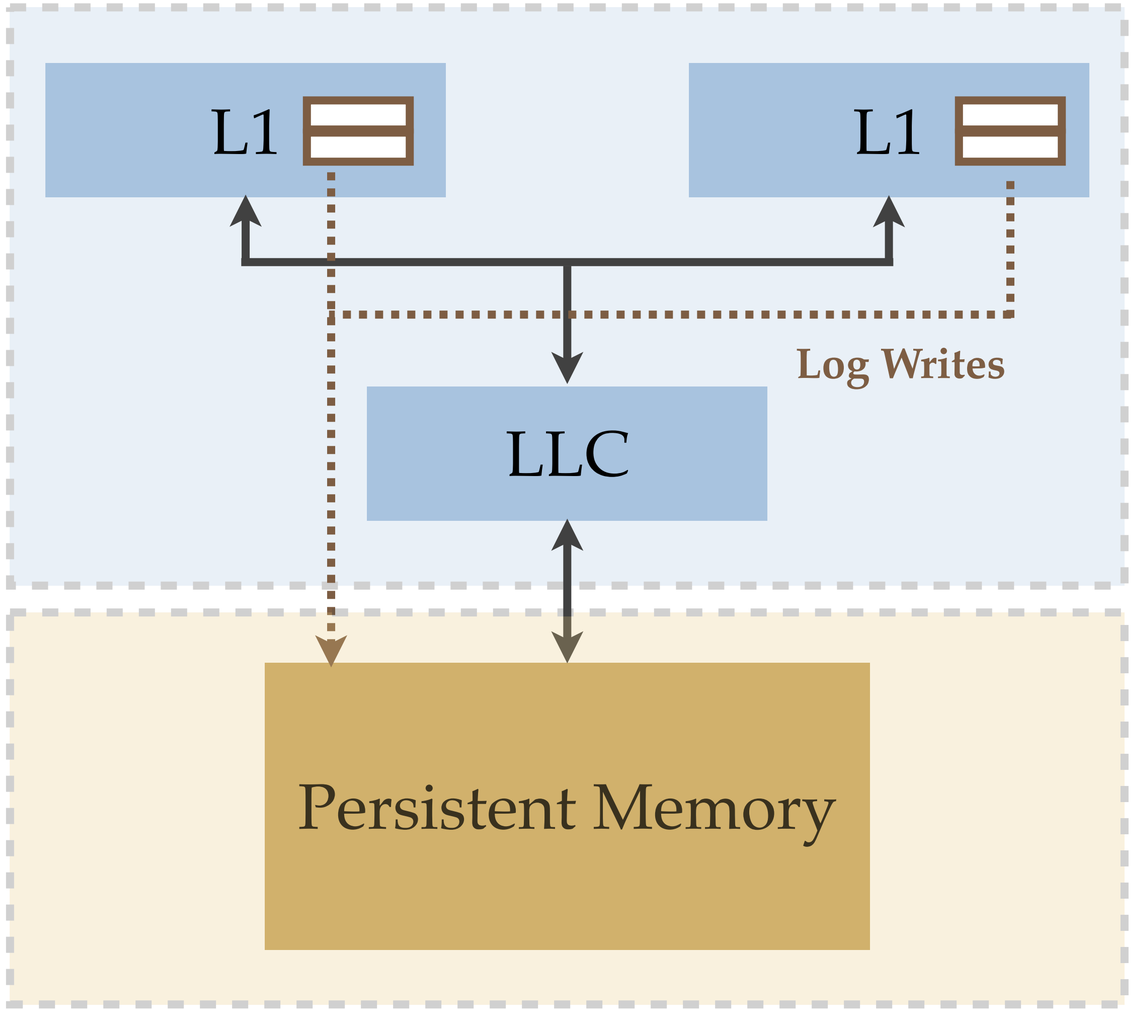
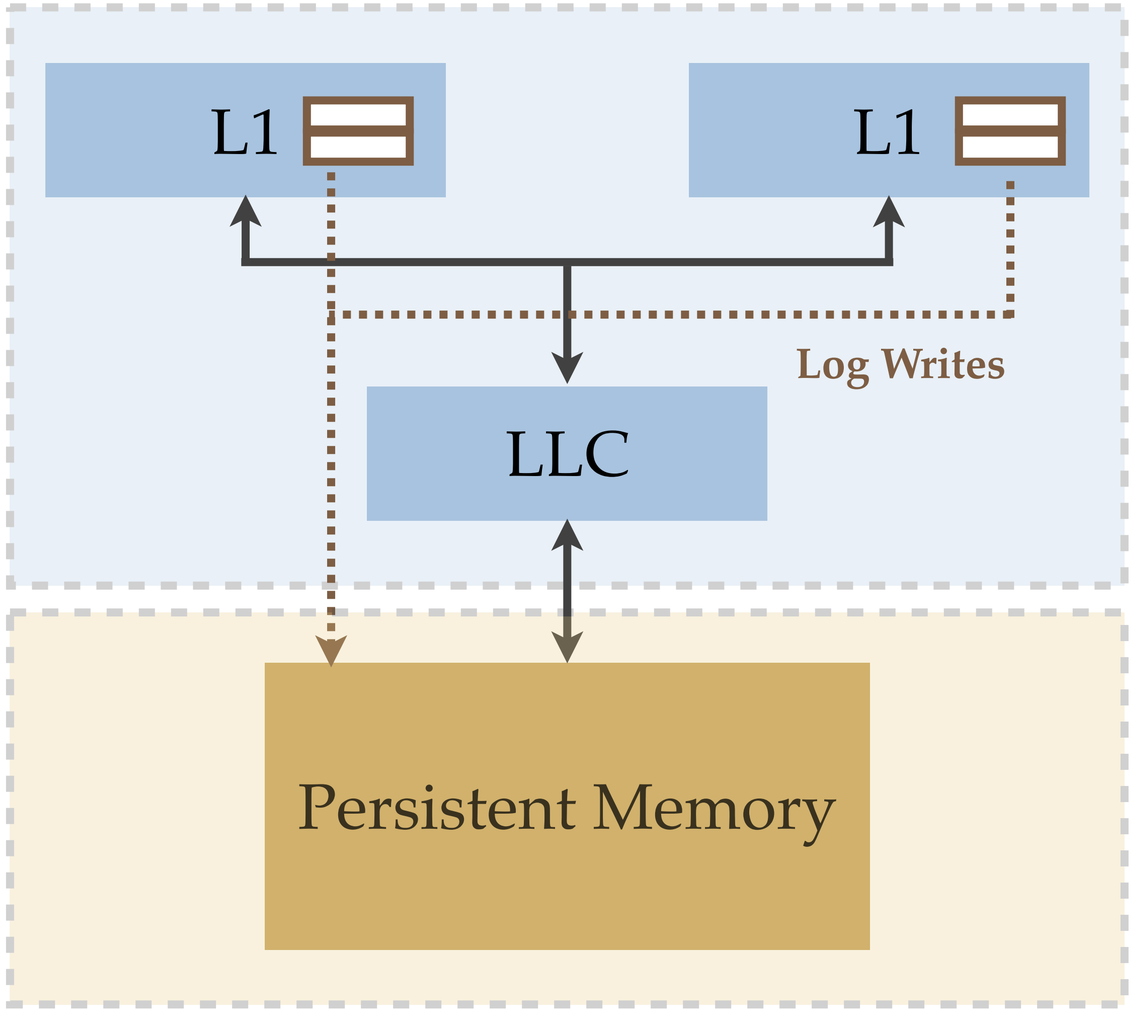


- **Redo Log Bandwidth Problem**

DHTM: Log Buffer



- **Redo Log Bandwidth Problem**
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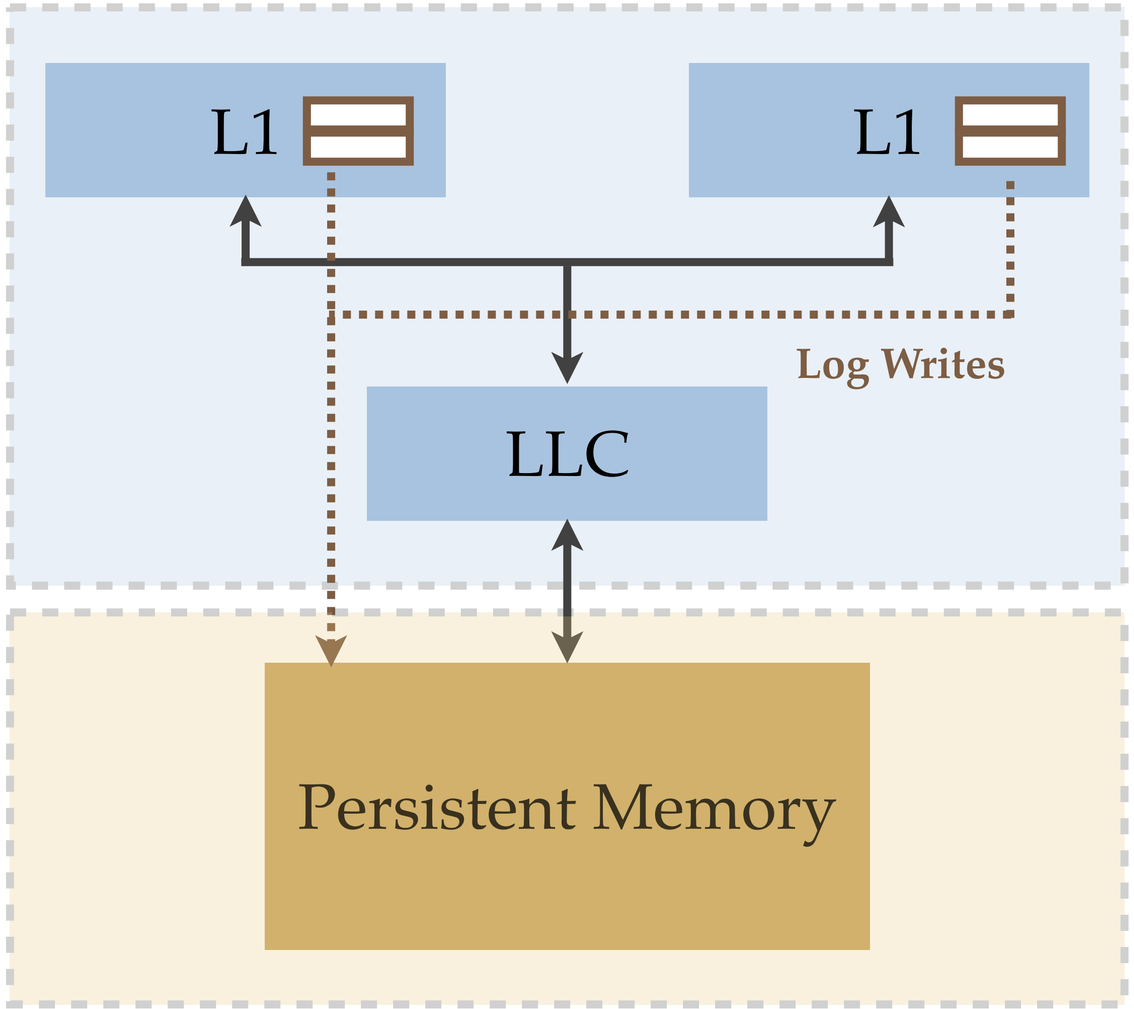

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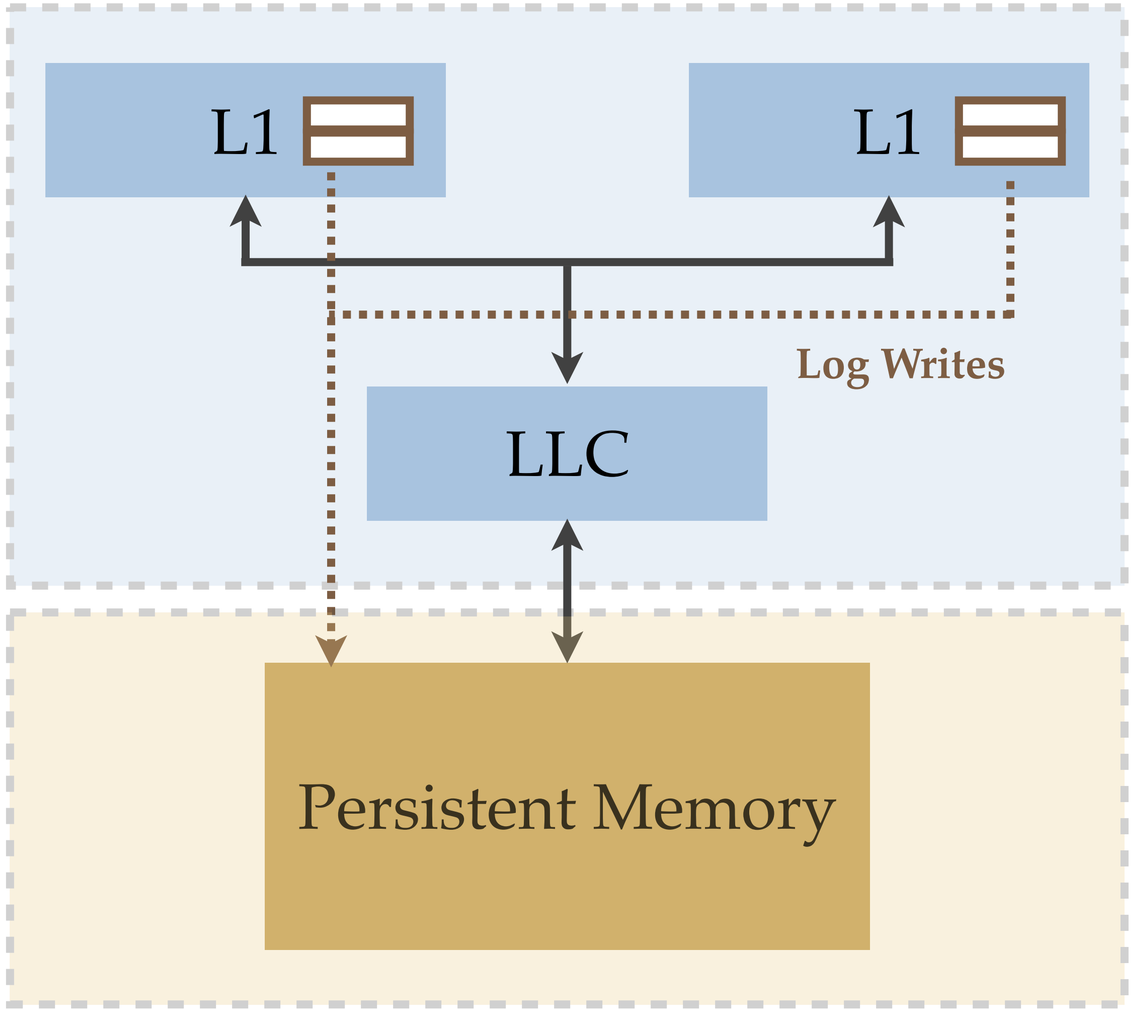

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- **Solution: Log Buffer**

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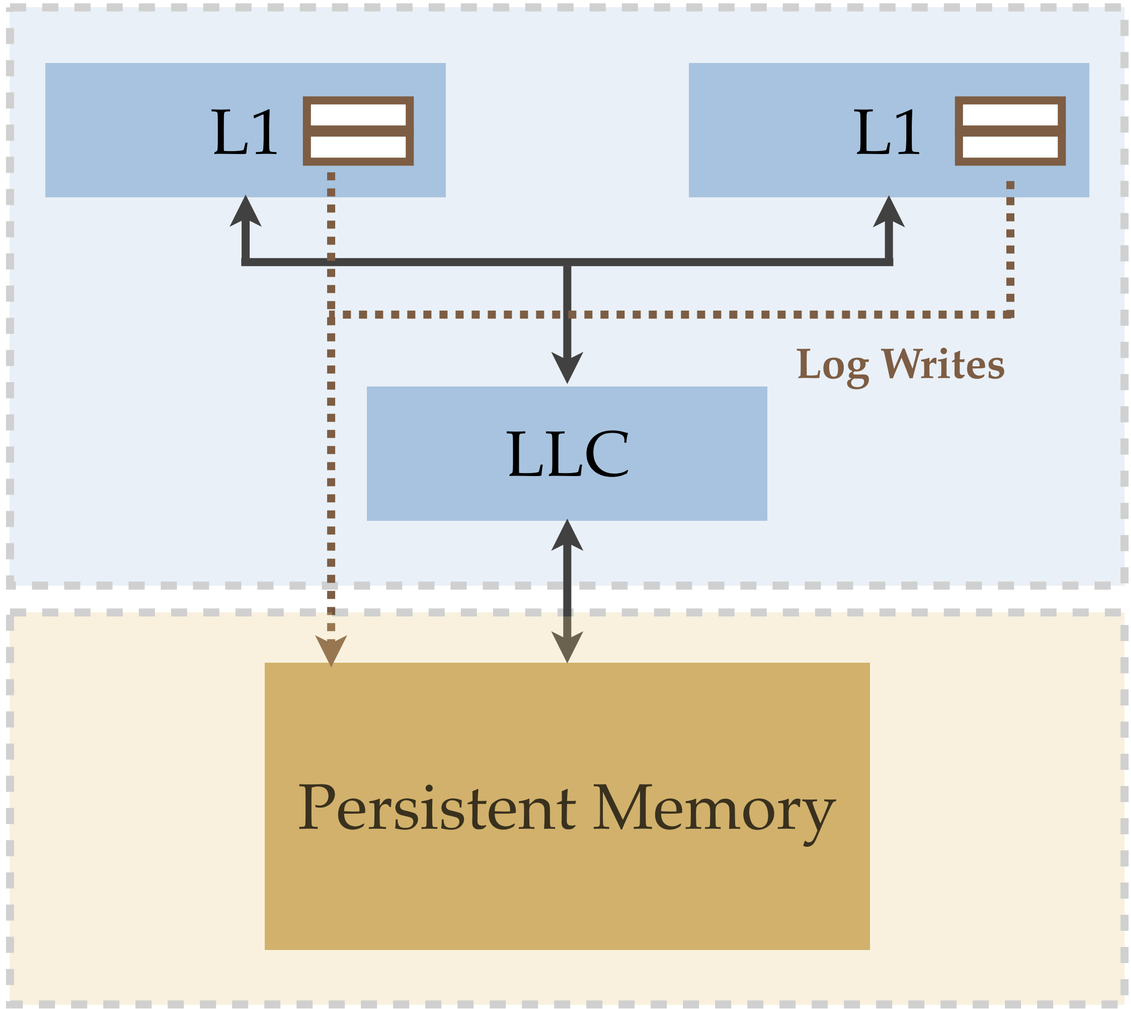

- **Redo Log Bandwidth Problem**
  - write a log entry for every store
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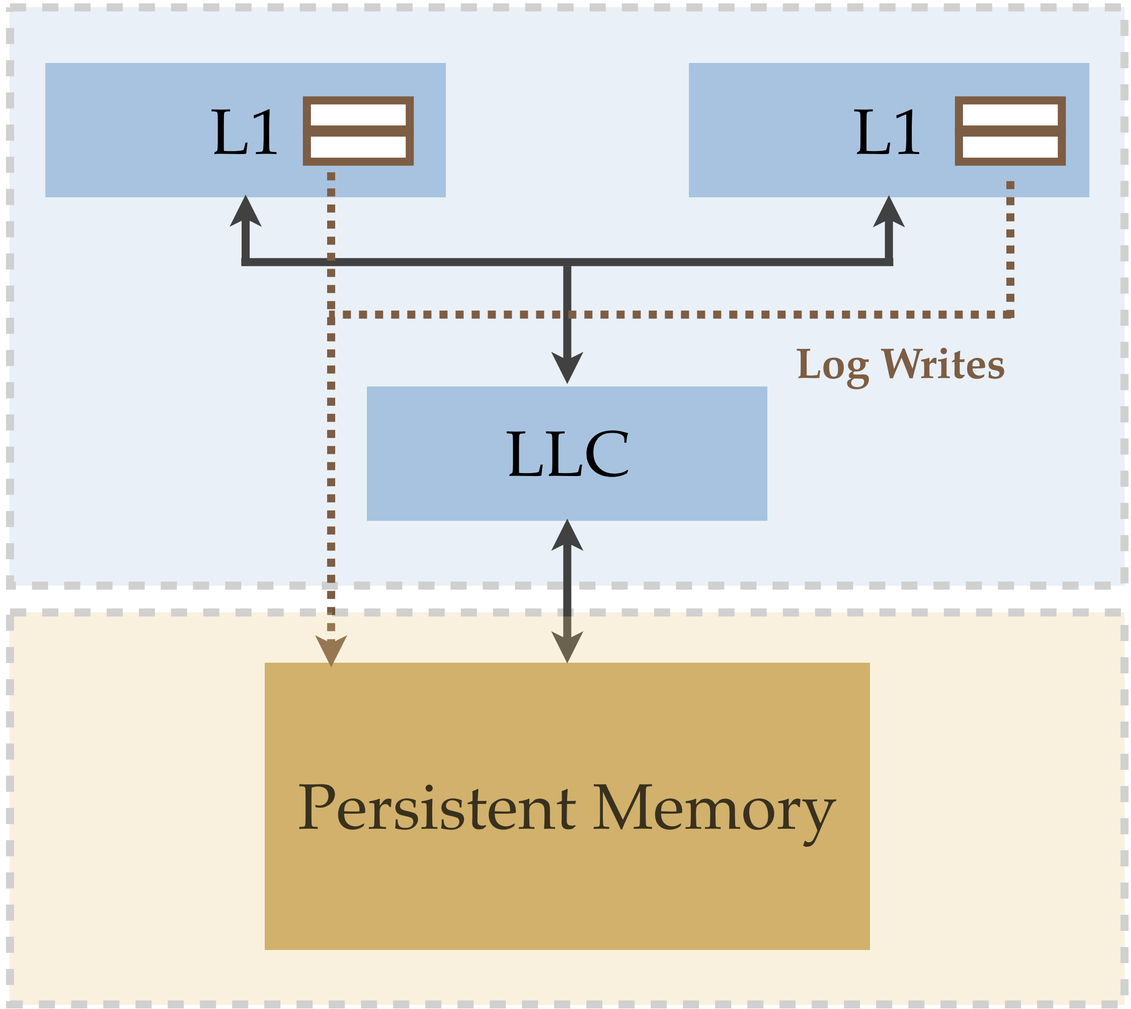
- **Solution: Log Buffer**
  - track cache lines being modified

DHTM: Log Buffer



- **Redo Log Bandwidth Problem**
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  - track cache lines being modified
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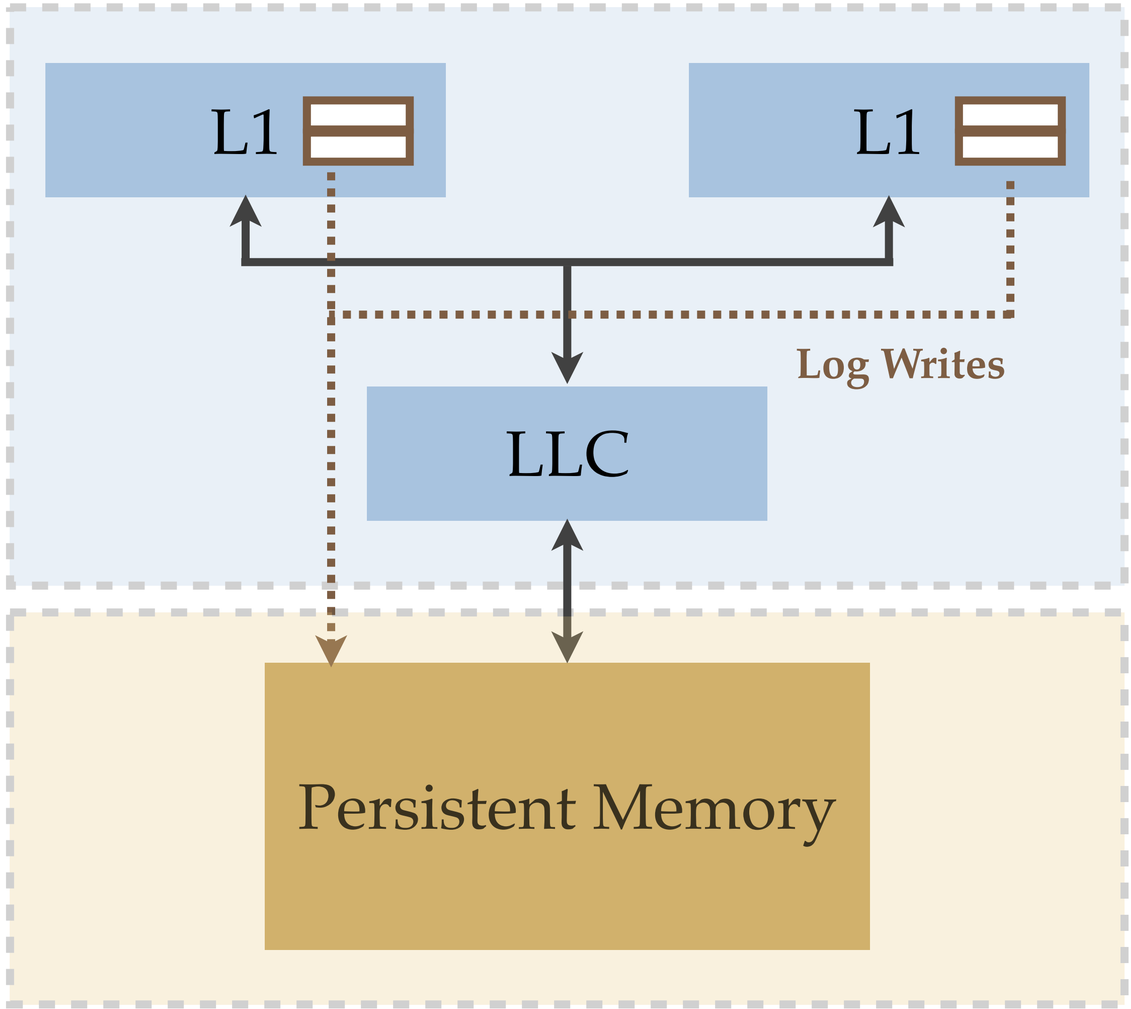
DHTM: Log Buffer



- **Redo Log Bandwidth Problem**
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  - log entry written to persistent memory on eviction from log buffer

DHTM: Transaction States

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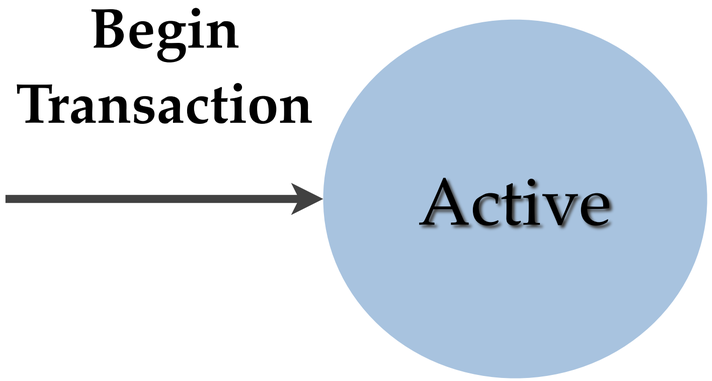

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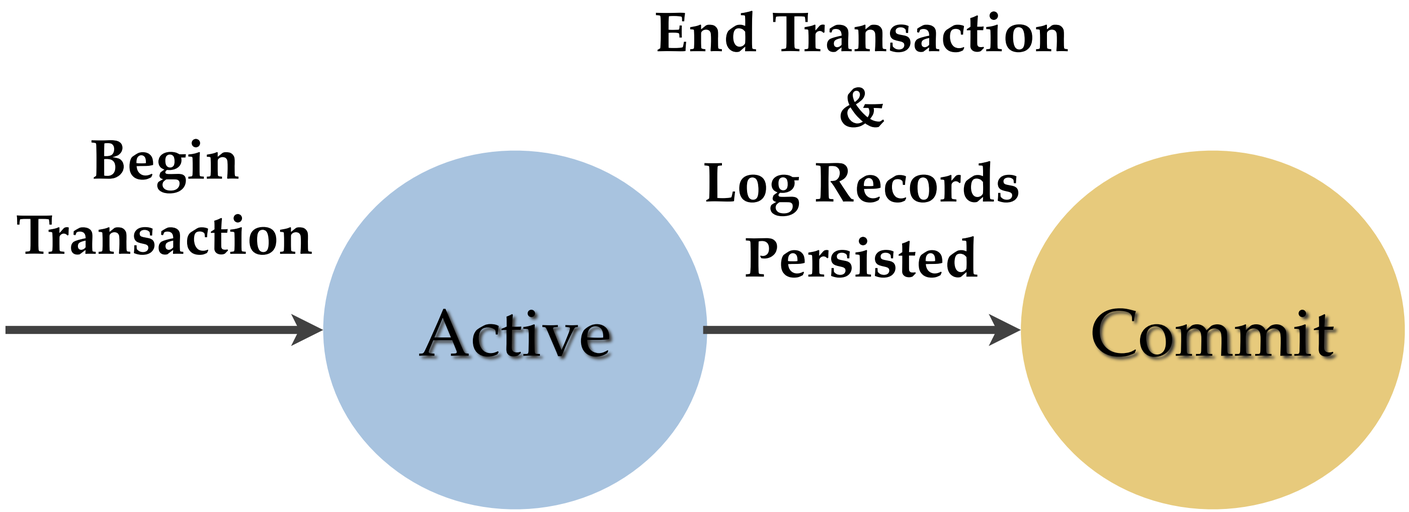

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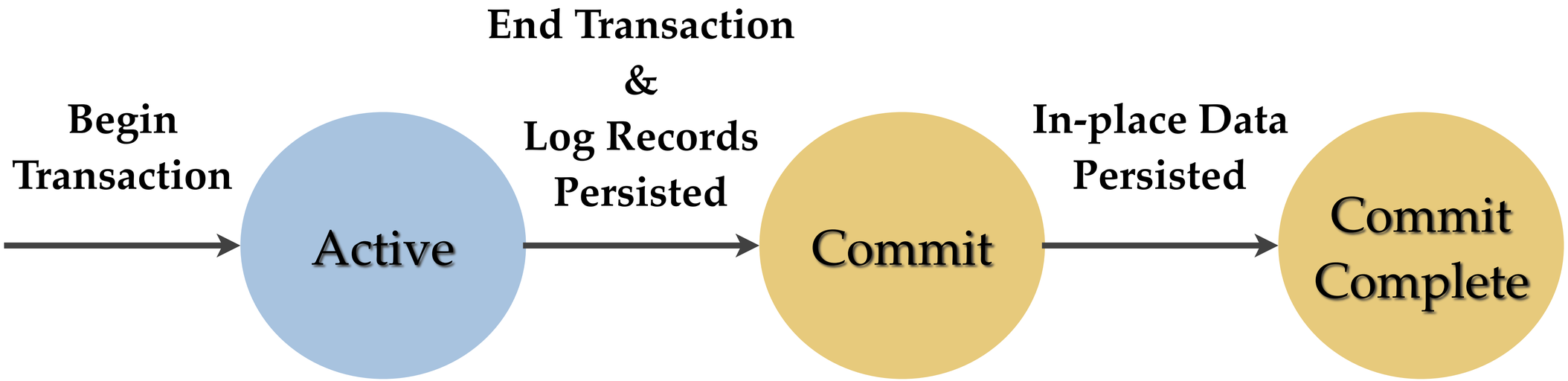

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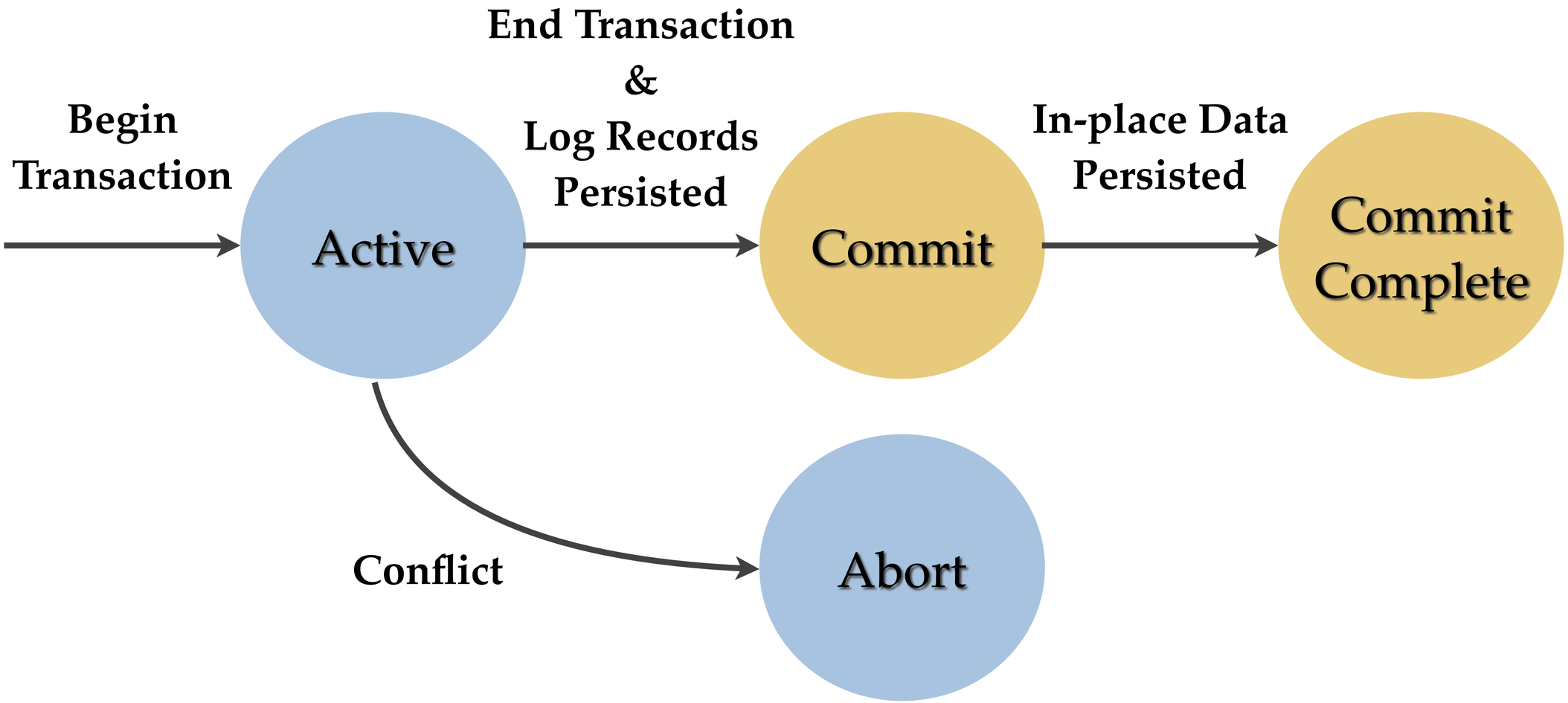
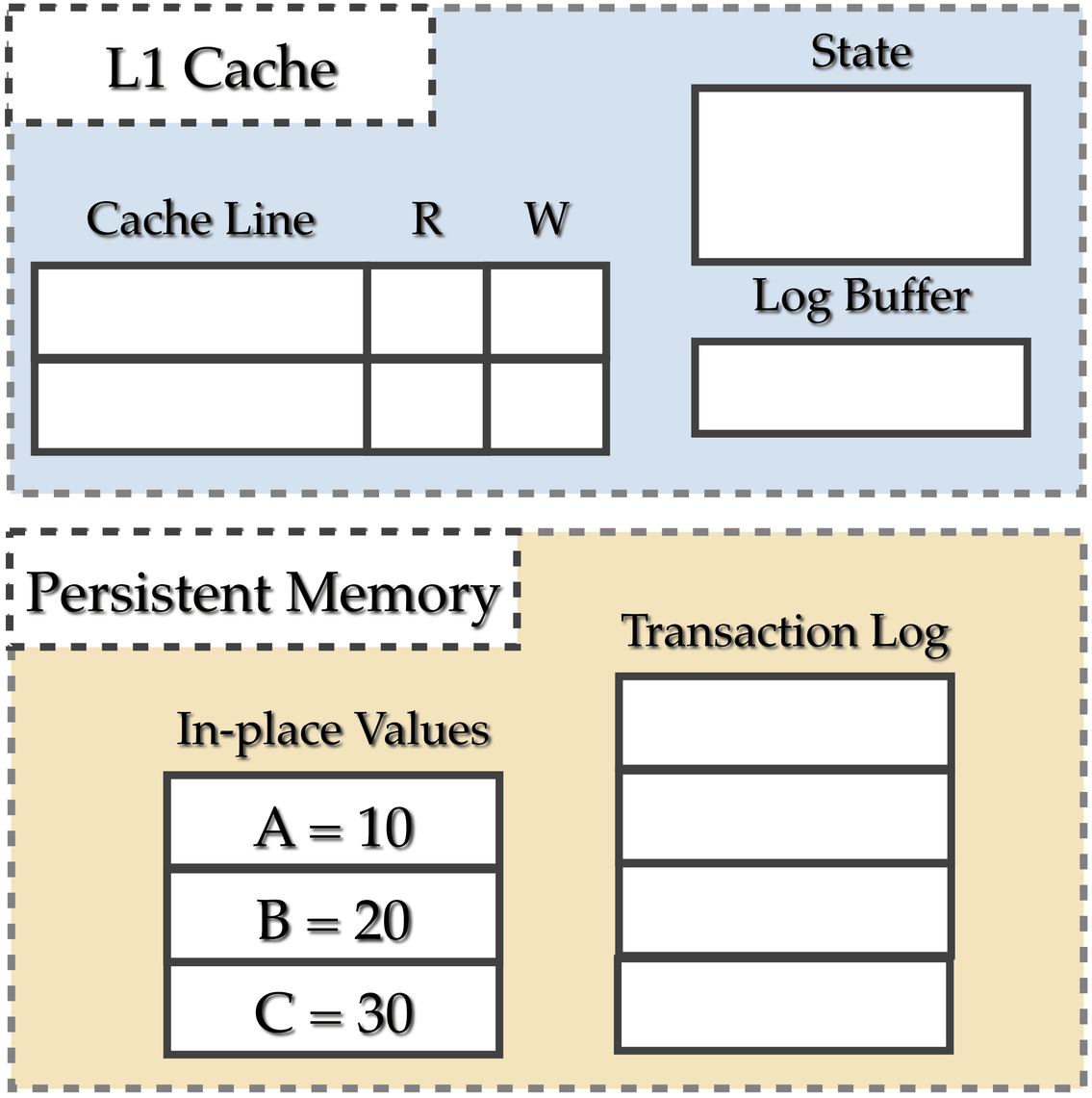


DHTM: Commit Example

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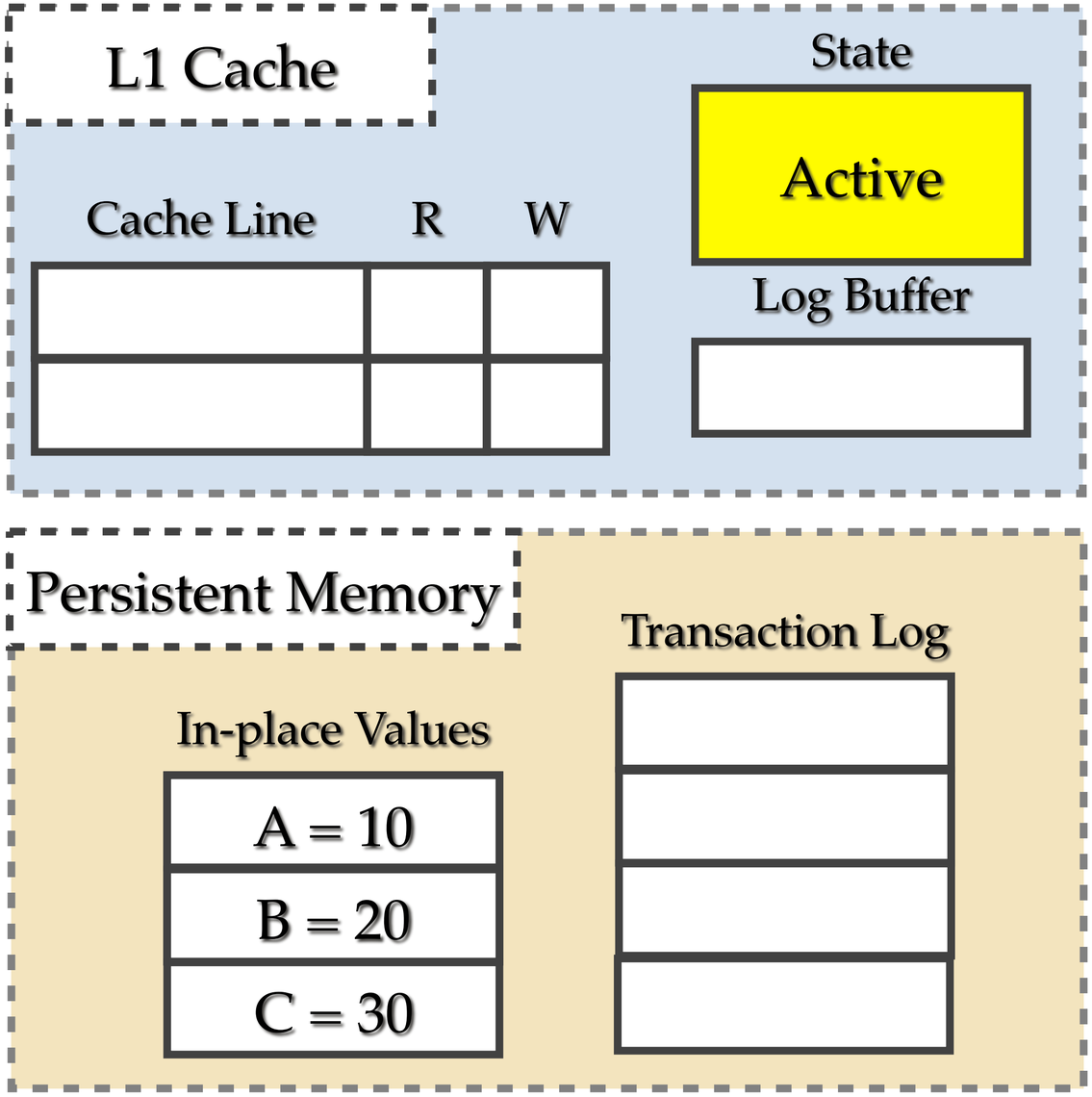


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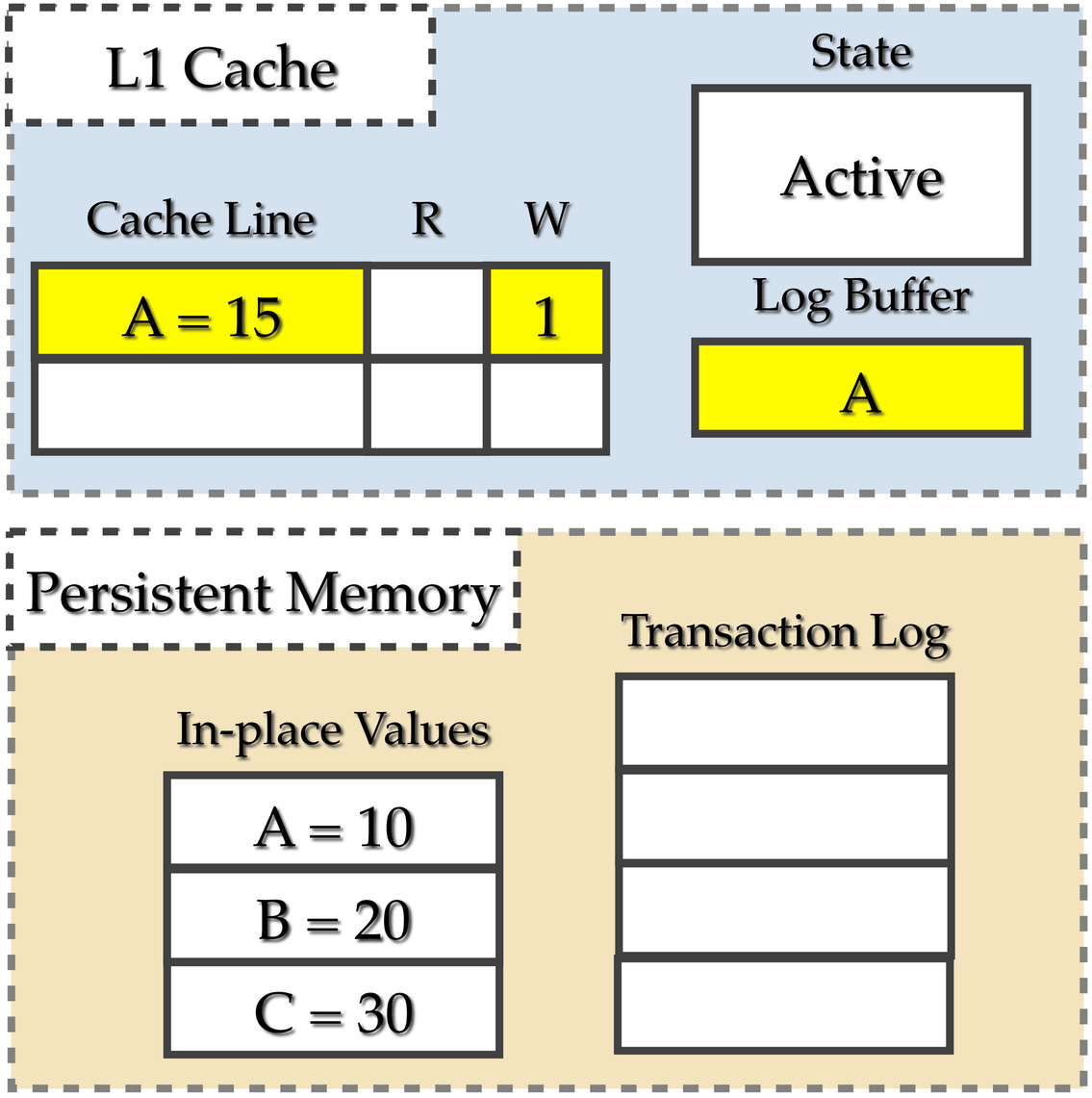


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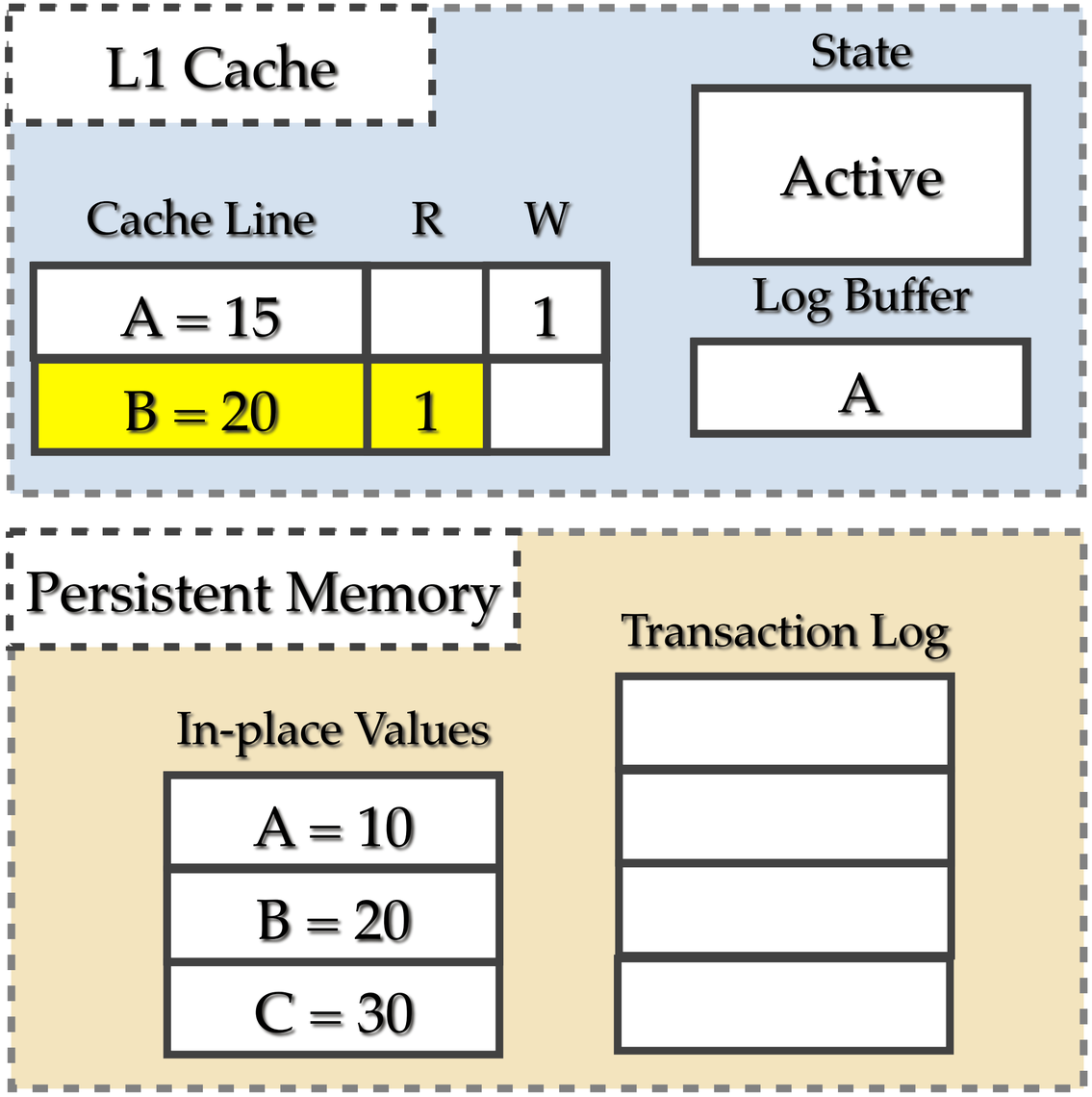


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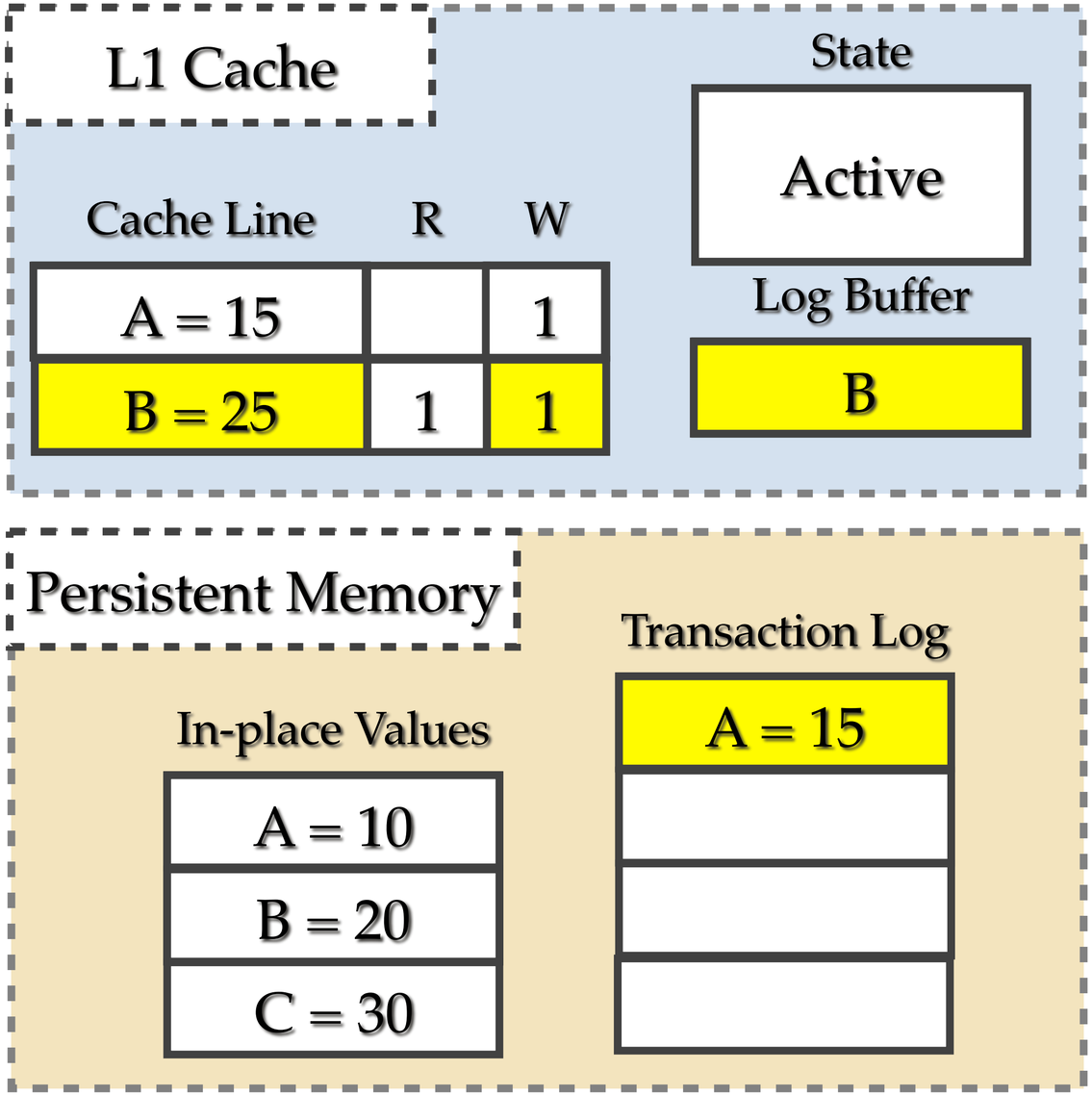


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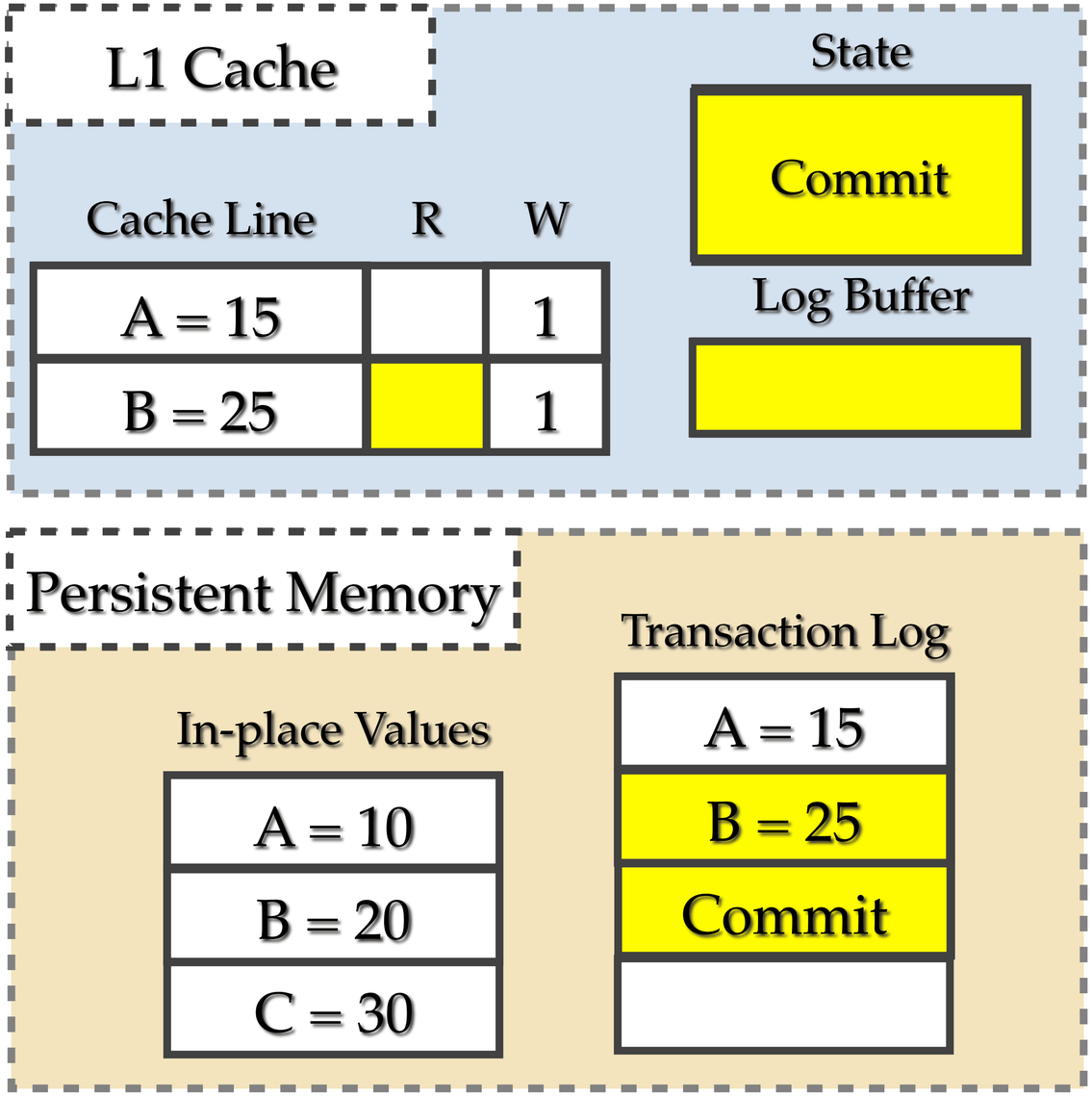


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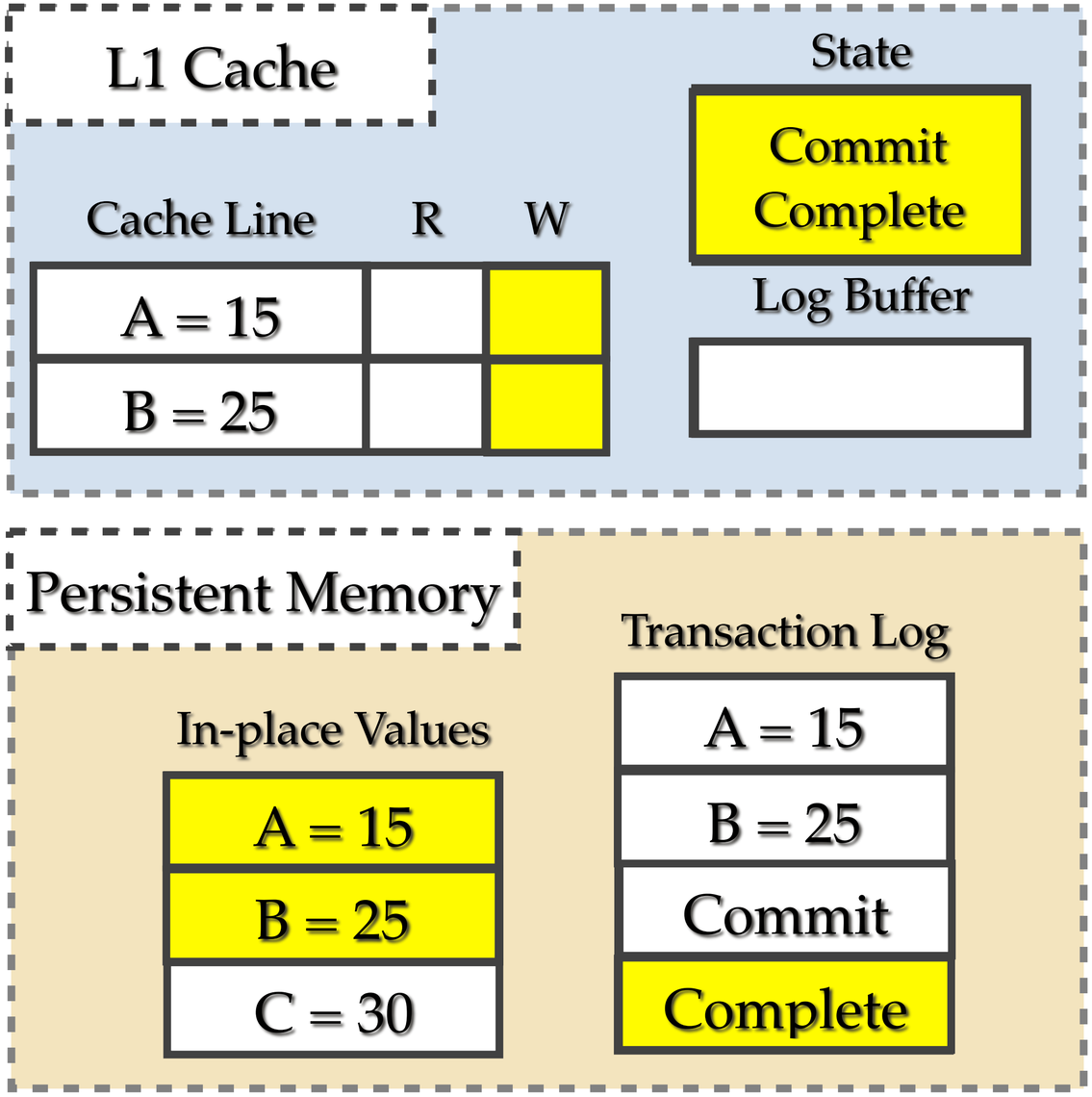


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    - overhead infeasible in larger caches (beyond L1)
  - **Conflict Detection**:
    - additional metadata to detect conflicts
    - increased complexity due to NACK based protocols

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- Solution

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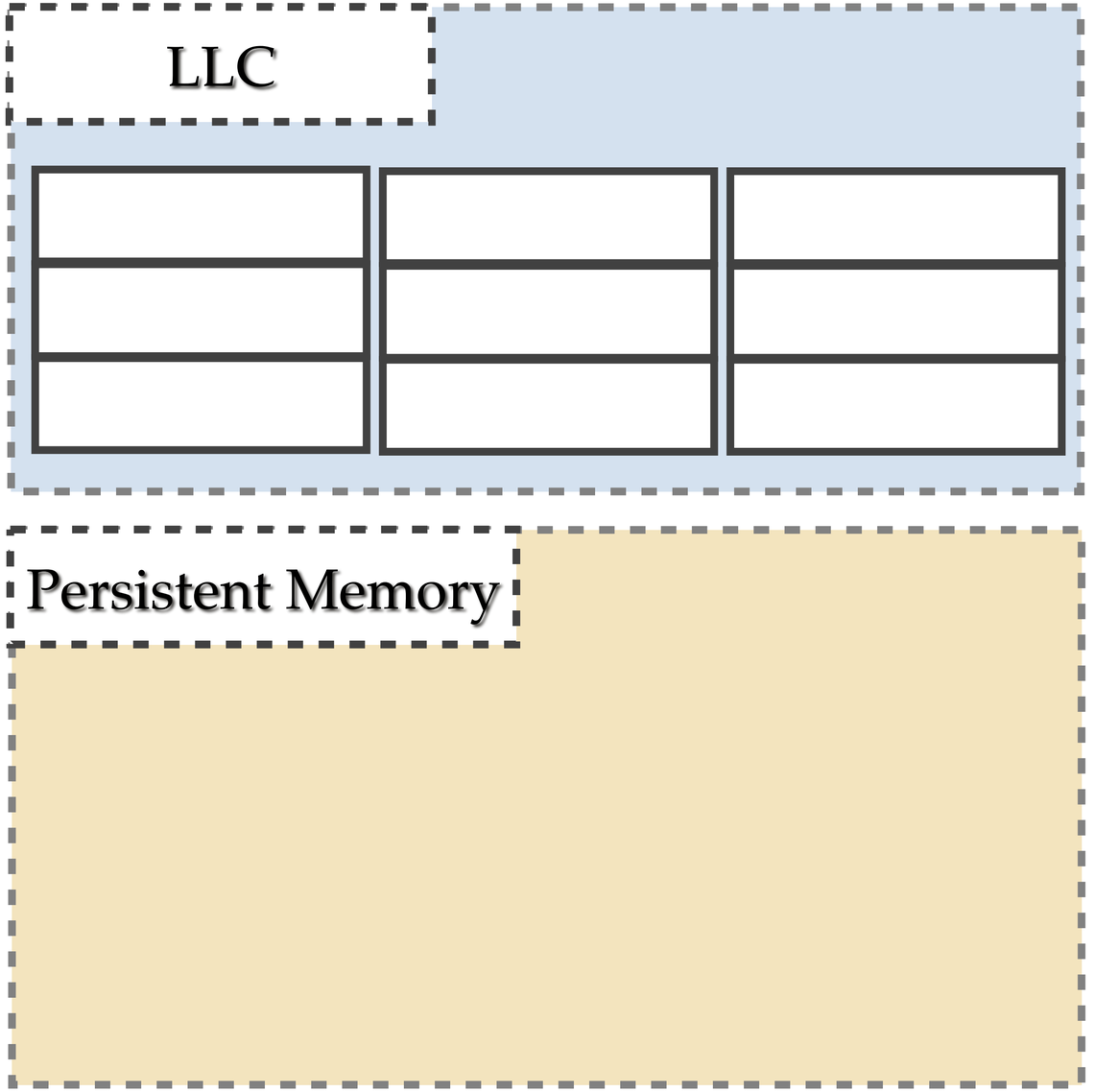
- **Solution**
  - **Version Management**:
    - Overflow List



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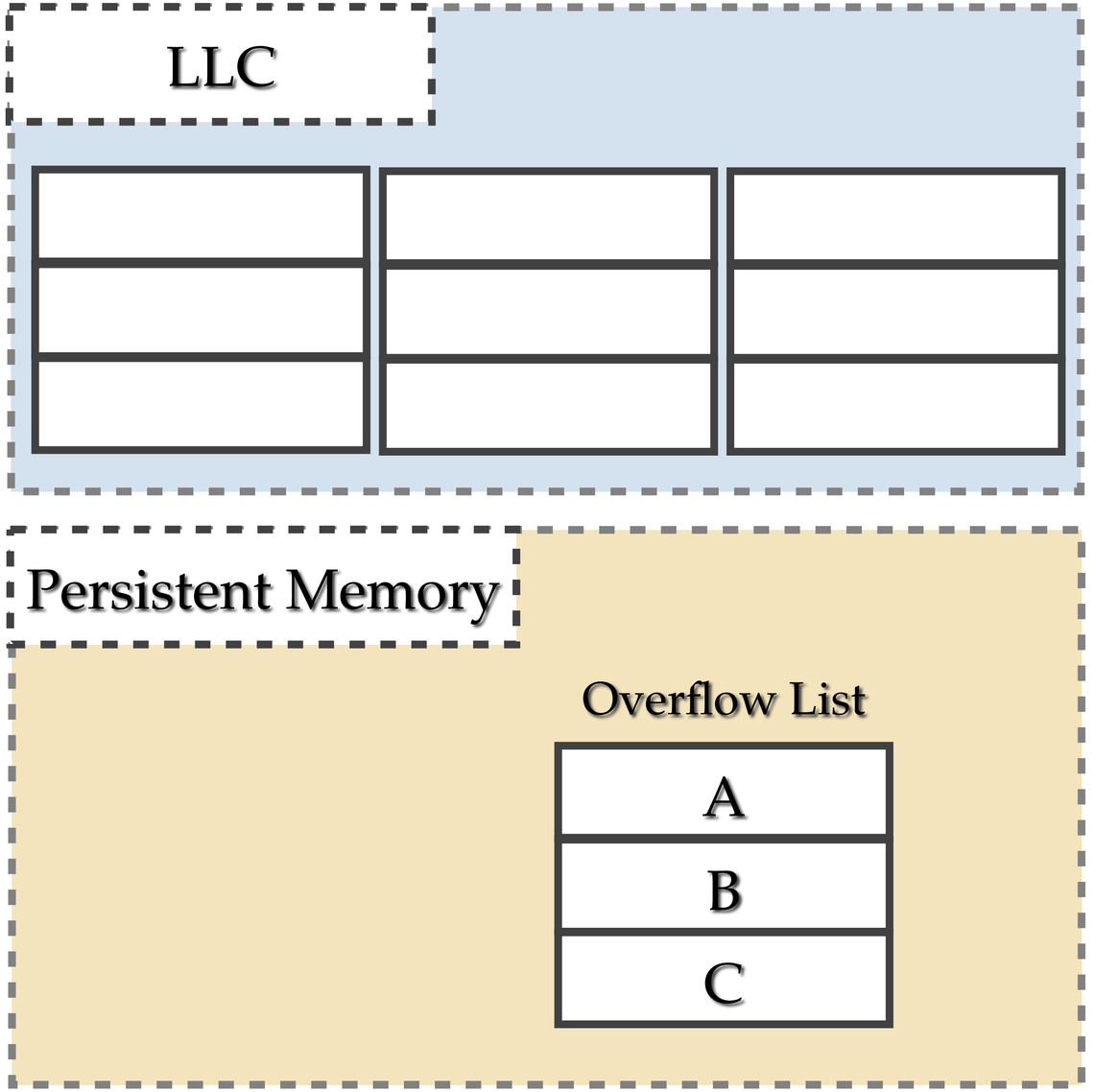

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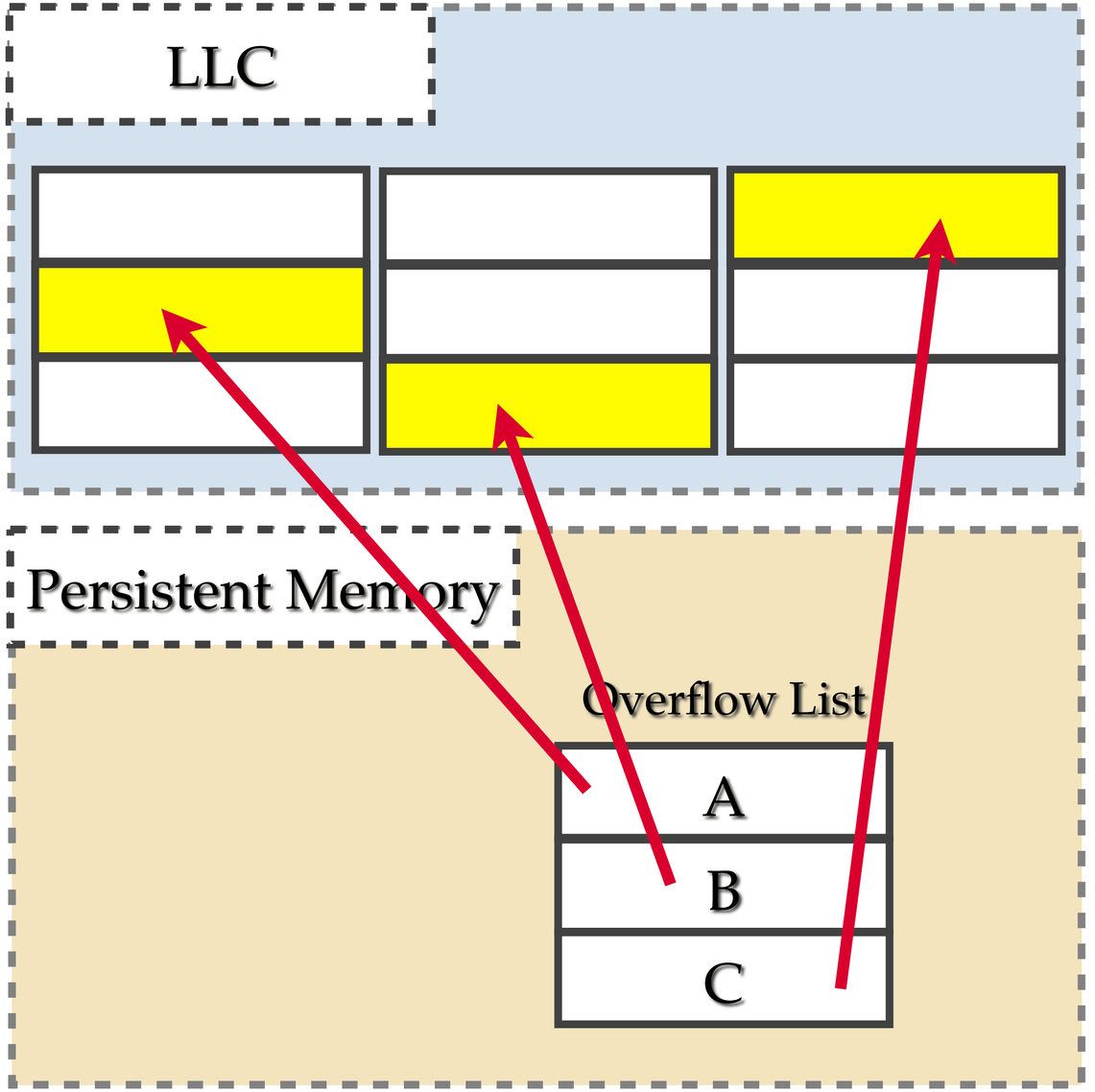

DHTM: Supporting Overflow

- **Solution**
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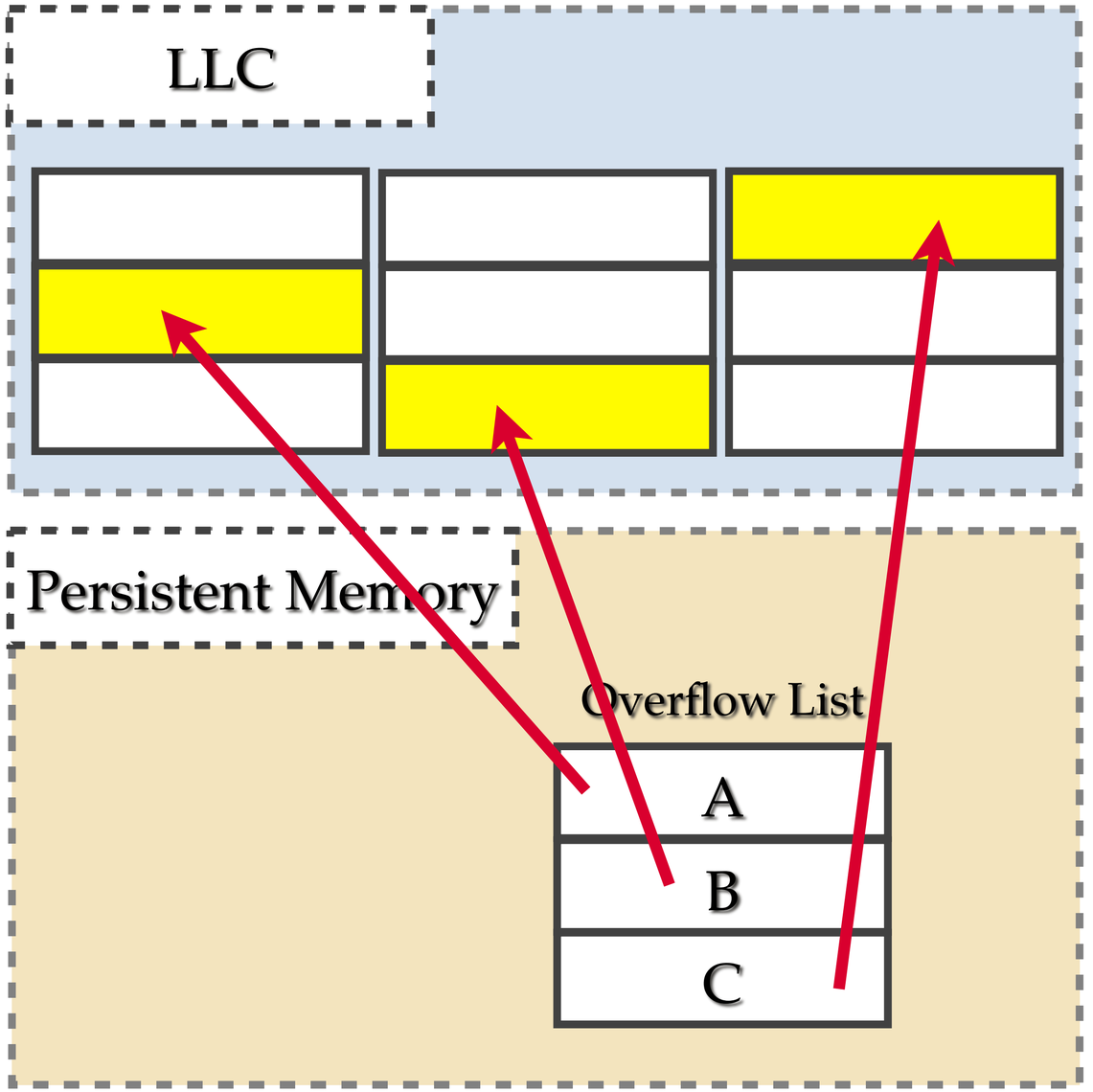

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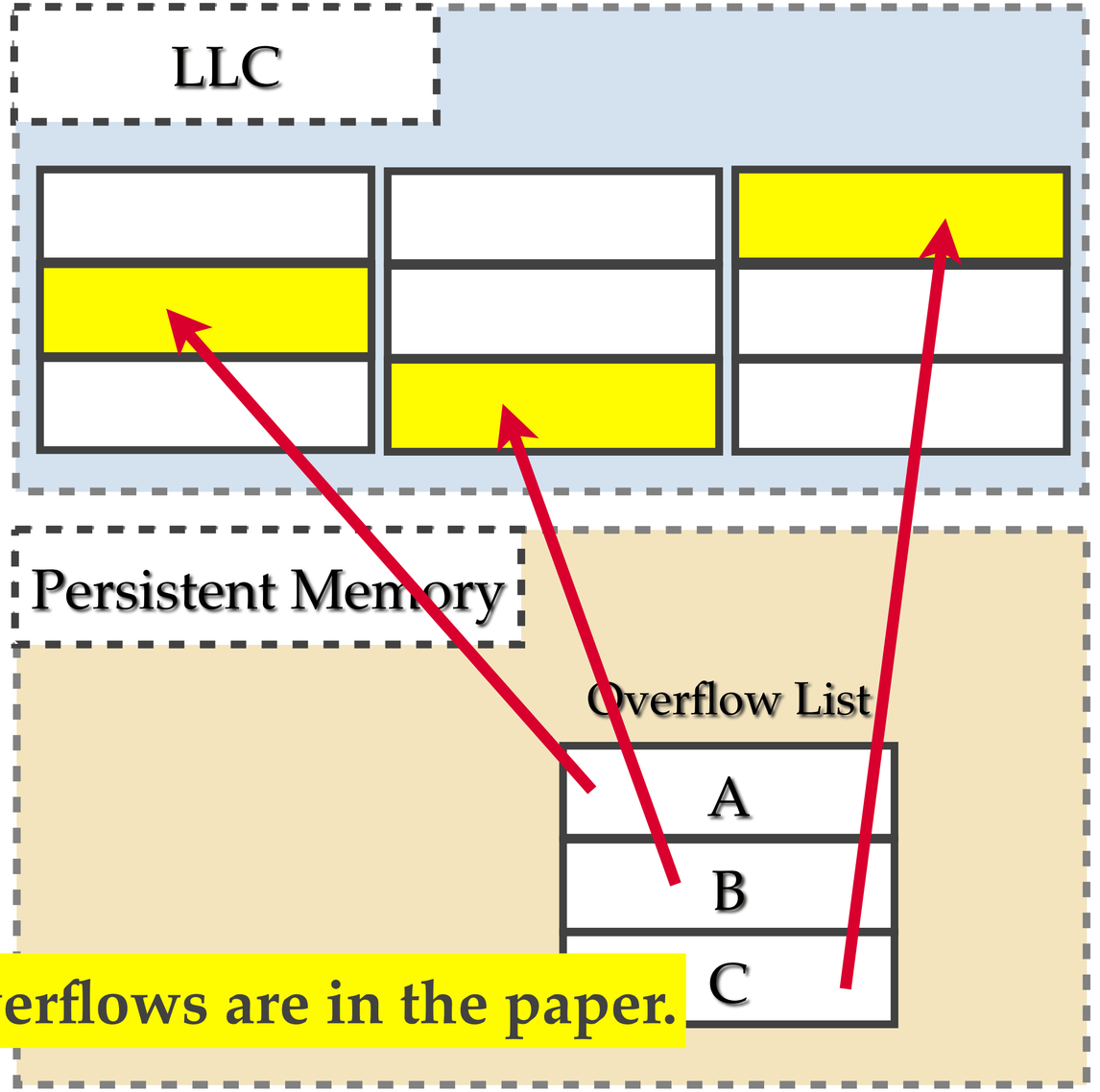


Further details on supporting overflows are in the paper.

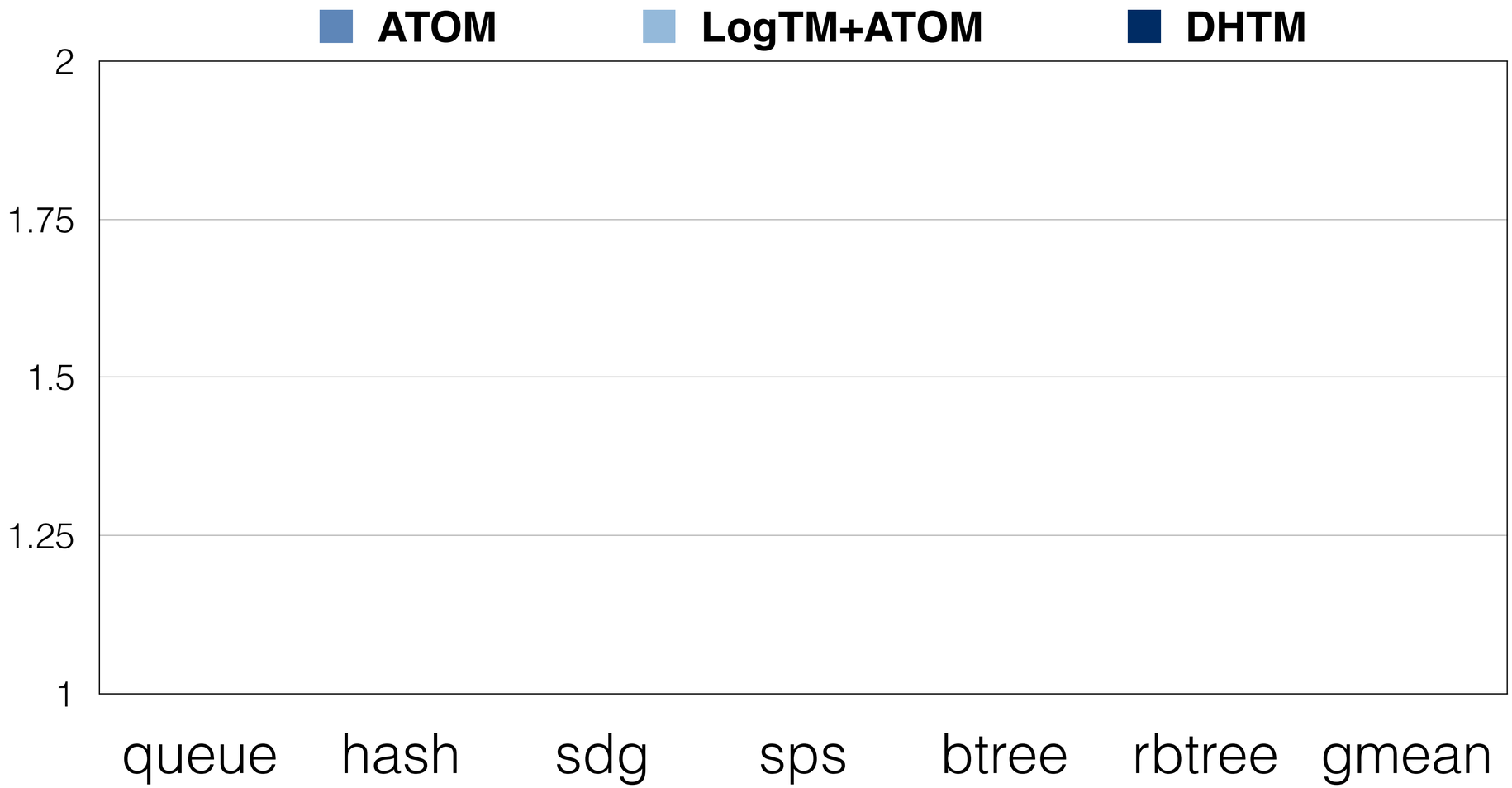
Evaluation

	Atomic Visibility	Atomic Durability
ATOM	Locks	Hardware Undo Log
LogTM+ATOM	HTM (LogTM)	Hardware Undo Log
DHTM	HTM	Hardware Redo Log (Log Buffer)

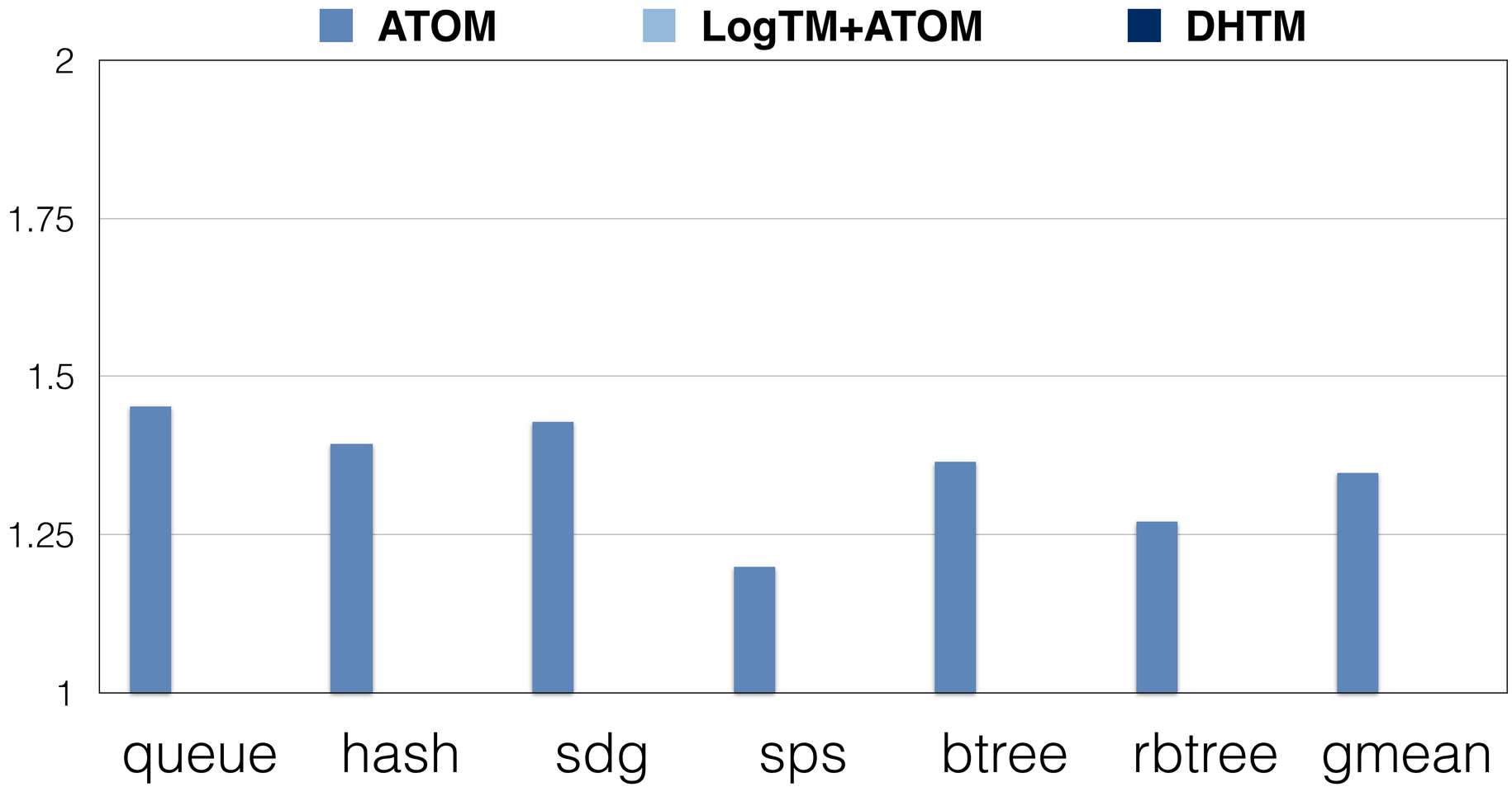
- **System Configuration**
  - We evaluate an 8-core machine with a 2-level cache hierarchy
  - HTM's implement (first) writer wins conflict resolution policy

Evaluation

Evaluation


ATOM
LogTM+ATOM
DHTM
2
1.75
1.5
1.25
1
queue
hash
sdg
sps
btree
rbtree
gmean

Evaluation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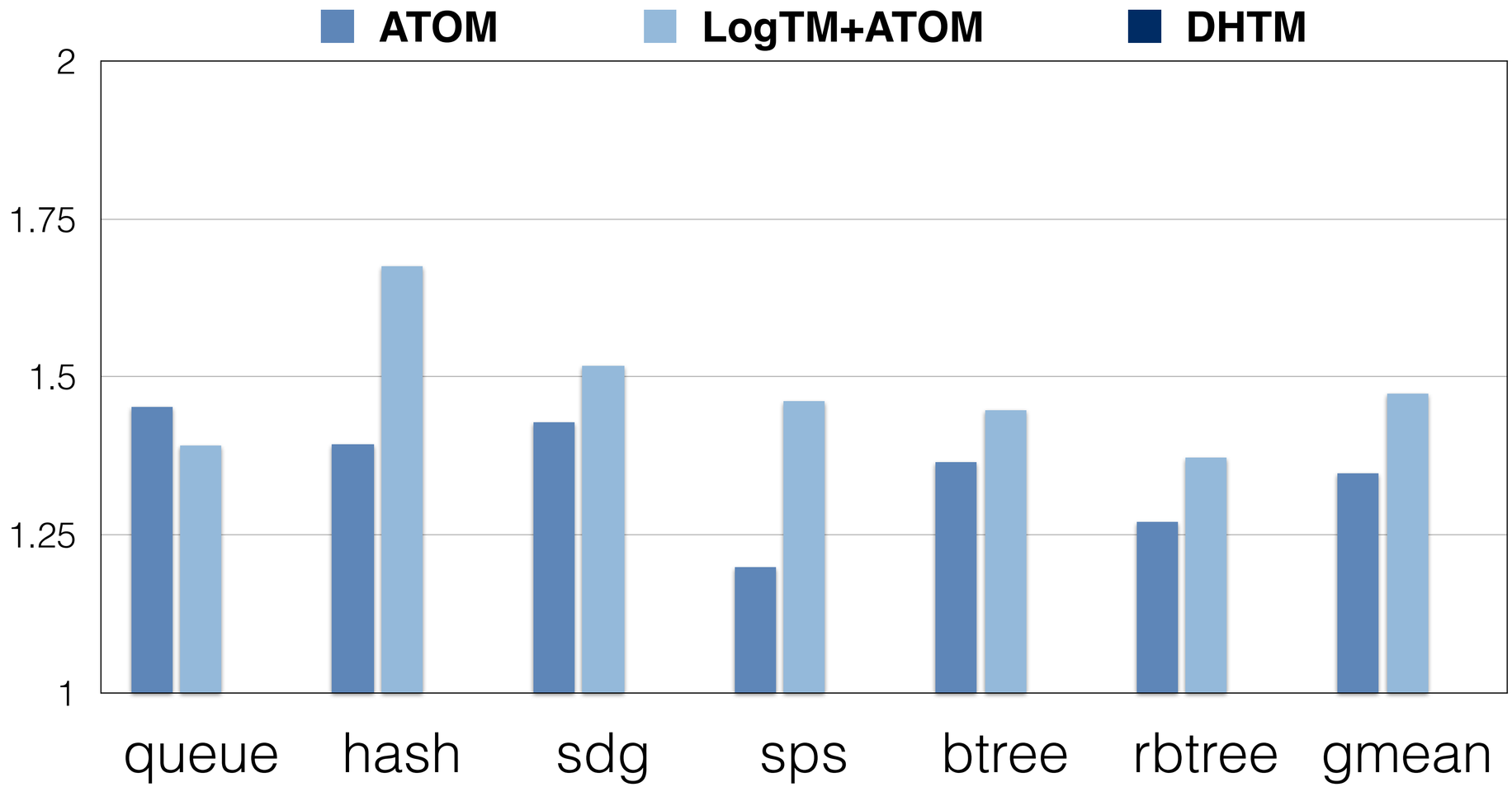
ATOM
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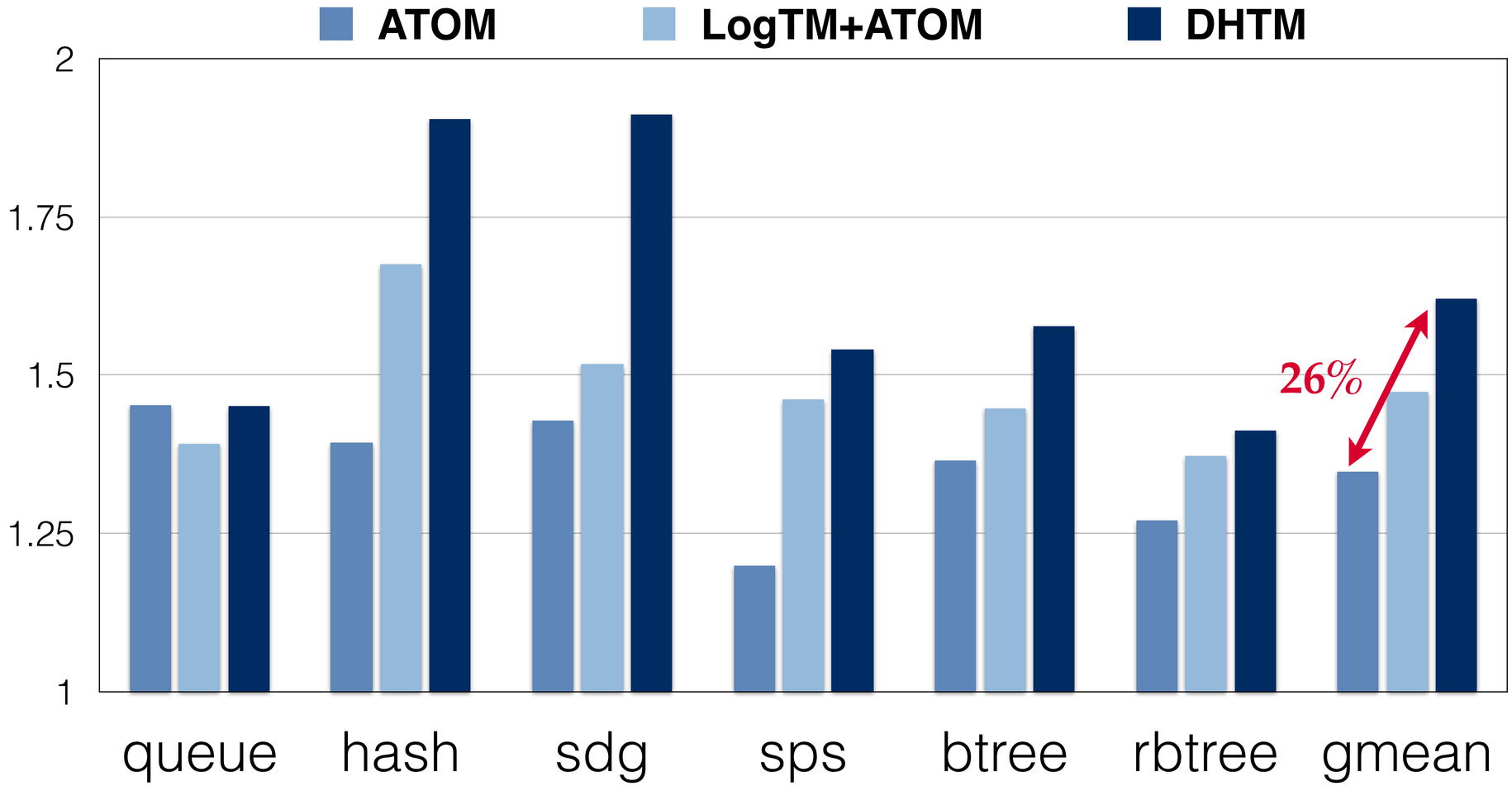
ATOM
LogTM+ATOM
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1.75
1.5
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1
26%
queue
hash
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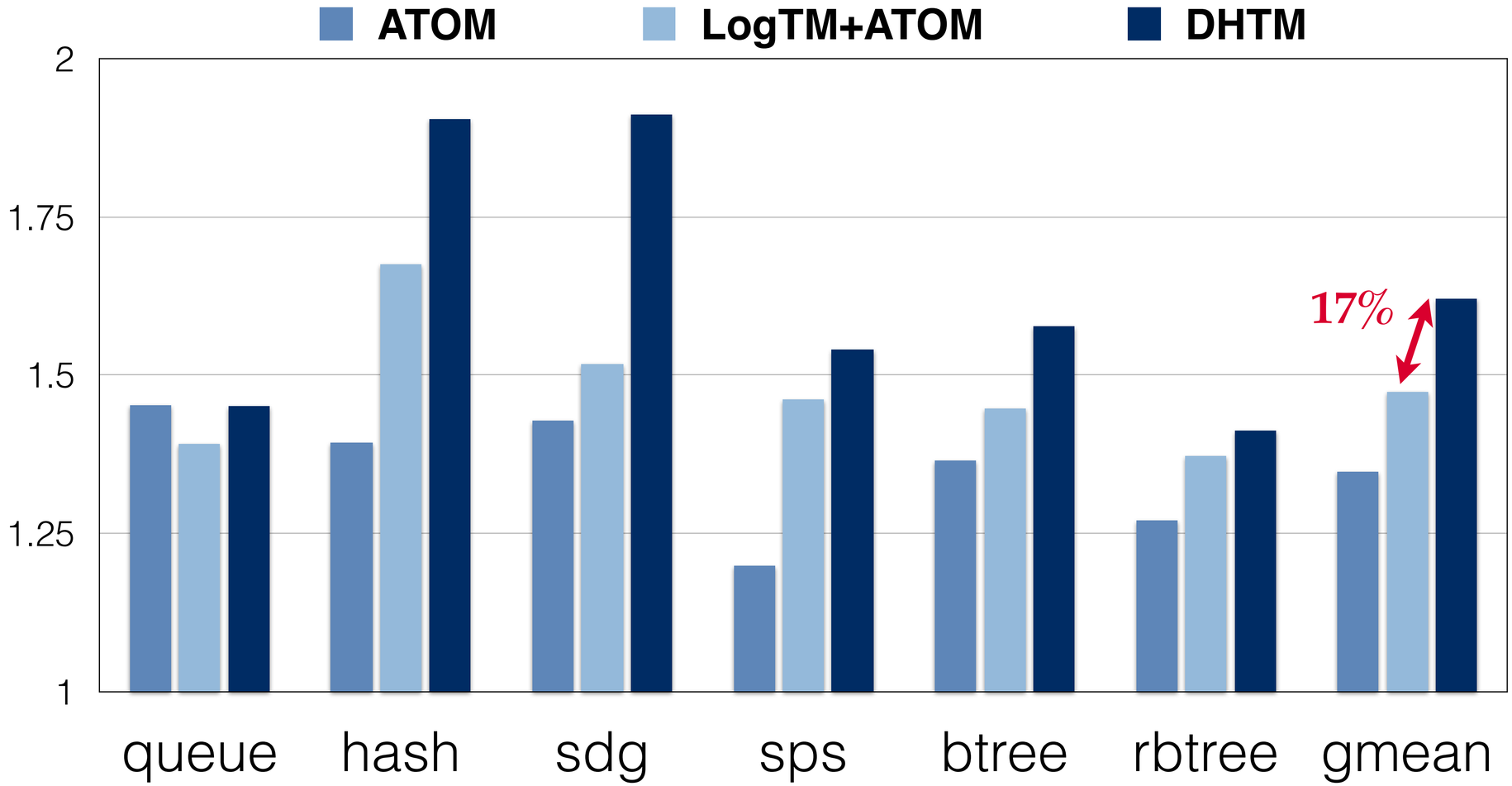
ATOM
LogTM+ATOM
DHTM
2
1.75
1.5
1.25
1
17%
queue
hash
sdg
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Conclusion

- Persistent memory systems require crash consistency
- ACID Transactions: widely understood crash consistency mechanism
- DHTM: ACID transactions in hardware
  - Atomic Visibility: commercial HTM
  - Atomic Durability: bandwidth optimized hardware redo log
  - Leverage hardware logging to extend transaction size unto LLC

DHTM: Durable Hardware Transactional Memory

Arpit Joshi, *Vijay Nagarajan, Marcelo Cintra, Stratis Viglas*

ISCA 2018

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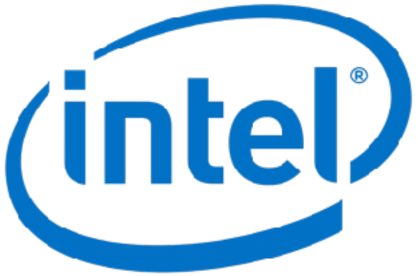

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