Quiz 4

1. Consider a workload that finds about 90% of its data in Level 1 cache, and 95% of its data in Level 2 cache. Compute the average time to load an item from memory as seen by the processor, given that the L1 cache requires 1 cycle to load, the L2 requires 10 cycles to load, and the main memory requires 65 cycles to load.

2. Reconsider Problem 1. A brilliant engineer working with you comes up with the idea of adding an L3 cache. Using simulation, you discover that the workload in problem 1 now finds its data in the L3 98% of the time. What is the average time to load an item from memory as seen by the processor. If the addition of the L3 will increase the cost of the processor by 50%, do you believe that this is worth doing?

3. Assume a memory array chip of "256M x 1" bits as a basic component. How many chips do you need to configure a 4GB memory? Assume one parity bit is added to every 8 bits of storage.

4. Repeat the above for an array of memory chips of "256M x 4" bits as the basic component. What is the overhead that is added for reliability?

5. Consider the following code:

```
double a[2 << 20];
double b[2 << 20];
double c[2 << 20];
for(i = 0; i < n; i++) {
        a[i] = b[i] * c[i];
}
```

   Assume that the cache line is 64 bytes. The processor runs at 2GHz. Calculate the necessary memory bandwidth that the processor needs to enable computation at 2GF/sec.

6. In a 32-bit machine we subdivide the virtual address into 4 segments as follows:

10-bit	8-bit	6-bit	8 bit

   We use a 3-level page table, such that the first 10-bit are for the first level and so on.
   - What is the page size in such a system?
   - What is the size of a page table for a process that has 256K of memory starting at address 0?

- What is the size of a page table for a process that has a code segment of 48K starting at address 0x1000000, a data segment of 600K starting at address 0x80000000 and a stack segment of 64K starting at address 0xf0000000 and growing upward (like in the PA-RISC of HP)