Quiz 3 Solutions

1. The following instructions can be issued concurrently:
    a. add R1, R2, R0 ld R3, (SP)
    b. add R1, #4
    c. ld R4 (R1)
    d. add R6, R3, R4

The dependence among the instructions is such that only the first and second can be issued concurrently. The third instruction needs the outcome of instruction 1, and also instructions 3, 4 and 5 are dependent in a sequential manner. This sort of sequential dependence is very common in application codes, and it is the antithesis of instruction-level parallelism.

2. In a pipeline consisting of 10 stages, there could be 10 instructions at various stages within the pipeline. Note, however, that this is a case of a pipeline with no bubbles. This corresponds to a processor that is running at its maximum potential. This is not very common.

3. The jump instruction will require getting an instruction that may not be in sequential order with the flow. This could precipitate a cache miss in the instruction cache. This can lead to a bubble in the pipeline. If the jump instruction is conditional, then a big bubble may ensue because the

4. Analyzing the flow, we can see that register R3 is used as a temporary holder for variables that are on the stack. There is no true dependence on the value of R3 that extends beyond the next instruction in each case. By using register renaming, the two instructions can be executed simultaneously.