First Trimester Examination

Name: _____

Student Id: _____

This is a closed book examination. You are not allowed to have your phone next to you. Attempt all questions.

Question 1 (5 points)

Consider the following code:

```
int a[0x10000000];              // an array of 256M entries

for(int i = 0; i < 0x10000000; i++) {

        // random() below returns a random 32-bit unsigned integer
        unsigned offset = random() & 0xffffffff;
        a[offset] = i;
}
```

Assume a pipelined processor unit with 4 ALU's, a quad-ported register file and a dual-issue instruction scheduler. Brad, who works for Shoddy Processor Systems (SPS), claims that this code can achieve an instruction per cycle (IPC) of about 1. Do you believe Brad? Why or why not?

Question 2 (5 points)

A processor's execution unit consists of 5 functional subsystems S1 through S5 with the following timing characteristics:

S1: 100 pico-seconds
S2: 150 pico-seconds
S3: 150 pico-seconds.
S4: 200 pico-seconds.
S5: 200 pico-seconds.

You also have access to latches, where a latch introduces 20 pico-seconds of delay.

a. What is the highest frequency an in-order, single issue processor can run at with the above design?
b. If we pipeline this execution unit by adding a latch after every subsystem, what is the highest frequency at which the processor can run?
c. You are given an alternative pipeline structure in which S1-S2-S3 are considered one stage and S4-S5 are considered another stage, with an intervening latch between the two stages. What is the highest frequency that you can run the pipeline at?
d. Between the design in (b) and (c), which one would you pick? Why?

Question 3 (5 points)

You are designing a video server for a big video streaming company. The server available to you has a main memory of 16GB, and memory bandwidth of 16GB/sec. The videos are stored in a secondary storage system connected to the server through four PCI channels, each capable of 4GB/second data transfer. The processor responds to clients that request streaming, runs the network protocol. It has been observed that the CPU utilization is 15%. The network subsystem consists of 6 Ethernet channels each supporting 10Gb/sec. A video stream requires 6Gb/sec to be streamed. The data flow is such that the processor loads the video from the secondary storage into main memory, and then the data are streamed from main memory to the network and eventually to the clients.

a. What is the maximum number of streams that can be pulled concurrently from the system?

b. You are approached by your boss to decide which component can be enhanced to improve performance. Which one would you pick? What would be the maximum number of streams in this case? (P.S. You are allowed to pick only one component to improve).

Question 4 (10 points)

The computation Y = a * X + Y has long been used as a benchmark for processor performance (known as SAXPY). The typical assembly code for this function is:

```
start:  ld      f1, (r1)        # the machine has two register sets
        mul     f4, f2, f0      # a * X[i], f4 holds the results, a is in f0, and f2 holds X[i]
        ld      f6, (r2)        # Y[i],
        add     f6, f4, f6      # a*X[i] + Y[i]
        st      f6, (r2)        # Updating Y[i]
        add     r1, r1, 8       # increment X[i]'s index
        add     r2, r2, 8       # increment Y[i]'s index
        add     r3, -1          # the loop index
        bnz     r3, start
```

Assume a pipeline containing a single-ported integer register file and a single-ported floating point register file. Assume an integer adder that finishes in one cycle, and a floating point multiplier that is pipelined over 7 stages, and a floating point adder that is pipelined over 4 stages. The instruction fetch and decode issue one instruction per cycle.

Answer the following questions:

a) Show how the code will execute on the pipeline. You may use out of order execution, register renaming, and branch prediction. Compute the IPC.

b) Unroll the loop with a depth of two. Add 3 more floating point adders and 3 more floating point multiplier. Make the register files dual ported and make the processor dual issue.