Sol 06

Problem 1

Jared and Joshua are designers of cache memory subsystem of a new chip at Sloppy Computing Systems (SCS). It was discovered late in the design that the power budget of the chip cannot be kept within the limits for cooling. An edict came from SCS's chief architect that each team must explore ways to reduce power consumption to help mitigate the crisis.

Jared declared that he has the answer. He suggested changing the 4-way set associate L2 cache to a direct-mapped cache can reduce power consumption and keep the chip within the power envelope of the design targets. He admitted that there will be a loss in performance, but since each cache access requires four comparisons and a complex replacement algorithm to be implemented, that the reduction in power was a fair tradeoff between performance and feasibility.

Joshua was adamant that Jared's idea is really bad. However, being overly shy and awkward, he was unable to articulate the reason. He dropped you a note to go explain his objection to the chief engineer and went on vacation. Unfortunately, he forgot to write down what his idea was. Your task is to figure out whether Joshua was correct and why, or to go tell the chief engineer to follow Jared's advice.

Joshua was arguing that Jared's solution does not save power at all. In fact, it may make matters worse. Each cache miss in the direct mapped cache will require moving data from and to memory, and the energy spent doing this will outweigh the relatively small cost of performing comparisons of addresses in the set associative cache. A more prudent approach, when power is at the limit, is to stagger the comparisons. Meaning, compare the first address in the set, and then compare the second only if the first is not found, and so on.

Problem 2

What is the size of an 8-entry TLB if the system has a 64-bit address space, a 44-bit physical address space, and a 4KB page?

We need not store the offset of the page either in the virtual address or the physical address. So every entry in the TLB will consist of a pair <vaddr, paddr>, with the sizes of (64-12) and (44-12), respectively. The TLB array thus is 8 x 84 bits (or 84 bytes).

Problem 3

Consider the stream benchmark. If we have a 4-way set associative cache, compare the performance of the following replacement algorithms:

- LRU
- FIFO
- Random

Explain your answers.

The stream benchmark tests the memory bandwidth of the chip. It does not involve any reuse of the data in the cache. Therefore, the replacement algorithm will not evict any data that will be soon needed again. So, all these replacement policies will perform more or less the same.

Problem 4

While running the daily regression tests, one application crashed with an "illegal instruction" exception. You have been called upon to find out what happened. An initial investigation identified the compiler as a possible cause for the problem. You read the report and it just did not make any sense to you. The code hasn't been modified since the night before, and when you tried to rerun the application, it succeeded. Explain what is happening.

A plausible explanation for what happened was that the memory was corrupted with a multi-bit transient error that went undetected by the parity or whatever protection system is used to detect memory error. Thus the instructions in question were likely corrupted by a silent error, causing the very unusual exception.