Quiz 3

1. The following instructions are presented to a fetch/decode/Instruction issue unit.

```
add     R1, R2, R0
ld      R3, (SP)
add     R1, #4
ld      R4, (R1)
add     R6, R3, R4
```

   Identify which of these instructions can be issued concurrently. Assume a dual-ported register file.

2. A pipeline consists of 10 stages. What is the maximum number of instructions that can be running concurrently?

3. Six arithmetic instructions are followed by a jump instruction. Do you foresee any effect of the jump instruction on the pipeline performance?

4. Consider the following instructions

```
ld      R3, (SP)
add     R0, R3, R4
sto     R0, (SP)
ld      R3, (SP + 4)
add     R1, R3, R4
sto     R1, (SP + 4)
```

   Is it possible to issue instructions 1 and 4 simultaneously? If so, show how. If not, argue why.