Class 3 Report

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1. Introduction

Introduction. The purpose of Class Report 3 was to familiarize ourselves with Pong Chu's Microblaze MCS package and the various files inside of his project. The hardware side in Verilog was quite simple, it involved us following Chu's instructions and installing the correct files and constraints. We then installed the correct CPU package and the Verilog side was done. We then moved into the Vitis side, showing how software is ran on FPGAs. We dove into IO reads and writes and how most of the software code is quite simple.

2. Experimental Plan

W. hat I did for my part of the Class Report 3 is building the project on my own, and then understanding the various parts of both the Verilog code and C++. I followed Chu's instructions, and uploaded to the Nexys4 DDR board. From there, I was able to see the C++ code in action and run. It tested the switches and the LEDs. The author names and affiliations could be formatted in two ways:

3. Analysis Section

T. he following figures show the Verilog and Vitis code that was included in this project. After compiling the C++ code in Vitis, you can see that it works just like Chu intended.

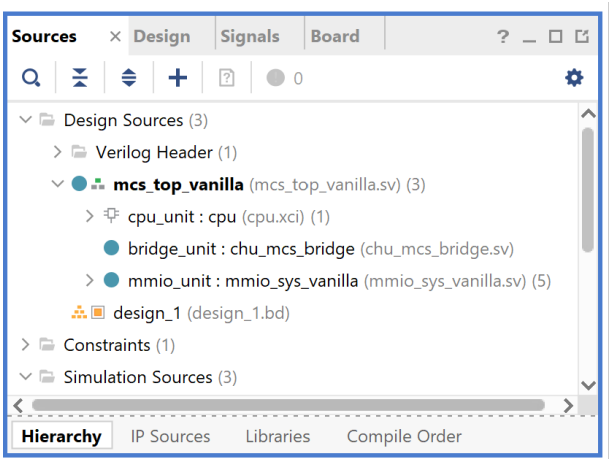

Figure 1: Sources

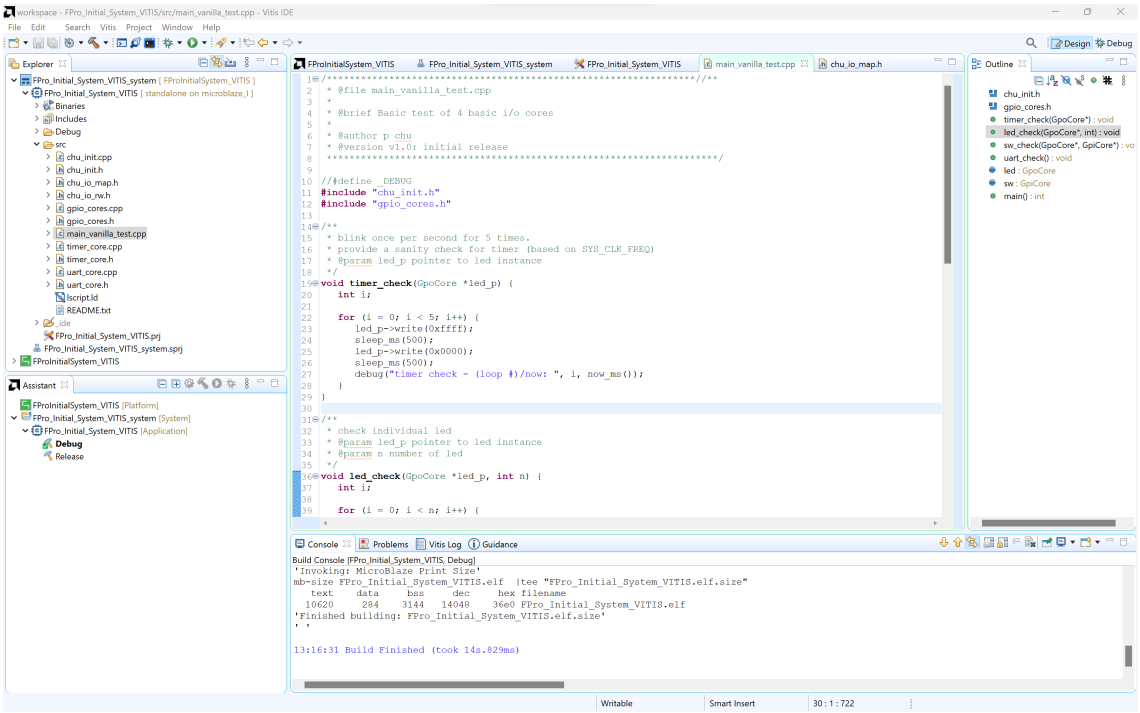

Figure 2: Vitis IDE

4. Conclusion

O. verall, this class report was mostly following Pong Chu's instructions. It was a tutorial to showcase how someone creates an FPGA and then codes the software to run on it. The future projects will build off of this base code, allowing us to take advantage of the predefined code, he has given us. Here is the GitHub link to my project: https://github.com/NoelSengel/Blinking-LED-Core.git