Periféricos

System I/O

Organización de Computadoras 2024

UNC Universidad Nacional de Córdoba

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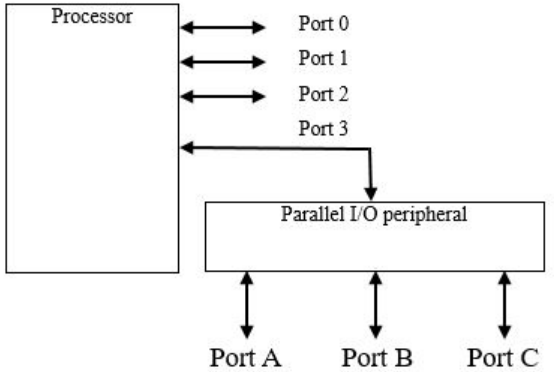
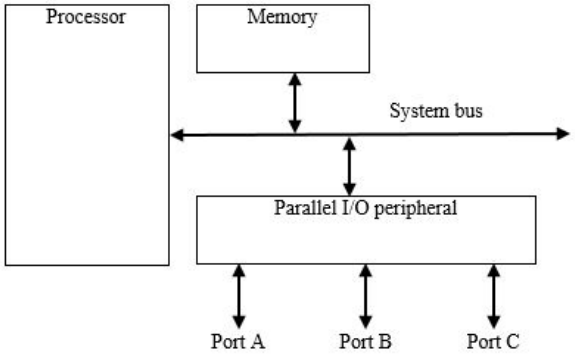
Microprocessor interfacing: I/O addressing

A microprocessor communicates with other devices using some of its pins

- **Port-based I/O (parallel I/O)**
  - Processor has one or more N-bit ports
  - Processor's software reads and writes a port just like a register

- **Bus-based I/O**
  - Processor has address, data and control ports that form a single bus
  - Communication protocol is built into the processor
  - A single instruction carries out the read or write protocol on the bus



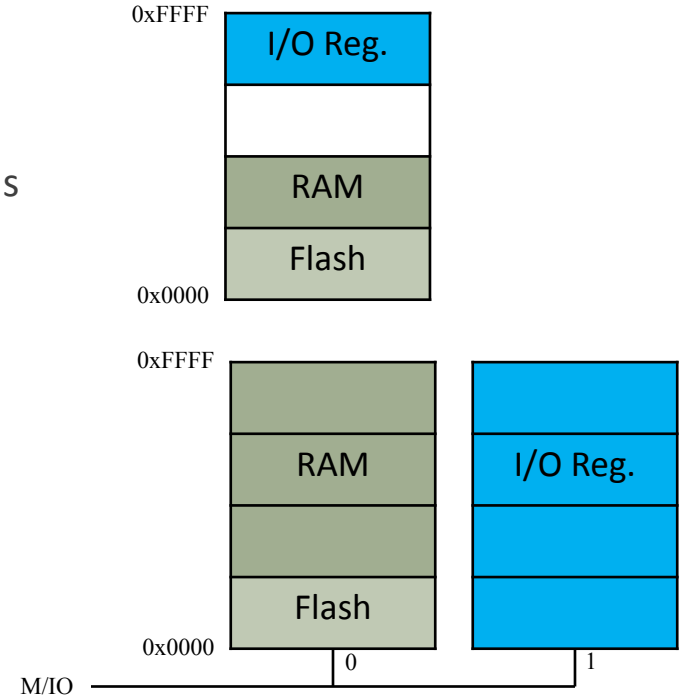


Types of bus-based I/O: **memory-mapped I/O** and **standard I/O**

Processor “talks” to both memory and peripherals using same bus

- **Memory-mapped I/O**
  - Peripheral registers occupy addresses in same address space as memory

- **Standard I/O (I/O-mapped I/O)**
  - Additional pin (*M/IO*) on bus indicates whether a memory or peripheral access



Memory-mapped I/O vs. Standard I/O

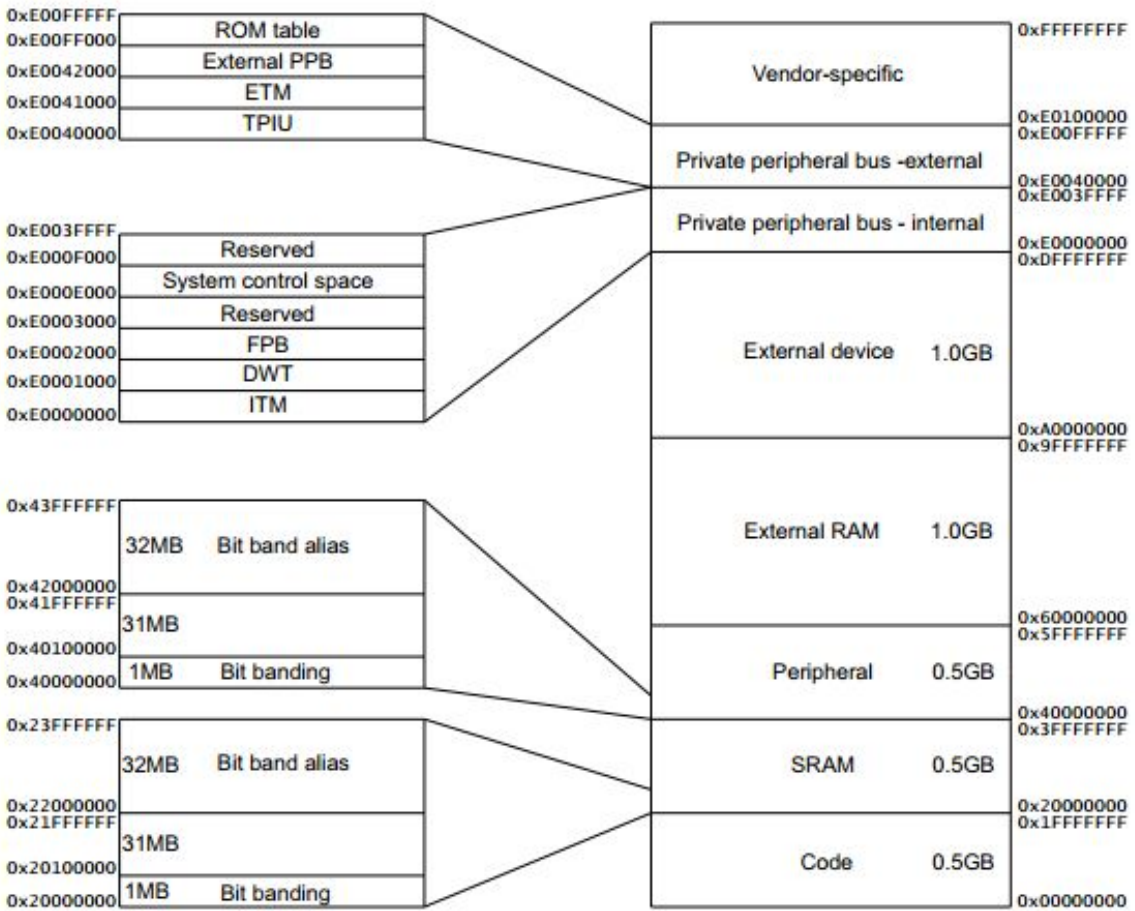
Memory-mapped I/O

- Requires no special instructions
  - Assembly instructions involving memory like LDUR and STUR work with peripherals as well
  - Standard I/O requires special instructions (e.g., IN, OUT) to move data between peripheral registers and memory

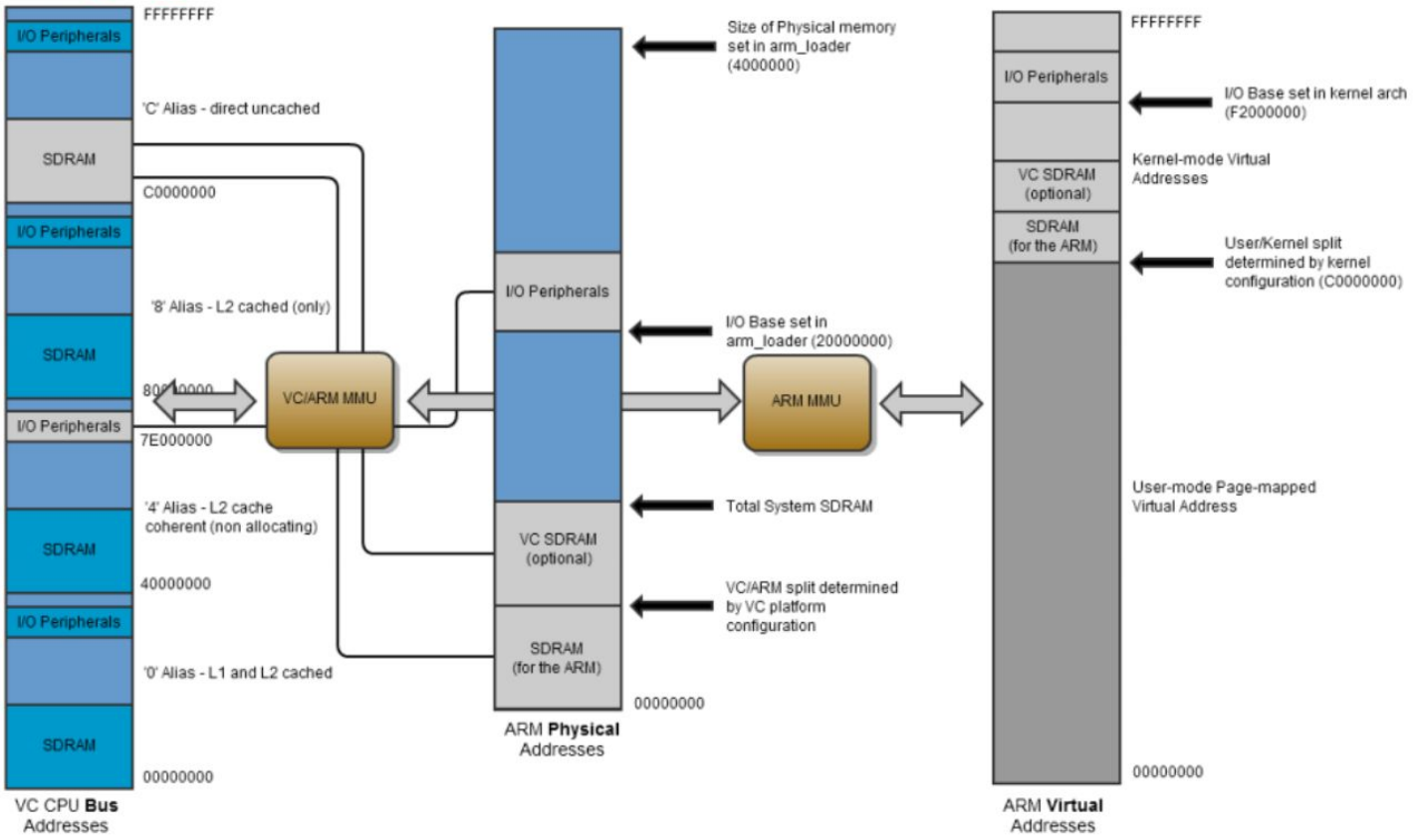
Standard I/O

- No loss of memory addresses to peripherals
- Simpler address decoding logic in peripherals
  - When number of peripherals much smaller than address space then high-order address bits can be ignored

Example:
ARM Cortex A9
Memory map

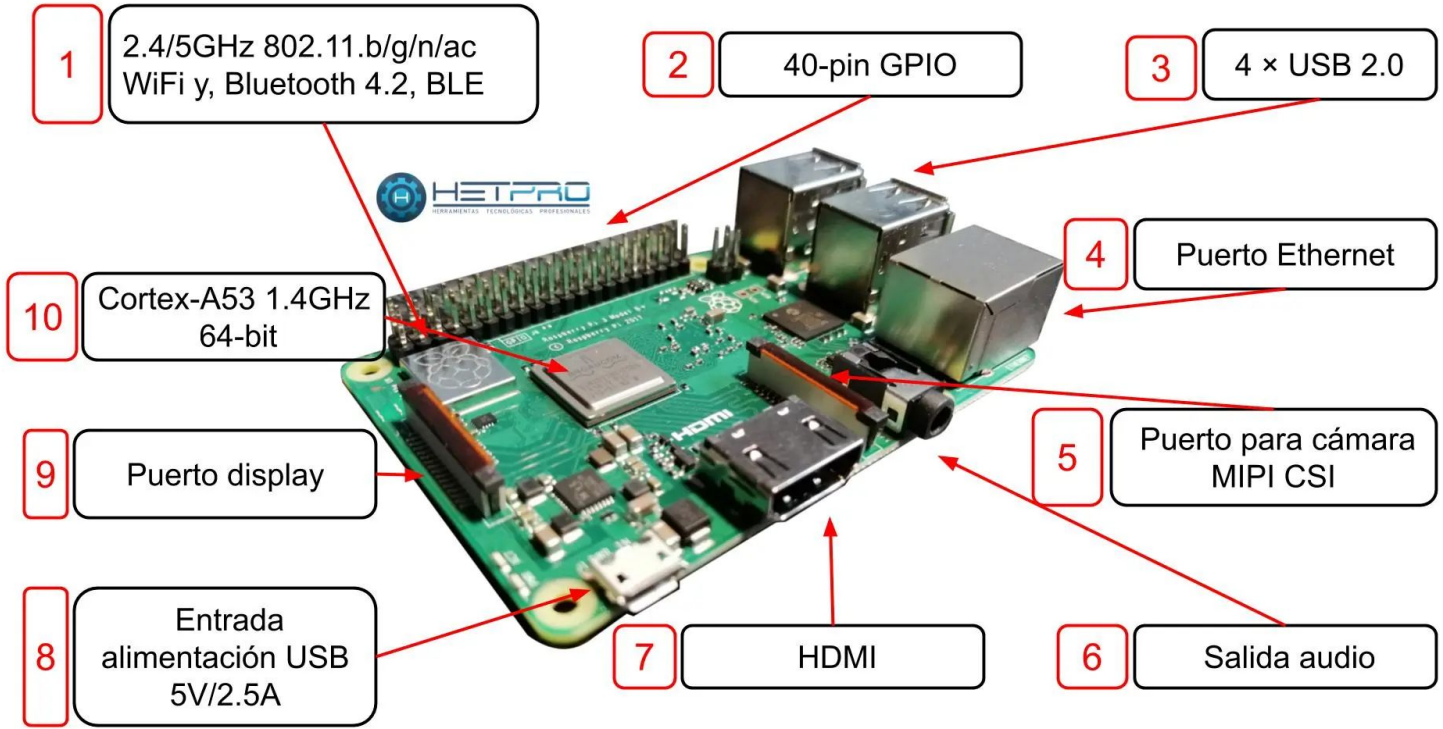


BCM2835 ARM Peripherals

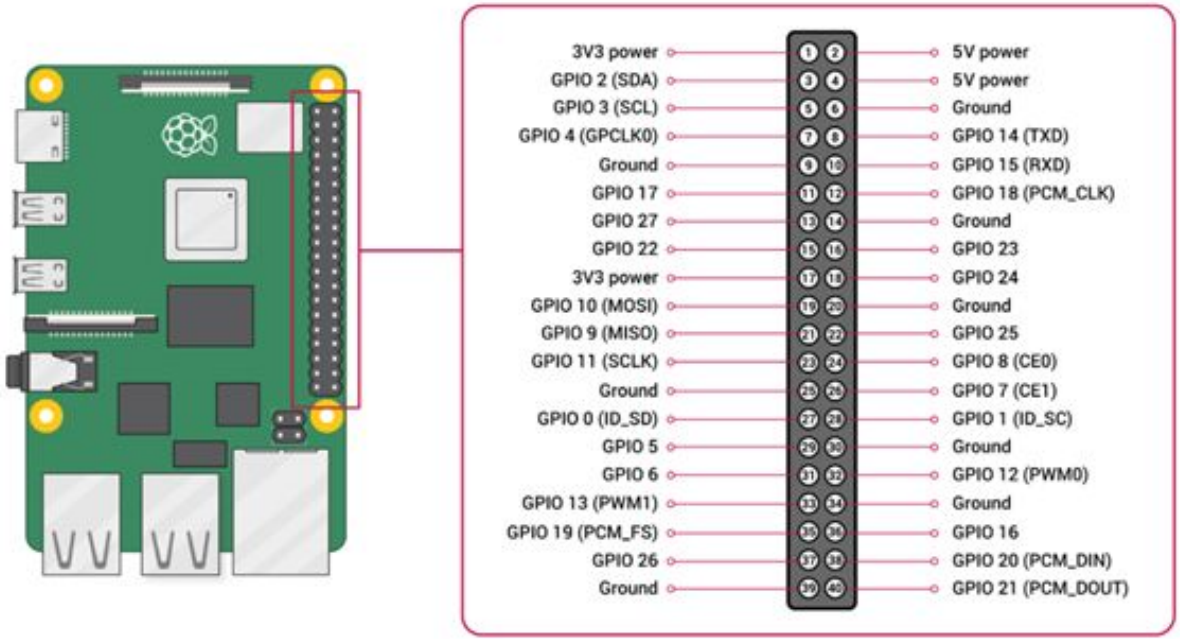


Trabajo de Laboratorio: VC FrameBuffer y GPIO en RPi3

Raspberry Pi 3 Model B

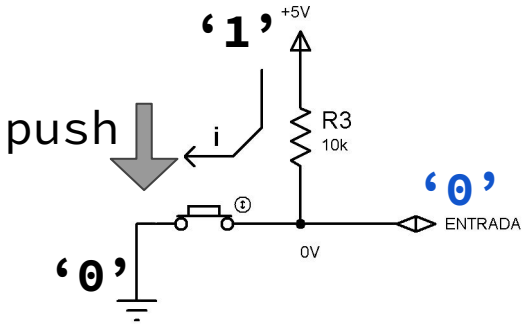


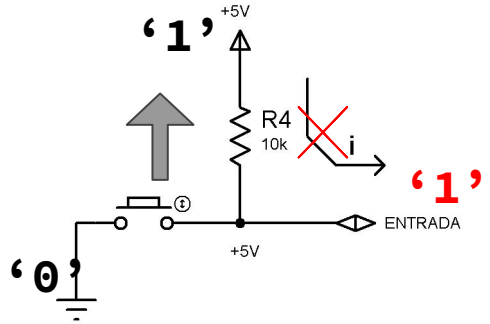
Raspberry Pi 3 B Pinout



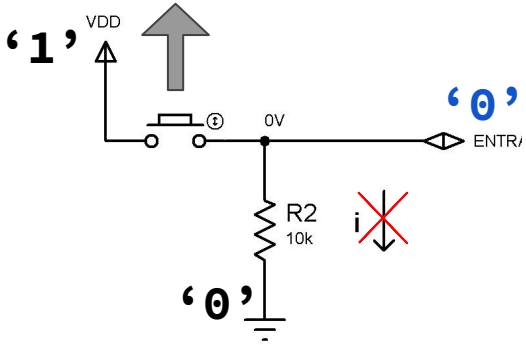
Switch Configuration

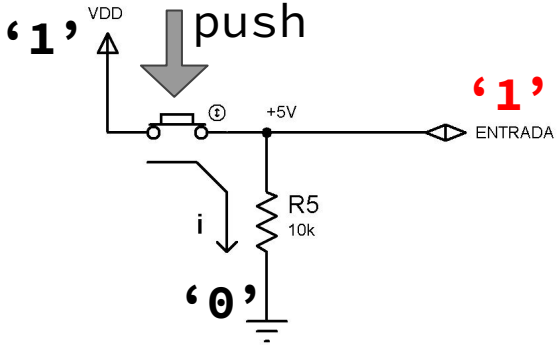
Pull-up

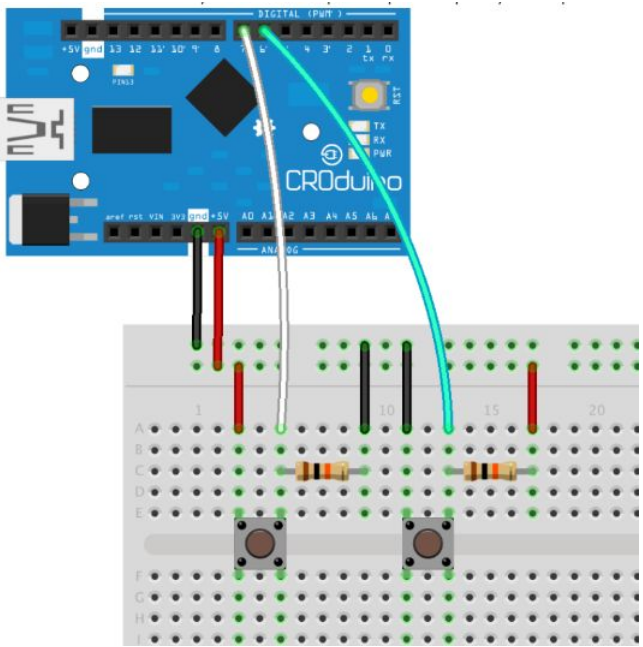




Pull-down







Registros para el manejo de GPIO

0x3F200000 →
\+ 0x04
\+ 0x1C
\+ 0x20
\+ 0x28
\+ 0x2C
\+ 0x34
\+ 0x38

Address	Field Name	Description	Size	Read/ Write
0x 7E20 0000	GPFSEL0	GPIO Function Select 0	32	R/W
0x 7E20 0000	GPFSEL0	GPIO Function Select 0	32	R/W
0x 7E20 0004	GPFSEL1	GPIO Function Select 1	32	R/W
0x 7E20 0008	GPFSEL2	GPIO Function Select 2	32	R/W
0x 7E20 000C	GPFSEL3	GPIO Function Select 3	32	R/W
0x 7E20 0010	GPFSEL4	GPIO Function Select 4	32	R/W
0x 7E20 0014	GPFSEL5	GPIO Function Select 5	32	R/W
0x 7E20 0018	-	Reserved	-	-
0x 7E20 001C	GPSET0	GPIO Pin Output Set 0	32	W
0x 7E20 0020	GPSET1	GPIO Pin Output Set 1	32	W
0x 7E20 0024	-	Reserved	-	-
0x 7E20 0028	GPCLR0	GPIO Pin Output Clear 0	32	W
0x 7E20 002C	GPCLR1	GPIO Pin Output Clear 1	32	W
0x 7E20 0030	-	Reserved	-	-
0x 7E20 0034	GPLEV0	GPIO Pin Level 0	32	R
0x 7E20 0038	GPLEV1	GPIO Pin Level 1	32	R
0x 7E20 003C	-	Reserved	-	-

Configuración de los GPIO - GPFSELO

Bit(s)	Field Name	Description	Type	Reset
31-30	---	Reserved	R	0
29-27	FSEL9	FSEL9 - Function Select 9 000 = GPIO Pin 9 is an input 001 = GPIO Pin 9 is an output 100 = GPIO Pin 9 takes alternate function 0 101 = GPIO Pin 9 takes alternate function 1 110 = GPIO Pin 9 takes alternate function 2 111 = GPIO Pin 9 takes alternate function 3 011 = GPIO Pin 9 takes alternate function 4 010 = GPIO Pin 9 takes alternate function 5	R/W	0
26-24	FSEL8	FSEL8 - Function Select 8	R/W	0
23-21	FSEL7	FSEL7 - Function Select 7	R/W	0
20-18	FSEL6	FSEL6 - Function Select 6	R/W	0
17-15	FSEL5	FSEL5 - Function Select 5	R/W	0
14-12	FSEL4	FSEL4 - Function Select 4	R/W	0
11-9	FSEL3	FSEL3 - Function Select 3	R/W	0
8-6	FSEL2	FSEL2 - Function Select 2	R/W	0
5-3	FSEL1	FSEL1 - Function Select 1	R/W	0
2-0	FSEL0	FSEL0 - Function Select 0	R/W	0

Table 6-2 – GPIO Alternate function select register 0

Configuración de los GPIO - GPFSEL1

Bit(s)	Field Name	Description	Type	Reset
31-30	---	Reserved	R	0
29-27	FSEL19	FSEL19 - Function Select 19 000 = GPIO Pin 19 is an input 001 = GPIO Pin 19 is an output 100 = GPIO Pin 19 takes alternate function 0 101 = GPIO Pin 19 takes alternate function 1 110 = GPIO Pin 19 takes alternate function 2 111 = GPIO Pin 19 takes alternate function 3 011 = GPIO Pin 19 takes alternate function 4 010 = GPIO Pin 19 takes alternate function 5	R/W	0
26-24	FSEL18	FSEL18 - Function Select 18	R/W	0
23-21	FSEL17	FSEL17 - Function Select 17	R/W	0
20-18	FSEL16	FSEL16 - Function Select 16	R/W	0
17-15	FSEL15	FSEL15 - Function Select 15	R/W	0
14-12	FSEL14	FSEL14 - Function Select 14	R/W	0
11-9	FSEL13	FSEL13 - Function Select 13	R/W	0
8-6	FSEL12	FSEL12 - Function Select 12	R/W	0
5-3	FSEL11	FSEL11 - Function Select 11	R/W	0
2-0	FSEL10	FSEL10 - Function Select 10	R/W	0

Table 6-3 – GPIO Alternate function select register 1

Registros de uso GPIO

Output Set Reg. - GPSETn

Bit(s)	Field Name	Description	Type	Reset
31-0	SETn (n=0..31)	0 = No effect 1 = Set GPIO pin *n*	R/W	0

Table 6-8 – GPIO Output Set Register 0

Output Clear Reg. - GPCLRn

Bit(s)	Field Name	Description	Type	Reset
31-0	CLRn (n=0..31)	0 = No effect 1 = Clear GPIO pin *n*	R/W	0

Table 6-10 – GPIO Output Clear Register 0

Input Level Reg. - GPLEVn

Bit(s)	Field Name	Description	Type	Reset
31-0	LEVn (n=0..31)	0 = GPIO pin *n* is low 0 = GPIO pin *n* is high	R/W	0

Table 6-12 – GPIO Level Register 0

1

Ejemplos:

- GPIO 2: 0000 0000 0000 0000 0000 0000 0000 0100 = 0x00000004
- GPIO 3: 0000 0000 0000 0000 0000 0000 0000 1000 = 0x00000008
- GPIO 2 y 3: 0000 0000 0000 0000 0000 0000 0000 1100 = 0x0000000C