Design Rules Verification Report

Filename : E:\Git\OMD\OMD_Hardware\PCB's\UWB_CAN_R3.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.076mm) (All),(All)	0
Clearance Constraint (Gap=0.15mm) (Disabled)(IsPad),(IsVia)	0
Short-Circuit Constraint (Allowed=No) (InPadClass('All Pads')),(All)	0
Un-Routed Net Constraint ((All))	0
Width Constraint (Min=0.124mm) (Max=0.254mm) (Preferred=0.254mm) (InNet('2V8'))	0
Width Constraint (Min=0.087mm) (Max=0.254mm) (Preferred=0.254mm) (InNet('Net3_1'))	0
Width Constraint (Min=0.124mm) (Max=0.254mm) (Preferred=0.254mm) (InNet('1V8'))	0
Width Constraint (Min=0.127mm) (Max=0.5mm) (Preferred=0.254mm) (All)	0
SMD Neck-Down Constraint (Percent=70%) (Disabled)(InNet('2V8'))	0
SMD Neck-Down Constraint (Percent=100%) (Disabled)(All)	0
SMD Neck-Down Constraint (Percent=70%) (Disabled)(InNet('1V8'))	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm	0
Hole Size Constraint (Min=0.025mm) (Max=5mm) (All)	0
Hole To Hole Clearance (Gap=0.203mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (Disabled)(All),(All)	0
Silk To Solder Mask (Clearance=0.001mm) (Disabled)(IsPad),(All)	0
Silk to Silk (Clearance=0.254mm) (Disabled)(All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Matched Lengths(Tolerance=25.4mm) (Disabled)(All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Silk primitive without silk layer	0
Total	0