Homework 4

1. (a) 8 word per block = 32 byte / block = 2^5 byte/block

offset: 4-0

There are $\frac{256}{32}$ = 8 blocks, index: 7-5

Then, tag: 31-8

(b)

Address	Tag	Index	Offset	Hit/Miss	Replaced
0x00	0x000000	000	00000	M	
0x04	0x000000	000	00100	H	
0x10	0x000000	000	10000	H	
0x84	0x000000	100	00100	M	
0xE8	0x000000	111	01000	M	
0xA0	0x000000	101	00000	M	
0x400	0x000004	000	00000	M	0x00 - 0x1F
0x1E	0x000000	000	11110	M	0x400 - 0x41F
0x8C	0x000000	100	01100	H	
0xC1C	0x00000C	000	11100	M	0x00 - 0x1F
0xB4	0x000000	101	10100	H	
0x884	0x000008	100	00100	M	0x80 - 0x9F

(d) ⟨0, 0xC, Mem[0xC00] - Mem[0xC1F]⟩

⟨4, 0x8, Mem[0x880] - Mem[0x89F]⟩

⟨5, 0x0, Mem[0xA0] - Mem[0xBF]⟩

⟨7, 0x0, Mem[0xE0] - Mem[0xFF]⟩

(c) Hit Ratio is $\frac{4}{12}$ = 33.3%

2. (a) Address is word address, block is 2-word block. offset: 0-0

3 way set × 2 word block = 6 word/set

There are $\frac{48}{6} = 8 = 2^3$ sets.

index: 3-1, tag: 31-4

(b) Total size 24 words. tag: 31-3 index: 2-1 offset: 0-0

Word Address	Tag	Index	Offset	Hit/Miss
0x03	00000	01	1	M
0xb4	10110	10	0	M
0x2b	00101	01	1	M
0x02	00000	01	0	H
0xbe	10111	11	0	M
0x58	01011	00	0	M
0xbf	10111	11	1	H
0x0e	00001	11	0	M
0x1f	00011	11	1	M
0xb5	10110	10	1	H
0xbf	10111	11	1	H
0xba	10111	01	0	M
0x2e	00101	11	0	M
0xce	11001	11	0	M

Final Cache:

	Way0 tag data		Way1 tag data		Way2 tag data	
Set 0	11	M[58-59]	NA		NA	
Set 1	0	M[02-03]	5	M[2a-2b]	23	M[ba-bb]
Set 2	22	M[b4-b5]	NA		NA	
Set 3	23	M[be-bf]	5	M[2e-2f]	25	M[ce-cf]

(c)

Word Address	Tag	Index	Hit/Miss
0x03	0x03	No Index	M
0xb4	0xb4		M
0x2b	0x2b		M
0x02	0x02		M
0xbe	0xbe		M
0x58	0x58		M
0xbf	0xbf		M
0x0e	0x0e		M
0x1f	0x1f		M
0xb5	0xb5		M
0xbf	0xbf		H
0xba	0xba		M
0x2e	0x2e		M
0xce	0xce		M

Final Cache:

	tag	data
way0	0x58	M[58]
way1	0x0e	M[0e]
way2	0x1f	M[1f]
way3	0xb5	M[b5]
way4	0xbf	M[bf]
way5	0xba	M[ba]
way6	0x2e	M[2e]
way7	0xce	M[ce]

3. (a) $2GHz \Rightarrow$ 1 cycle 0.5 ns.

Access main memory needs $\frac{100nS}{0.5ns/cycle} = 200$ cycles.

$CPI = 1.5 + 7\% \times 200 = 15.5$

(b) $CPI = 1.5 + 7\% \times 12 + 3.5\% \times 200 = 9.34$

(c) $CPI = 1.5 + 7\% \times \overset{28}{12} + 1.5\% \times 200 = 6.46$

(d) $CPI = 1.5 + 7\% \times (12 + 3.5\% \times 200) = 2.83$

4. (a) $2^p \geq p + 128 + 1 \Rightarrow p = 8$

Hence we need 9 bits to protect.

(b)

D_7	D_6	D_5	D_4	P_4	D_3	D_2	D_1	P_3	D_0	P_2	P_1
0	0	1	1	0	1	1	1	0	1	0	1

$G_1 = P_1 \oplus D_0 \oplus D_1 \oplus D_3 \oplus D_4 \oplus D_6 = 1$

$G_2 = P_2 \oplus D_0 \oplus D_2 \oplus D_3 \oplus D_5 \oplus D_6 = 0$

$G_3 = P_3 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_7 = 1$

$G_4 = P_4 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 = 0$

$\overline{G_4 G_3 G_2 G_1} = 0101 = 5$, Hence H5 that is D_1 is incorrect.

The correct one is 0x365.

5. (a) Next Page

5. (a)

Address	Virtual Page Num	TLB H/M, PT H/M, PF
4669	1	TLB miss, PT hit, PF
2227	0	TLB miss, PT hit,
13916	3	TLB hit, PT hit
34587	8	TLB miss, PT hit, PF
48870	b	TLB miss, PT hit
12608	3	TLB hit, PT hit
49225	c	TLB miss, PT miss, PF

Final TLB:

Valid	Tag	Physical Page Num	Time Since Last Access
1	0xC	15	0
1	0x8	14	3
1	0x3	6	1
1	0xb	12	2

Final Page Table:

Valid	Physical Page or in Disk
1	5
1	13
0	Disk
1	6
1	9
1	11
0	Disk
1	4
1	14
0	Disk
1	3
1	12
1	15

(b)

Address	Virtual Page	Index	Tag	TLB H/M, PT H/M, PF
4669	1	1	0	TLB Miss, PT hit, PF
2227	0	0	0	TLB miss, PT hit
13916	3	1	1	TLB miss, PT hit
34587	8	0	4	TLB miss, PT hit, PF
48870	b	1	5	TLB miss, PT hit
12608	3	1	1	TLB hit, PT hit
49225	c	0	6	TLB miss, PT miss, PF

Final TLB:	Index	Valid	Tag	Physical Page	Time Since Last Access
	0	1	0x6	15	0
	0	1	0x4	14	3
	1	1	0x1	6	1
	1	1	0x5	12	2