Computer Organization HW1

1. For the following C statement, write the corresponding RISC-V assembly code. Assume that the C variables f, g, and h, have already been placed in registers x5, x6, and x7 respectively. Use a minimal number of RISC-V assembly instructions.

   f = g + (h − 5);

2. Translate the following C code to RISC-V. Assume that the variables f, g, h, i, and j are assigned to registers x5, x6, x7, x28, and x29, respectively. Assume that the base address of the arrays A and B are in registers x10 and x11, respectively. Assume that the elements of the arrays A and B are 4-byte words:

   B[8] = A[i] + A[j];

3. The table below shows 32 bit values of an array stored in memory

Address	Data
24	2
28	4
32	3
36	6
40	1

   1) For the memory locations in the table above, write C code to sort the data from lowest to highest, placing the lowest value in the smallest memory location shown in the figure. Assume that the data shown represents the C variable called Array, which is an array of type int, and that the first number in the array shown is the first element in the array. Assume that this particular machine is a byte addressable machine and a word consists of four bytes.
   2) For the memory locations in the table above, write RISC-V code to sort the data from lowest to highest, placing the lowest value in the smallest memory location. Use a minimum number of RISC-V instructions. Assume the base address of Array is stored in register x22.

4. Provide the instruction type and assembly language instruction for the following binary value:

   $0000\ 0000\ 0001\ 0000\ 1000\ 0000\ 1011\ 0011_{two}$

5. Provide the instruction type, assembly language instruction, and binary representation of instruction described by the following RISC-V fields:
   opcode=0x3, funct3=0x2, rs1=27, rd=3, imm=0x4