

## Homework 3

1. a) pipeline: 350 ps. The longest stage is ID, it takes 350 ps.  
non-pipeline: 1250 ps. A clock cycle include 5 stages.
- b) pipeline: 1250 ps. lw should take all 5 stages, so no matter pipeline or not, it will both take 1250 ps.  
non-pipeline: 1250 ps.
- c) We cut the longest stage ID, then the longest will be MEM.  
It takes 300 ps, so the new clock cycle should be 300 ps.
- d) Load and store use data memory.  $20\% + 15\% = 35\%$
- e) ~~Branch~~ ALU/Logic and Load need write back.  $45\% + 20\% = 65\%$
- f) clock cycle times:

- single-cycle: 1250 ps

- multi-cycle: 350 ps

- pipeline: 350 ps

execution times:

- single-cycle: 1250 ps per instruction

- multi-cycle:  $45\% \times \overset{1400 \text{ ps}}{1250 \text{ ps}} + 20\% \times \overset{1050 \text{ ps}}{1250 \text{ ps}} + 20\% \times \overset{1750 \text{ ps}}{1250 \text{ ps}} + 15\% \times \overset{1400 \text{ ps}}{1250 \text{ ps}}$   
 $= \overset{1400}{1400} \text{ ps per instruction}$

- pipeline: 350 ps per instruction

2. a) Before, need  $(n + 4n) \cdot 250 \text{ ps} = 1250n \text{ ps}$

After, need  $(n + 0.05n) \cdot 300 \text{ ps} = 315n \text{ ps}$

$$\text{speedup} = \frac{1250n}{315n} = 3.97$$

b)  $\frac{(1+x) \cdot 250}{(1+0.05) \cdot 300} = 1 \Rightarrow x = 0.26$

Only

b)  $\frac{(1+4) \cdot 250}{(1+x) \cdot 300} = 1 \Rightarrow x = 3.17$

3.17n NOPs can remain.

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3. a)

CC1 CC2 CC3 CC4 CC5 CC6 CC7 CC8 CC9 CC10 CC11 CC12

sw x29, 12(x16)



lw x29, 8(x16)



sub x17, x15, x14



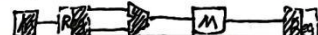
beqz x17, label



add x15, x11, x14



sub x15, x30, x14



b) No. If we put load and store at the end, there will be some problems about branch.

c) No. NOP is "addi zero, zero, 0", it still needs fetch instruction.

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4. a) 1 2 3 4 5 6 7 8 9 10

li x12, 0 IF ID EX MEM WB

jnl ENT IF ID EX MEM WB

bne x12, x13, TOP IF ID EX MEM WB

slli x5, x12, 2 IF ID EX MEM WB

add x6, x10, x5 IF ID EX MEM WB  
lw x7, 0(x6) IF ID EX MEM WB

lw x29, 4(x6) IF ID EX MEM WB

sub x30, x7, x29 IF ID EX MEM WB

add x31, x11, x5 IF ID EX MEM WB

sw x30, 0(x31) IF ID EX MEM WB

addi x12, x12, 2 IF ID EX MEM WB

~~bne x12, x13, TOP~~  
bne x12, x13, TOP IF ID EX MEM WB

slli x5, x12, 2 IF ID EX MEM WB

add x6, x10, x5 IF ID EX MEM WB  
lw x7, 0(x6) IF ID EX MEM WB

lw x29, 4(x6) IF ID EX MEM WB

sub x30, x7, x29 IF ID EX MEM WB

add x31, x11, x5 IF ID EX MEM WB

sw x30, 0(x31) IF ID EX MEM WB

addi x12, x12, 2 IF ID EX MEM WB

bne x12, x13, TOP IF ID EX MEM WB

b) For one-issue, a loop needs 9 cycles. For two-issue, a loop needs 8 cycles. Hence, speed up is  $\frac{9}{8} = 1.25$

c) beqz x13, OUT

li x12, 0

jal ENT

TOP: lw x7, 0(x10)

lw x29, 4(x10)

sub x30, x7, x29

sw x30, 0(x11)

addi x12, x12, 2

addi x10, x10, 8

addi x11, x11, 8

ENT: bne x12, x13, TOP

OUT:

d) beq x13, DONE

li x12, 0

TOP: lw x7, 0(x6)

addi x12, x12, 2

lw x29, 4(x6)

addi x6, x6, 8

sub x30, x7, x29

sw x30, 0(x31)

bne x12, x13, TOP

e) One-issue needs 8 cycles a loop, two-issue needs 6 cycles a loop.

Speedup is  $\frac{8}{6} = 1.33$