Saravan Kumar Boddeda

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Education

Indian Institute of Technology Bombay — **Mumbai**
Bachelors of Technology in Electrical Engineering, **7.03 GPA** — **2023–present**

Sri Venkateswara Classes — **Visakhapatnam**
Intermediate/+2, **95.50%** — **2020–2022**

Navy Children School — **Visakhapatnam**
Matriculation, **92%** — **2020**

Scholastic Achievements

- Achieved **All India Rank 3000** in **JEE Advanced (2023)** among 0.15 million+ candidates across the country
- Secured **All India Rank 7000** in **JEE Main (2023)** among 1.2 million+ candidates across India
- Achieved a perfect **100% score in Physics and Maths** in the Andhra Pradesh Board Examination (2021-2022)

Courses Undertaken

Electrical	Digital Systems, Power Engineering, Microprocessors, Signal Processing, Analog Circuits, Control Systems, VLSI Design , EM Waves, Communications
Mathematics	Calculus, Differential Equations, Linear Algebra, Probability and Random Processes
Labs	Digital Circuits Lab, Power Engineering Lab, Chemistry Lab, Physics Lab, Makerspace Lab, Analog Lab, Microprocessor Lab , Electronic Devices Lab , Communications Lab
Others	Quantum Physics and Applications, Classical Physics, Computer Programming and Utilization, Economics, Introduction to Entrepreneurship, Sociology, Machine learning

Experience

Embedded Systems Intern — **Jun 2025–present**
Nirixense Technologies, Prof Siddhart Tallur

- Granted **letter of recommendation** for exceptional work on self-healing mesh network, recognizing contributions to developing an autonomous network topology that dynamically reconfigures routing paths in response to node failures
- Led the ideation and development of an **ultra-low-power embedded sensor node** for **structural health monitoring**
- Configured a custom **self-healing mesh network** for **LoRa communication** using the **STM32WL MCU**
- Incorporated a **two-stage path planning approach** combining **Flood Fill** and **Dijkstra** for optimal route selection
- Developing a central **4G gateway** to bridge the mesh network with the **cloud**, enabling secure and remote monitoring

Key Technical Projects

VLSI Design — **Sept 2025–present**
VLSI Design, Guide: Prof. Laxmeesha Somappa

- Designed transistor-level layouts for **X1/X2 inverter**, **NOR** gate and **DFF** on **Magic VLSI** using **Sky130A** PDK
- Verified post-extraction **timing and functionality** using **NGSPICE**, achieving rise time $\sim$20 ps
- Implemented a simplified **Q-learning agent (4×4 state-action space)** in **Verilog**, performing one Q-value update per clock cycle
- Followed complete **ASIC design flow**—RTL design, synthesis, place-and-route, and physical verification—using **Yosys–OpenLane**, generating post-synthesis/post-routing reports and final **GDSII** layout

AI-Assisted Wi-Fi Radio Resource Management — **Oct 2025–Dec 2025**
Inter-IIT Tech Meet 14.0 (Arista Networks)

- Architected a **Multi-Timescale Control Loop** system integrating a sub-second **"Fast Loop"** for real-time interference avoidance and a **"Slow Loop"** for global configuration updates
- Implemented **Bayesian Optimization** engine integrated with **NS-3** to tune Tx Power, Channel Width, and OBSS-PD, achieving **31.5% increase** in mean edge-client throughput and eliminating bottlenecks by **1364%**
- Developed a **Graph Attention Network (GAT)** surrogate model to predict throughput with **92%** R^2 **accuracy**, replacing expensive simulations to reduce optimization inference time by **1000**× for real-time control
- Modeled enterprise environments using **NS-3** (Nakagami-m fading, Spectrum WifiPhy) to validate algorithms, balancing trade-offs between coverage maximization and **P95 retry rate** reduction

IITB-CPU V1.5 — **Jun 2025 - Aug 2025**
Electronics and Robotics Club

- Designed and implemented a **16-bit RISC CPU** using a **finite state machine (FSM)** architecture with 23 pipeline states for instruction fetch, decode, execute, memory access, and write-back
- Developed and verified **combinational and sequential logic modules** for arithmetic, branching, control flow, and memory access operations using **ModelSim** simulations
- Optimized the **state transition flow** and datapath design to minimize latency and improve instruction throughput, achieving reduced cycle count per instruction

Frequency Analysis of Nonlinear Circuit **Jan 2025–April 2025**

Microprossors, Guide: Prof. Shalab Gupta

- Generated dual-tone test signals using the **ESP32 DAC** to study intermodulation distortion in nonlinear diode circuits
- Implemented **coherent sampling** on an **8051 (PT-51)** microcontroller for synchronized data acquisition and amplitude estimation
- Performed **FFT-based harmonic analysis**, observing the effect of DC offset on harmonic and intermodulation components
- Developed firmware for **I–Q amplitude detection** to extract magnitudes of key tones (e.g., 27 Hz, 73 Hz, 154 Hz) from multi-tone inputs and applied averaging and phase-alignment correction algorithms to suppress noise and enhance amplitude stability across multiple acquisition cycles.

Combinatorial and Sequential Circuits **Jun 2024–Dec 2024**

Digital Circuits lab, Guide: Prof. Saurabh Lodha

- Designed and synthesized combinational and sequential digital circuits in **VHDL** using **Intel Quartus Prime**, including an **Arithmetic Logic Unit (ALU)**, **BCD adder**, and **sequence detector**
- Developed and verified **behavioral, dataflow,and structural architectures** through **testbench** and **RTL simulations**
- Implemented a **FSM** for word detection and performed **scan-chain testing** on an **XEN10 FPGA board**
- Implemented a simple **two-layer neural network** on FPGA, including **fixed-point arithmetic** for neuron activation and **parallel multiply–accumulate (MAC)** operations for real-time inference

8051 Microcontroller Interfacing **Sept 2025–present**

Digital Circuits lab, Guide: Prof. S

- Designed and implemented a **clock pulse generator**, **8-bit adder**, and **2×2 matrix multiplier** entirely in **8051 Assembly** with optimized instruction cycles, demonstrating low-level control over arithmetic and timing operations
- Configured on-chip **timers**, **external interrupts**, and serial communication interfaces (**SPI/UART**) for seamless integration with **ADC**, **LCD modules**, and multiple sensor peripherals using polling and interrupt-driven mechanisms
- Developed a complete **RSA encryption–decryption algorithm** from scratch in Assembly, including **key generation**, **modular exponentiation**, **encryption**, and **modular decryption** routines with efficient memory management

Autonomous SLAM Bot **April 2025–May 2025**

Electronics and Robotics Club

- Simulated a fully autonomous differential-drive robot in a custom **Gazebo** environment using **ROS2 Humble** with **SLAM Toolbox** for real-time map generation, localization, and path planning; configured and tuned **AMCL** and **Navigation2**
- Established bidirectional **UART communication protocol** between **Raspberry Pi 5** (ROS2 master node) and **ESP32 with motor controller** to execute **Twist velocity commands**, implement **PID-based motor control**,
- Deployed real-world **SLAM mapping** using a **3D LiDAR sensor** on Raspberry Pi, achieving autonomous point-to-point navigation accuracy through real-time pose estimation, map updates, and sensor fusion with **IMU data**

Hardware Hacking **March 2025**

Electronics and Robotics Club

- Investigated **timing-based side-channel vulnerabilities** in password verification and cryptographic routines, demonstrating how response-time variations can leak sensitive information
- Conducted **Simple Power Analysis (SPA)** on RSA and password-checking routines to identify data-dependent instruction patterns (e.g., **square-and-multiply**) that reveal exponent bits or password bytes
- Used **ChipWhisperer Nano** with **STM32**-based targets to capture, align, average and analyze power traces; applied statistical scoring and visualization to extract key-dependent patterns from noisy measurements
- Evaluated and validated countermeasures such as **constant-time** comparison, **blinding**, and **dummy operations** to reduce leakage and harden implementations

Other Technical Projects

Drone Assembly and Calibration **Jan 2024-April 2024**

Makerspace, Guide: Prof. Joseph John

*Part of an **6-member team** to make a fully working Quadcopter*

- Designed functional **quadcopter drone** from scratch, including frame construction, motor installation, and wiring
- Implemented **PID control** combined with a gyroscope to improve flight stability, Used **Arduino Nano** as the controller to process sensor data, optimizing the drone's responsiveness to changes in orientation and ensuring smooth flight dynamics.
- Integrated a **Wi-Fi card** to establish a robust wireless communication link, facilitating remote control through a **Mobile Joystick Interface**, allowing for user interaction and precision maneuvering of the quadcopter

Fake News Detection Using Machine Learning **Dec 2023**

Winter in Data Science,Analytical Club

- Engineered a comprehensive **Fake news detection system** that involved data cleaning, detailed feature engineering, and the application of **TF-IDF vectorization** for text preprocessing.This process effectively transformed raw datasets into structured data,Achieved an accuracy over **90%** using **Decision Tree models** for reliable classification and prediction
- Implemented and rigorously compared a diverse set of **machine learning models**, including **Logistic Regression**, **Decision Trees**, and other classifiers. Employed advanced evaluation metrics such as **precision**, **recall**, **F1 score**, and confusion matrices to conduct thorough assessment of model performance across multiple datasets and scenarios

Analog Computer **Jan 2025 - April 2025**

Analog Lab, Guide: Prof. Anil Kottantharayil

- Built an **analog computer** to solve second-order differential equations using **op-amp–based amplifiers** and **dual integrator** feedback networks
- Implemented precision **Howland current-source integrators** to enhance linearity,and long-term stability of integration
- Designed and experimentally validated nonlinear analog modules including **log/antilog converters**, **square-root circuits**, and **Schmitt triggers** for analog computation and waveform shaping
- Developed and analyzed **Butterworth** and **Chebyshev active filters** using the **Sallen–Key topology**, verifying frequency response and cutoff characteristics through Bode plot measurements

ESP32-based AI Chatbot **Jan 2025**

Electronics and Robotics Club

- Built an AI chatbot on **ESP32** using **Gemini API** and **Text-to-Speech (TTS)** with I2S audio interface for real-time voice interaction
- Implemented dual ESP32 architecture with master-slave configuration for parallel STT and AI+TTS processing, communicating via UART protocol at 115200 baud rate
- Optimized **PSRAM allocation** and implemented **chunked streaming** to handle API responses within 4MB memory constraints, reducing latency by buffering audio frames efficiently

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Mentorship and Leadership Roles

Institute Electronics & Robotics Secretary **Mar 2025–Present**

Institute Technical Council, IIT Bombay

- Leading a **13-member team** organizing 20+ events, hackathons, and discussions for a community of **8000+ enthusiasts**
- Promoted club-community interaction by driving **social media** engagement and organizing community meetings
- Optimized the tenure timeline and a budget of INR **0.8 million+** to ensure effective outreach and successful events
- Led the organizing team of Institute's largest hardware competition with more than **800 participants** out of 1200 students, managed all logistics and budget allocation

Convener **Mar 2024–Mar 2025**

Electronics and Robotics Club, IIT Bombay

- Organized **Institute's largest tech event, XLR8'24**, a month-long program for over **900 first-year students**, guiding participants in building functional **four-wheel bots** using the **Raspberry Pi Pico** with **gesture-based control**
- Strengthened club-community engagement by curating a strong social media presence and impactful technical workshops on **Docker**, **IoT**, and a month-long online **ROS2** series to foster hands-on learning and collaboration
- Conducted a first-of-its-kind **2-day workshop on Embedded Security**, covering concepts such as **side-channel analysis** including **timing attacks** and **power analysis**, both in simulation and on actual hardware using **ChipWhisperer Nano**

Operations Coordinator **Sep 2024–Jan 2025**

Inter-IIT Tech Meet, IIT Bombay

- Part of a **50-member team** organizing a 3-month event with **2000+ footfall** and **15+ leading MNCs**
- Led execution of technical problem statements from **ISRO** and **Rigbetel Labs**; coordinated with **50+ student representatives** to manage logistics, hospitality, and smooth on-ground operations for participants and stakeholders

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Technical Skills

Programming	C++, Python, Embedded C, VHDL, Verilog, Assembly, HTML, Docker, LaTeX
Libraries	NumPy, Pandas, Matplotlib, Scikit-learn
Softwares	Arduino IDE, Keil, KiCAD, Quartus, MATLAB, ROS & ROS2, Gazebo, Fusion 360, Jupyter, Anaconda

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Extra Curricular Activities

- Mentored a **4-member team** for the national competition *Innovation Story*, guiding them to **3rd place in India** by addressing a real-world challenge through a solution pitch and working prototype **(2024)**
- Mentoring **three 4-member teams** for the institute's technical summer projects in Mechatronics, focusing on **autonomous warehouse** systems, **healthcare robots**, and **multi-terrain vehicles** **(2025)**
- Volunteered with NGO **GnaanU** (*Smile Foundation*) to conduct a hands-on **STEM workshop** on building mobile-controlled 4-wheel bots for school children, promoting curiosity and technical awareness **(2025)**
- Successfully completed rigorous one-year training in **Hockey** under the **NSO** programme at IIT Bombay **(2023–2024)**
- Part of E-Cell's digital outreach team and helped organize **E-Summit 2024**, boosting national visibility for **India's largest student-run startup body** **(2024)**
- Represented school at district level in the prestigious *INSPIRE MANAK* National Competition; presented an **energy-saving innovation** and was recognized for **creativity and problem-solving** **(2019)**