Index

架構圖總共有以下Part:

Part 1. ALU:
- full_adder.v
- alu_1bit.v
- alu_1bit32th.v
- ALU.v

Part 2. 乘法器:
- Multiplier.v
- HiLo.v

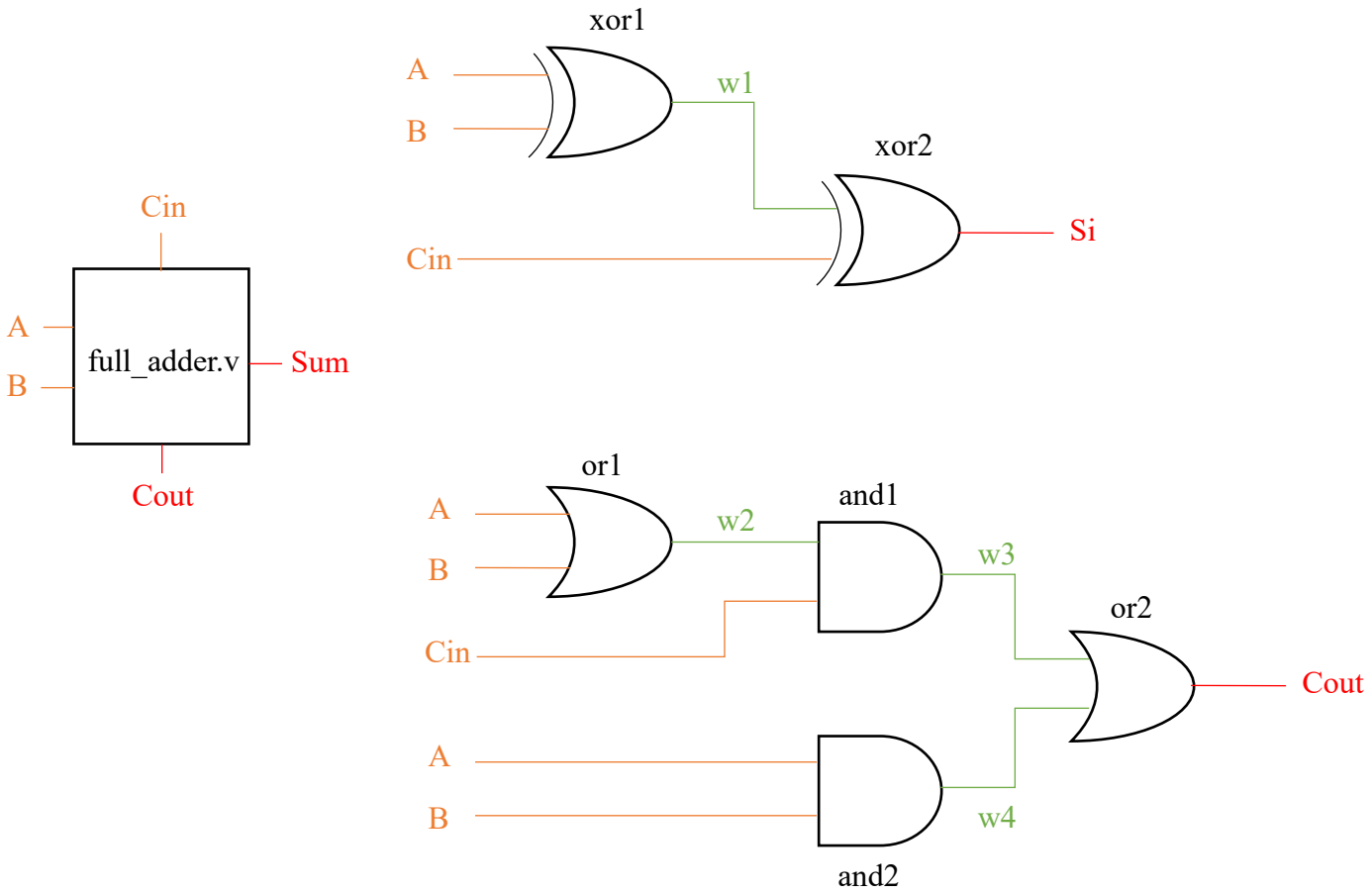
Part 3. 移位器:
- mux_2to1.v
- Shifter.v

Part 4. 輸入輸出:
- ALUControl.v
- MUX.v

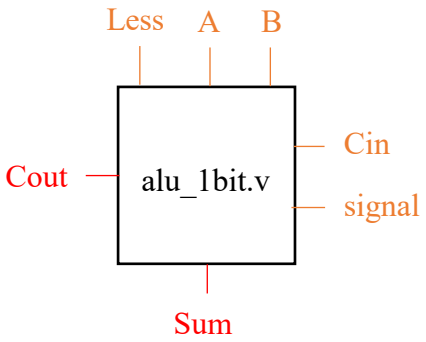
Part 5. Total:
- TotalALU.v

Part 6. 測試檔:
- tb_ALU.v

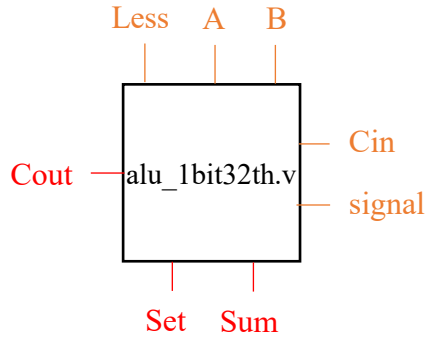
full_adder.v


xor1
A
B
w1
xor2
Cin
Si
Cin
A
full_adder.v
Sum
B
Cout
or1
A
B
w2
and1
w3
Cin
or2
Cout
A
B
w4
and2

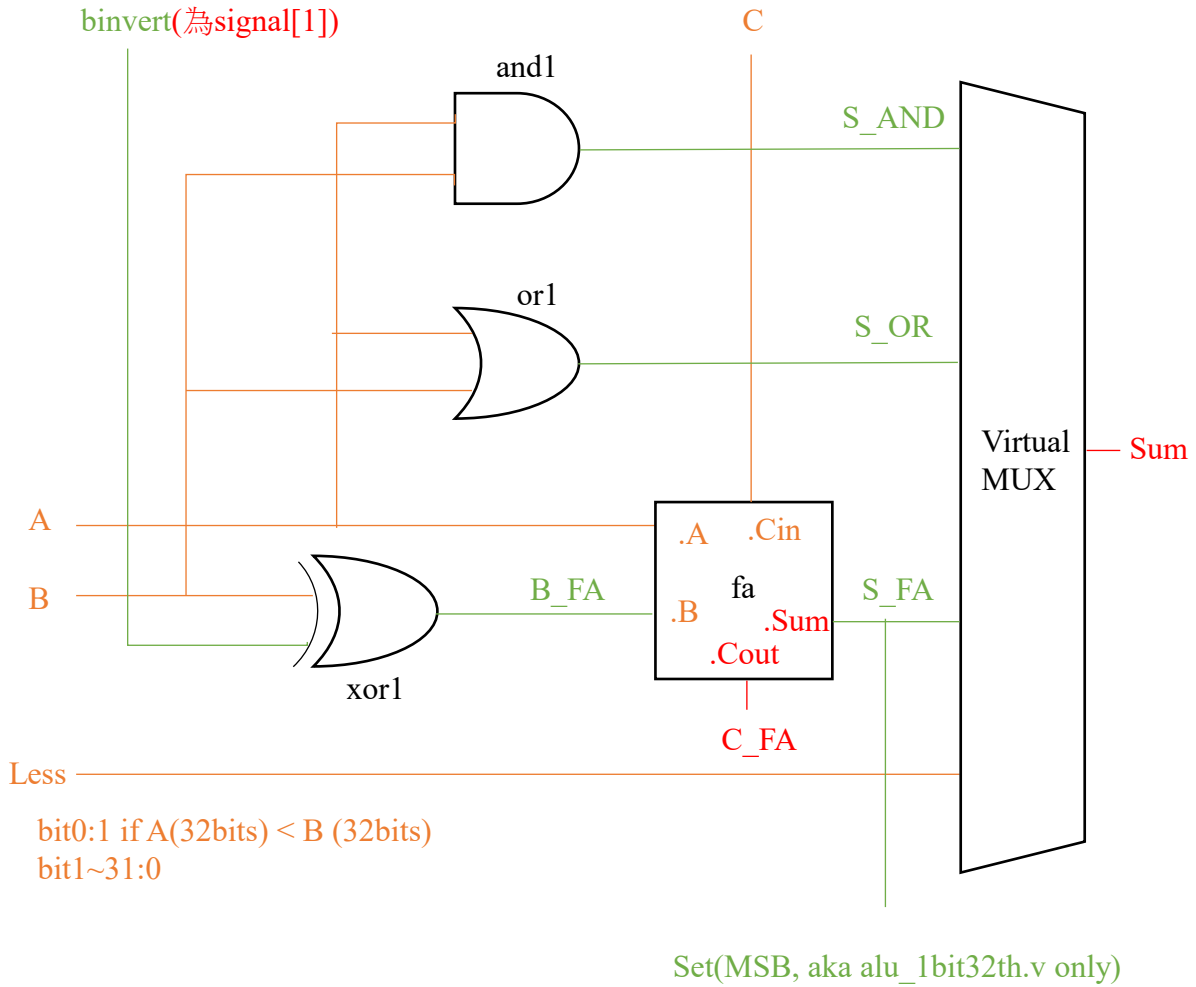
alu_1bit.v



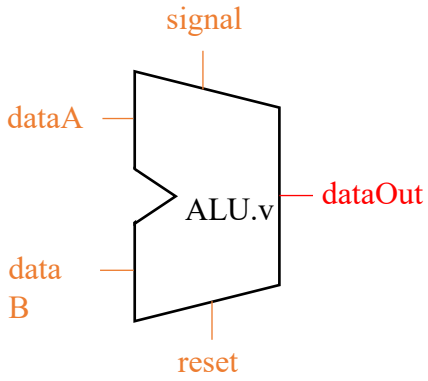
alu_1bit32th.v

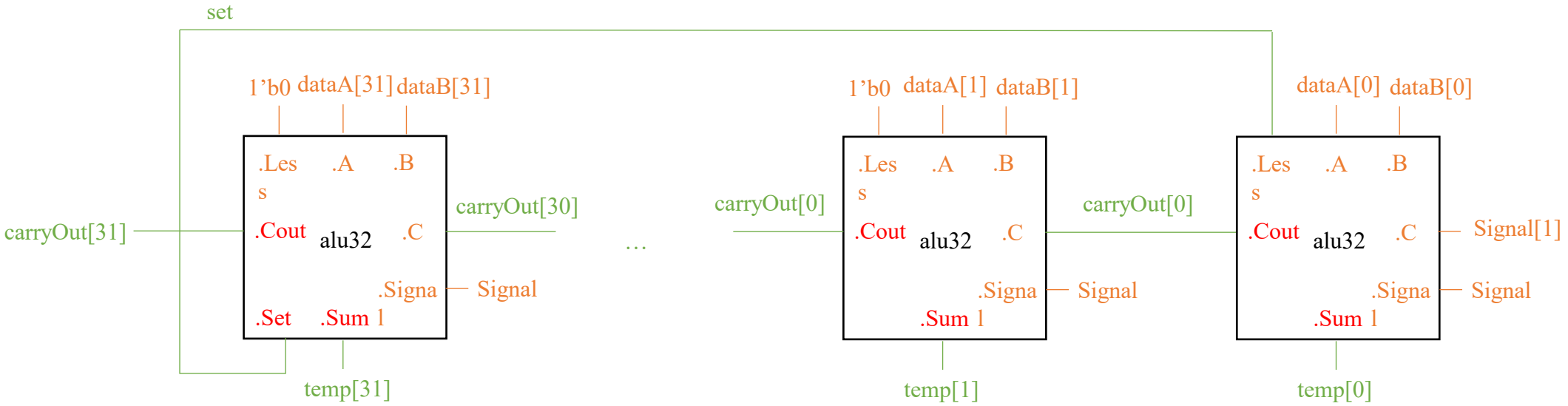


alu_1bit.v / alu_1bit32th.v (32bits比1bit多一個set)

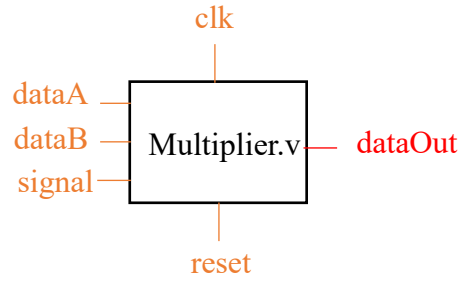


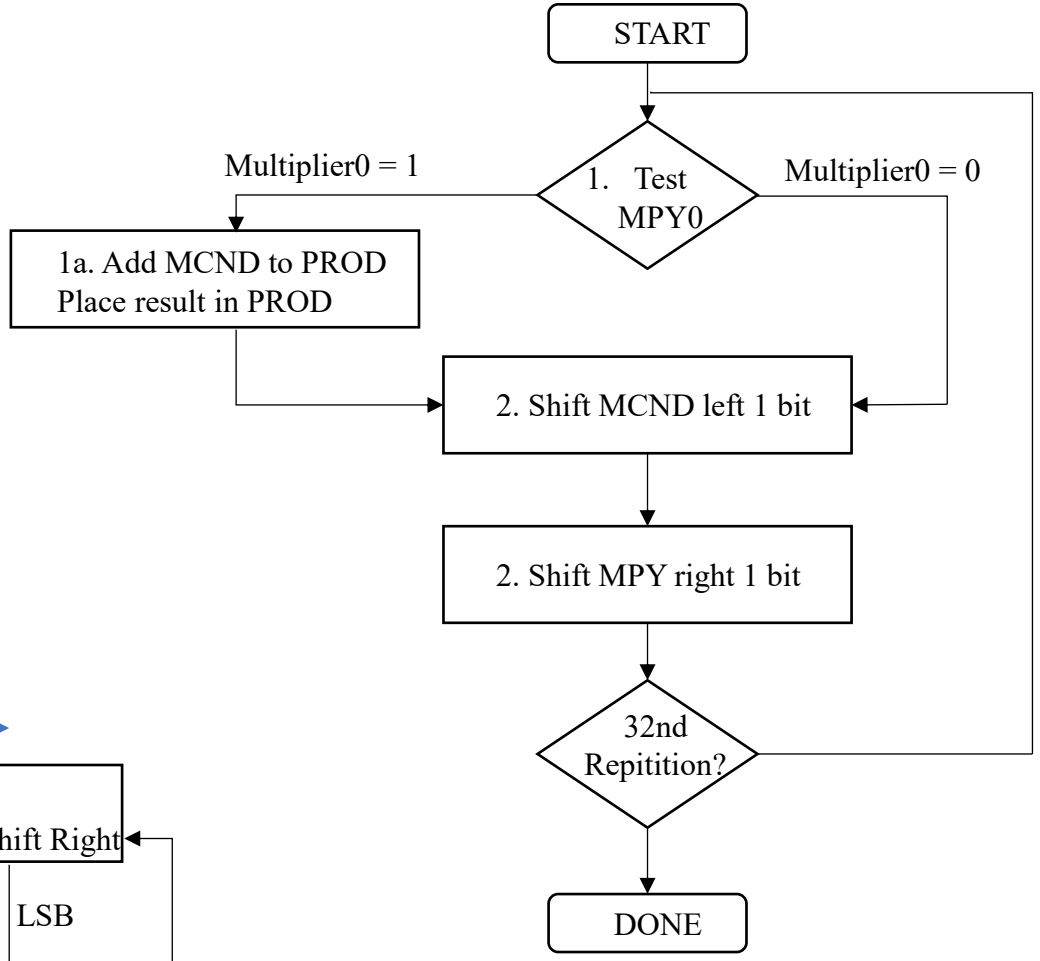
ALU.v

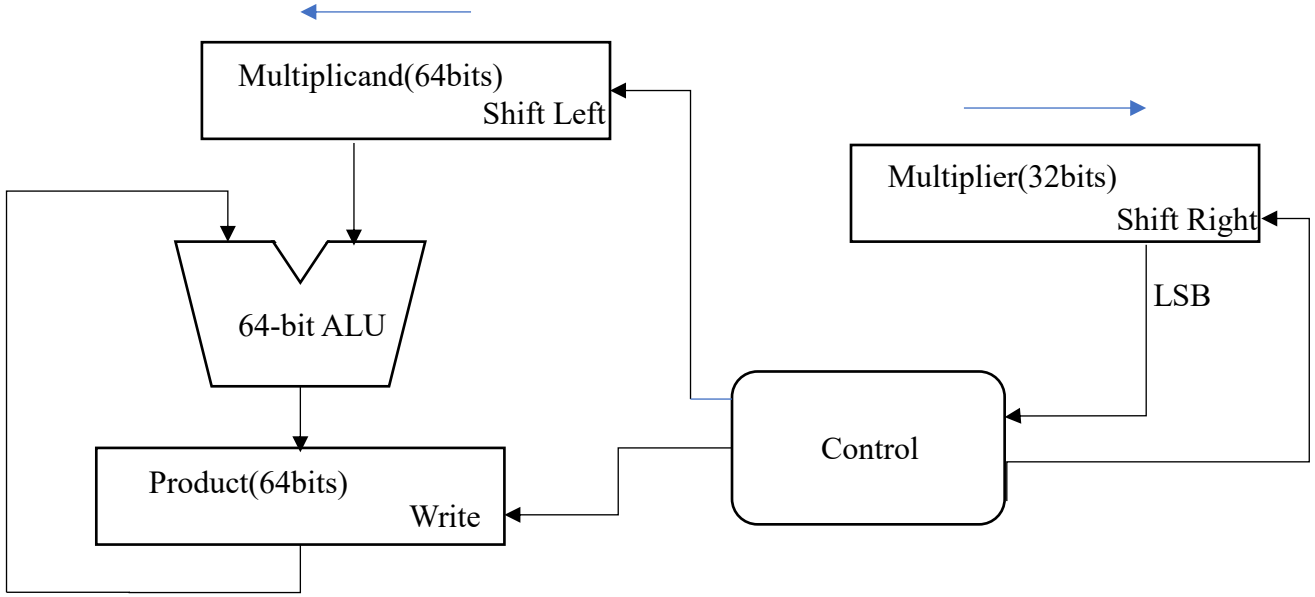

signal
dataA
ALU.v
dataOut
data
B
reset


set
1'b0
dataA[31]
dataB[31]
.Les
s
.A
.B
carryOut[31]
.Cout
alu32
.C
carryOut[30]
.Signa
Signal
.Set
.Sum
l
temp[31]
…
1'b0
dataA[1]
dataB[1]
carryOut[0]
temp[1]
dataA[0]
dataB[0]
Signal[1]
temp[0]

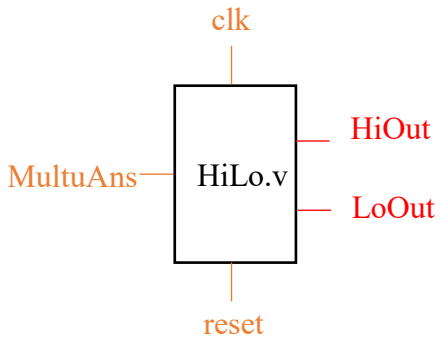
Multiplier.v



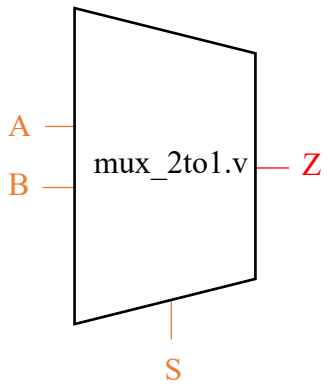




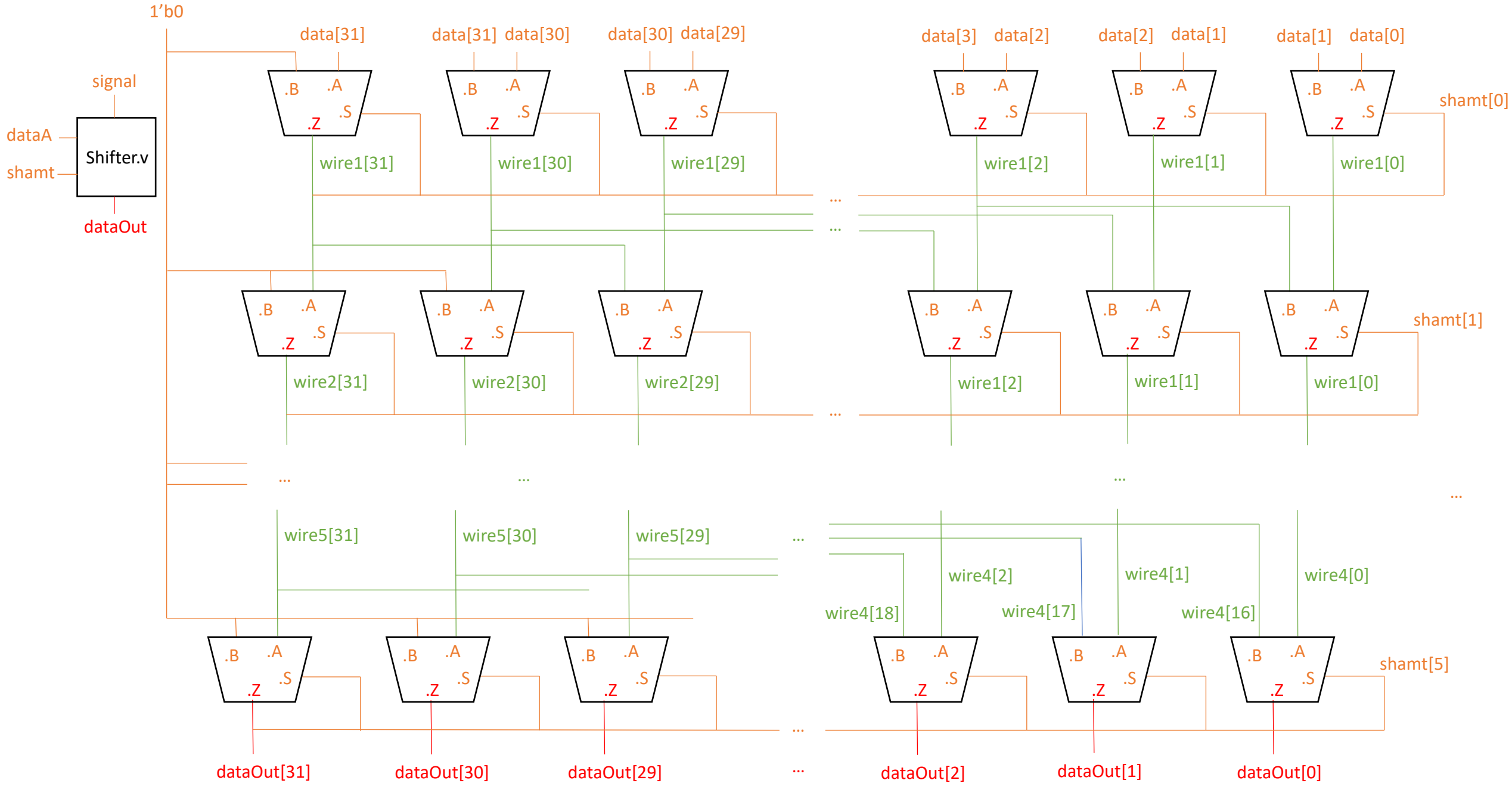
HiLo.v



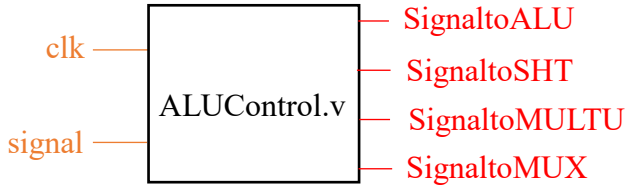
mux_2to1.v



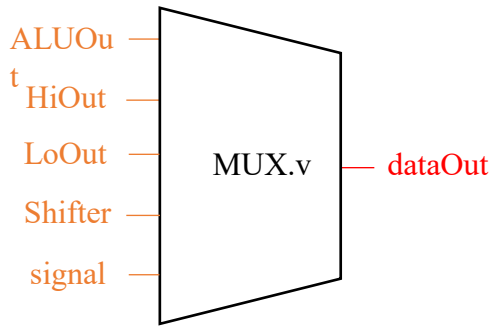
Shifter.v


1'b0
signal
dataA
shamt
Shifter.v
dataOut
data[31]
data[31] data[30]
data[30] data[29]
data[3] data[2]
data[2] data[1]
data[1] data[0]
.B .A .S .Z
wire1[31]
wire1[30]
wire1[29]
wire1[2]
wire1[1]
wire1[0]
shamt[0]
wire2[31]
wire2[30]
wire2[29]
shamt[1]
wire5[31]
wire5[30]
wire5[29]
wire4[18]
wire4[2]
wire4[17]
wire4[1]
wire4[16]
wire4[0]
shamt[5]
dataOut[31]
dataOut[30]
dataOut[29]
dataOut[2]
dataOut[1]
dataOut[0]

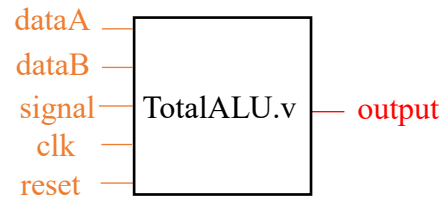
ALUControl.v

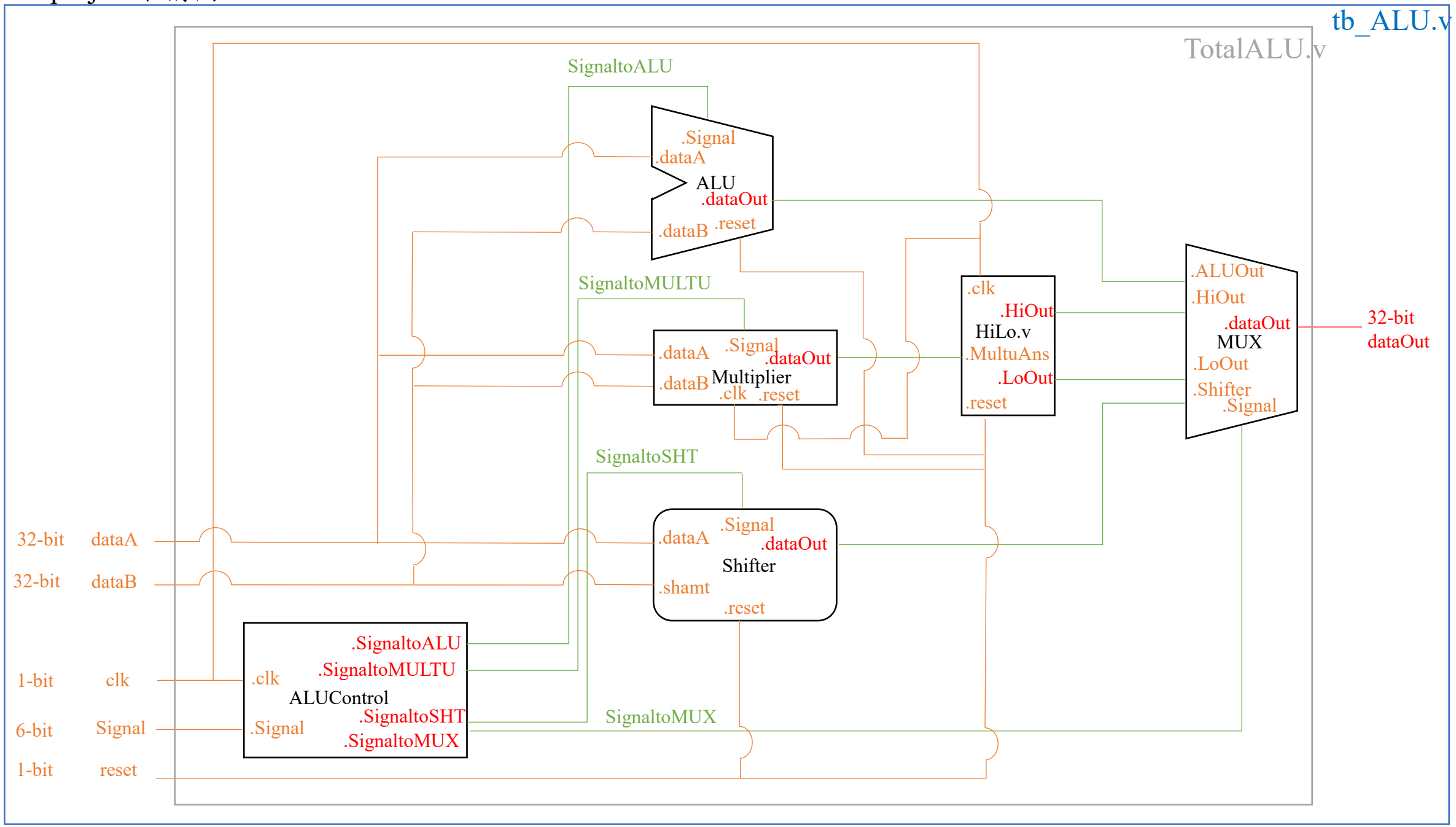


MUX.v



TotalALU.v



Midterm project架構圖

(testbench)
tb_ALU.v