DSD HW4 REPORT

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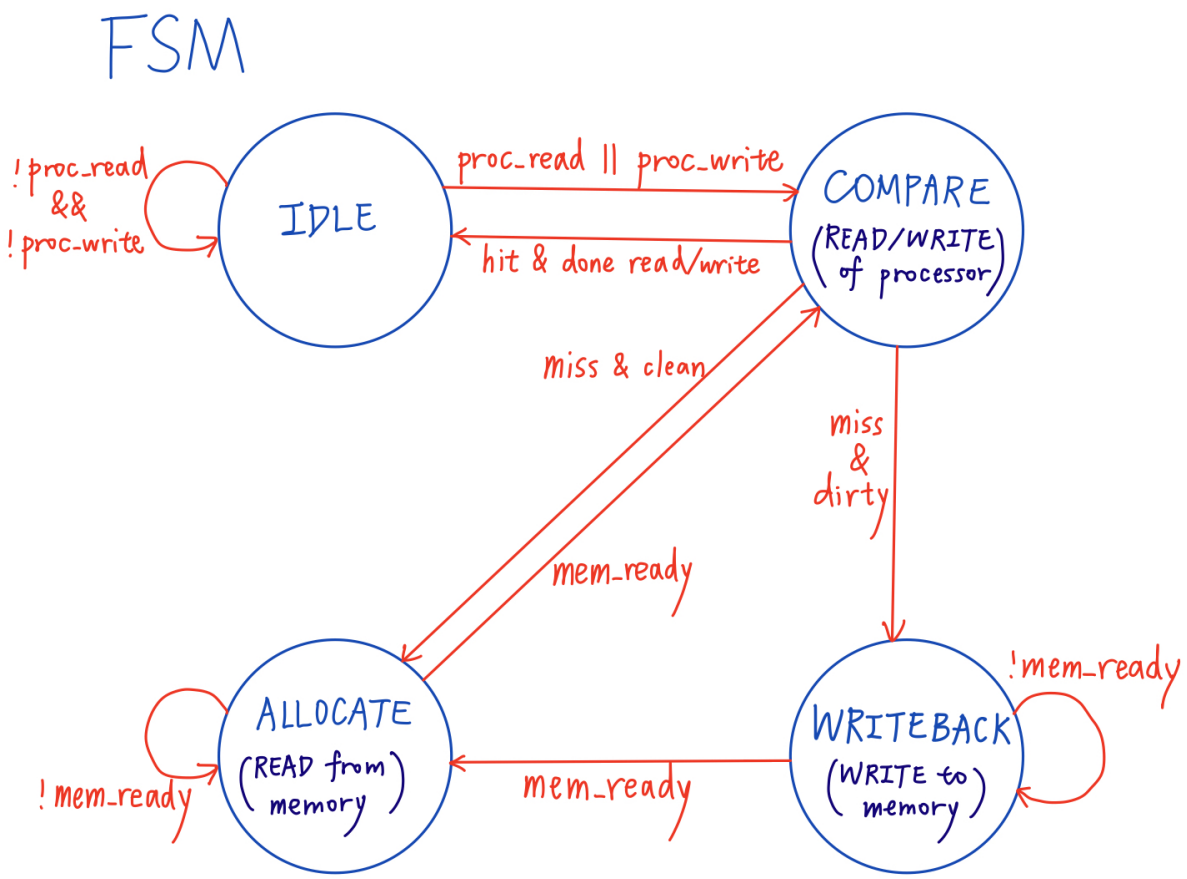
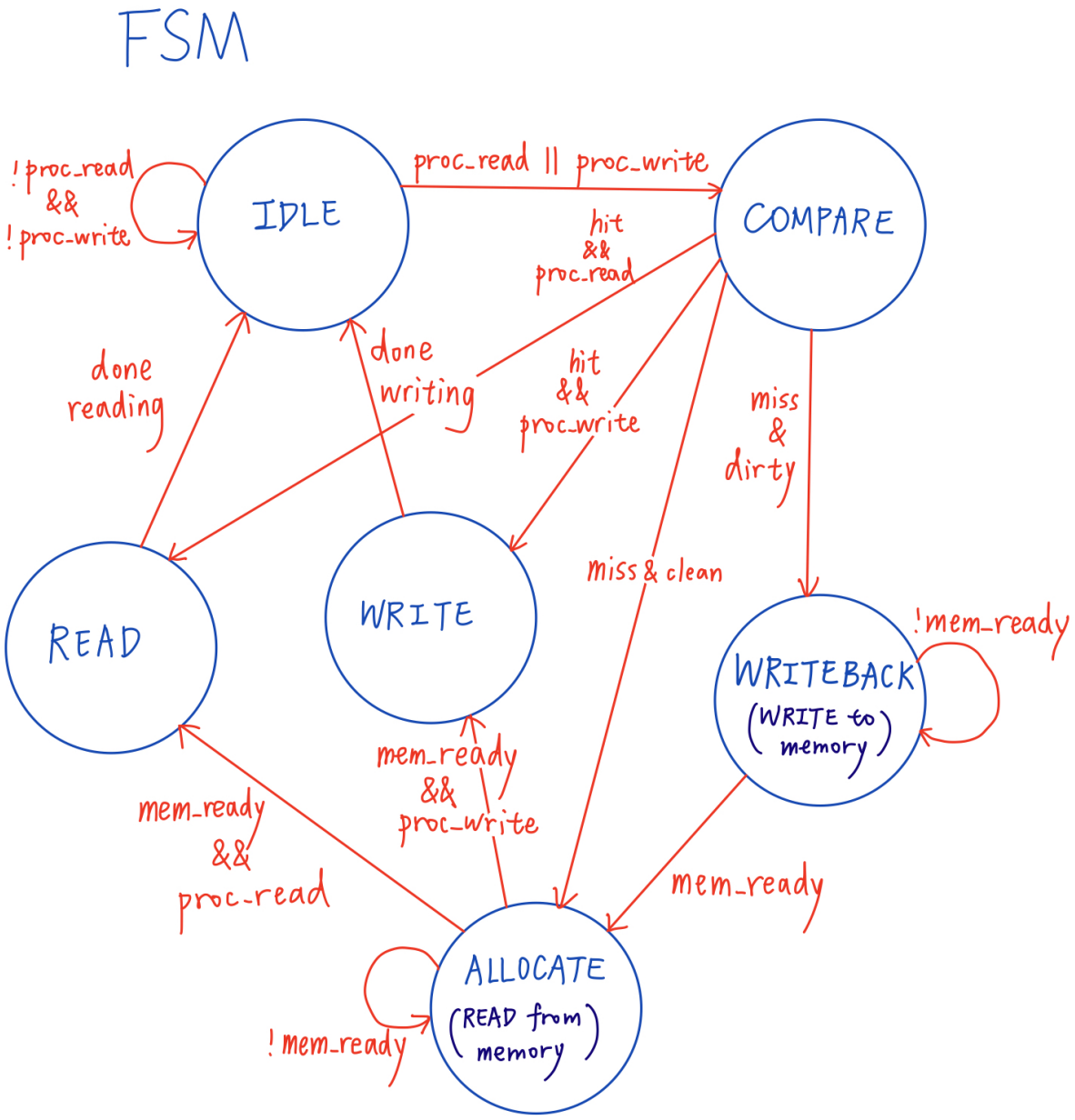
My cache design: Write Back Cache

1. Direct mapped cache
    - Every read/write operation of the proc./cache interface is done in COMPARE state.
    - Every instruction starts and ends at IDLE state.



2. 2-way set associative cache
    - Read/write operations are move to READ and WRITE states respectively.
    - Every instruction starts and ends at IDLE state.
    - If a miss is countered, I choose to do read/write operations of cache/mem. interface on the first block of the set.
    - Hit/miss signals are preprocessed.



hit = hit1 || hit2
hit1 = valid1 && tag_match1
hit2 = valid2 && tag_match2
miss = !hit

miss_clean1 = !hit1 && !dirty1
miss_clean2 = !hit2 && !dirty2
miss_dirty1 = !hit1 && dirty1
miss_dirty2 = !hit2 && dirty2

RTL Simulation Result

1. cache_dm.v

```
Memory has been initialized.

Processor: Read initial data from memory.
    Done correctly so far! ^_^

Processor: Write new data to memory.
    Finish writing!

Processor: Read new data from memory.
    Done correctly so far! ^_^

==== CONGRATULATIONS! Pass cache read-write-read test. ====

Finished all operations at:               184395 ns
Exit testbench simulation at:             184495 ns


Simulation complete via $finish(1) at time 184495 NS + 0
./tb_cache.v:183         $finish;
ncsim> exit
```

2. cache_2way.v

```
Memory has been initialized.

Processor: Read initial data from memory.
    Done correctly so far! ^_^

Processor: Write new data to memory.
    Finish writing!

Processor: Read new data from memory.
    Done correctly so far! ^_^

==== CONGRATULATIONS! Pass cache read-write-read test. ====

Finished all operations at:               199745 ns
Exit testbench simulation at:             199845 ns


Simulation complete via $finish(1) at time 199845 NS + 0
./tb_cache.v:183         $finish;
ncsim> exit
```

Gate-Level result

1. cache_dm_syn.v

```
Memory has been initialized.

Processor: Read initial data from memory.
    Done correctly so far! ^_^

Processor: Write new data to memory.
    Finish writing!

Processor: Read new data from memory.
    Done correctly so far! ^_^

==== CONGRATULATIONS! Pass cache read-write-read test. ====

Finished all operations at:               184395 ns
Exit testbench simulation at:             184495 ns


Simulation complete via $finish(1) at time 184495 NS + 0
./tb_cache.v:183         $finish;
ncsim> exit
```

2. cache_2way_syn.v

```
Memory has been initialized.

Processor: Read initial data from memory.
    Done correctly so far! ^_^

Processor: Write new data to memory.
    Finish writing!

Processor: Read new data from memory.
    Done correctly so far! ^_^

==== CONGRATULATIONS! Pass cache read-write-read test. ====

Finished all operations at:               199745 ns
Exit testbench simulation at:             199845 ns


Simulation complete via $finish(1) at time 199845 NS + 0
./tb_cache.v:183         $finish;
ncsim> exit
```

Observation:

Although 2-way associative cache is supposed to save time of miss penalty, but the effect doesn't show much.

Guess it is caused by the testbench, which contains little close and repeated processor address.

Synthesis Result

1. Direct-mapped Cache

   Timing (slack>0):

```
Point                                    Incr       Path
-----------------------------------------------------------
clock CLK (rise edge)                    0.00       0.00
clock network delay (ideal)              0.50       0.50
input external delay                     0.30       0.80 f
proc_addr[4] (in)                        0.01       0.81 f
U7213/Y (CLKBUFX3)                       0.26       1.07 f
U4387/Y (CLKINVX1)                       0.36       1.43 r
U7543/Y (NOR2X1)                         0.16       1.59 f
U7544/Y (AND2X1)                         0.36       1.95 f
U4385/Y (CLKBUFX3)                       0.59       2.54 f
U4176/Y (CLKBUFX3)                       0.66       3.21 f
U4175/Y (CLKBUFX3)                       0.55       3.76 f
U4032/Y (CLKBUFX3)                       0.61       4.37 f
U8232/Y (AOI22X1)                        0.31       4.68 r
U8236/Y (NAND4X1)                        0.25       4.93 f
U4266/Y (XNOR2X1)                        0.20       5.13 r
U4264/Y (NAND4X1)                        0.14       5.27 f
U4130/Y (NOR4X1)                         0.19       5.47 r
U4128/Y (NAND4X1)                        0.19       5.66 f
U4251/Y (NOR2BX1)                        0.35       6.01 r
U3668/Y (NAND2X1)                        0.16       6.17 f
U3857/Y (CLKBUFX3)                       0.24       6.41 f
U3446/Y (NOR3X1)                         0.56       6.97 r
U3689/Y (NAND2X1)                        0.43       7.40 f
U4152/Y (CLKBUFX3)                       0.48       7.88 f
U4277/Y (OA22X1)                         0.39       8.27 f
U4274/Y (OAI221XL)                       0.17       8.44 r
proc_rdata_reg[0]/D (DFFQX1)             0.00       8.44 r
data arrival time                                   8.44

clock CLK (rise edge)                   10.00      10.00
clock network delay (ideal)              0.50      10.50
clock uncertainty                       -0.10      10.40
proc_rdata_reg[0]/CK (DFFQX1)            0.00      10.40 r
library setup time                      -0.09      10.31
data required time                                 10.31
-----------------------------------------------------------
data required time                                 10.31
data arrival time                                  -8.44
-----------------------------------------------------------
slack (MET)                                         1.87
```

Area:

```
Number of ports:                          386
Number of nets:                          6517
Number of cells:                         6314
Number of combinational cells:           4881
Number of sequential cells:              1433
Number of macros/black boxes:               0
Number of buf/inv:                       1141
Number of references:                      43
[
[Combinational area:              42609.831524
[Buf/Inv area:                     7677.340127
[Noncombinational area:           36947.306452
[Macro/Black Box area:                0.000000
[Net Interconnect area:          879204.485046
[
[Total cell area:                 79557.137976
[Total area:                     958761.623022
```

2. 2-way associative Cache

   Timing (slack>0):

```
[
[  Point                                   Incr       Path
[  -----------------------------------------------------------
[  clock CLK (rise edge)                   0.00       0.00
[  clock network delay (ideal)             0.50       0.50
[  state_reg[2]/CK (DFFQX1)                0.00 #     0.50 r
[  state_reg[2]/Q (DFFQX1)                 0.46       0.96 r
[  U6807/Y (CLKINVX1)                      0.26       1.22 f
[  U6804/Y (XNOR2X1)                       0.27       1.50 r
[  U4550/Y (NAND4BX1)                      0.15       1.65 f
[  U4549/Y (NAND2X1)                       0.21       1.85 r
[  U3374/Y (AOI31X1)                       0.22       2.08 f
[  U4356/Y (NOR2X1)                        0.49       2.57 r
[  U4424/Y (NAND2X1)                       0.26       2.83 f
[  U4158/Y (NOR2X1)                        0.58       3.40 r
[  U4420/Y (NAND2X1)                       0.43       3.83 f
[  U3934/Y (CLKBUFX3)                      0.62       4.45 f
[  U4045/Y (CLKBUFX3)                      0.55       5.00 f
[  U4756/Y (OAI222XL)                      0.46       5.47 r
[  cch2_reg[0][0]/D (DFFX1)                0.00       5.47 r
[  data arrival time                                  5.47
[
[  clock CLK (rise edge)                  10.00      10.00
[  clock network delay (ideal)             0.50      10.50
[  clock uncertainty                      -0.10      10.40
[  cch2_reg[0][0]/CK (DFFX1)               0.00      10.40 r
[  library setup time                     -0.08      10.32
[  data required time                                10.32
[  -----------------------------------------------------------
[  data required time                                10.32
[  data arrival time                                 -5.47
[  -----------------------------------------------------------
[  slack (MET)                                        4.85
```

Area:

```
Number of ports:                          386
Number of nets:                          7166
Number of cells:                         5947
Number of combinational cells:           4507
Number of sequential cells:              1440
Number of macros/black boxes:               0
Number of buf/inv:                       1007
Number of references:                      43
[
[Combinational area:              46615.695450
[Buf/Inv area:                     8200.139482
[Noncombinational area:           38408.766956
[Macro/Black Box area:                0.000000
[Net Interconnect area:          932964.745422
[
[Total cell area:                 85024.462406
[Total area:                    1017989.207829
```

Observation:

The slack of 2-way cache is much longer than that of direct_mapped cache, while its area is slightly larger than dm cache's area.

Discussions

- After the read/write sequence in the testbench is finished, a well-functioned cache should write all the dirty datas back to memory. However, I haven't figure out how to

implement this.

- In the middle of coding, I had a struggle about when the stall signal should be pilled. After reading the tb code, I found out that every instruction is called after the stall signal is being pulled down, so I pulled it up whenever an instruction is received and down whenever the read/write is done, and the cache is ready.
- I wasted a lot of cycles on IDLE states. After each read/write is done, I can just jump to COMPARE state if either proc_read or proc_write is high, so it is a way to improve my design.
- After this homework, I fell like I understand a little more about cache than last semester when I was learning computer architecture; and also, a little better in RTL coding.