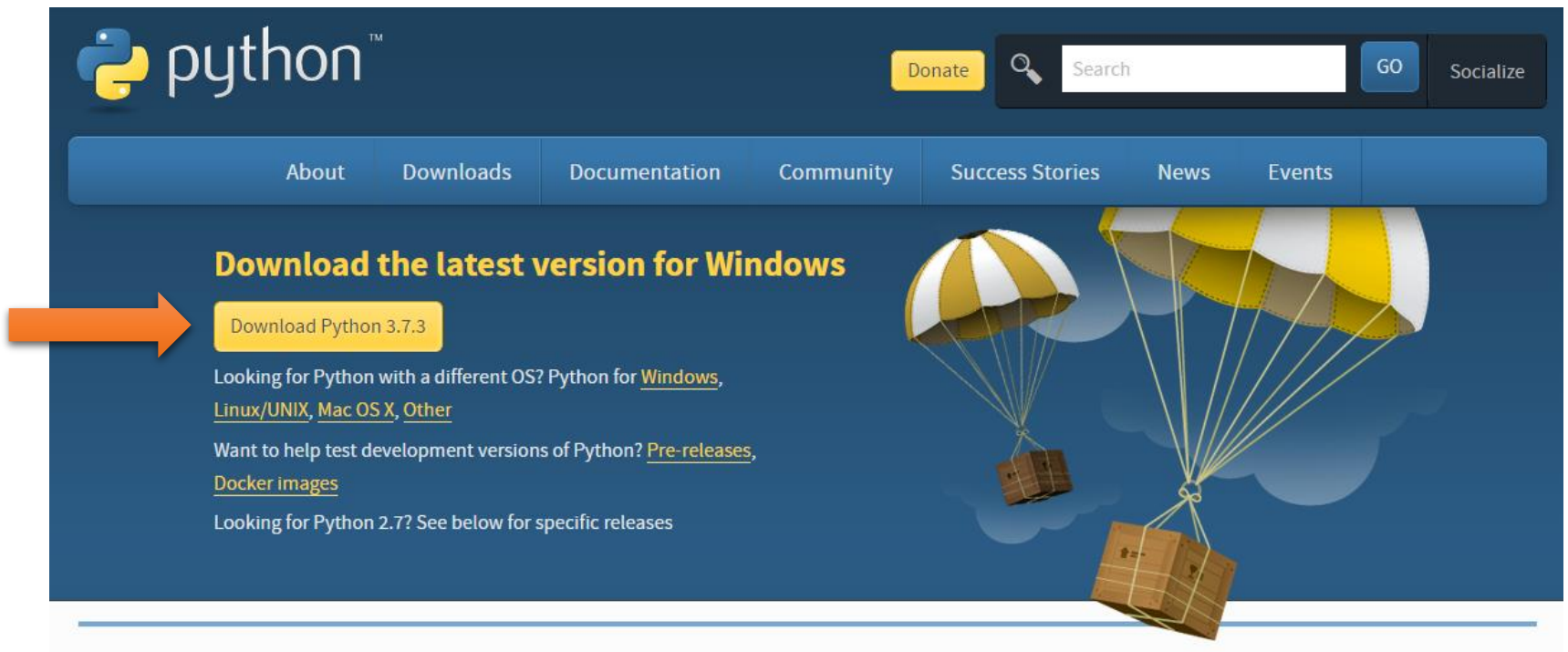


How to Use Generate?

Example: `hasHazard_generate.py`

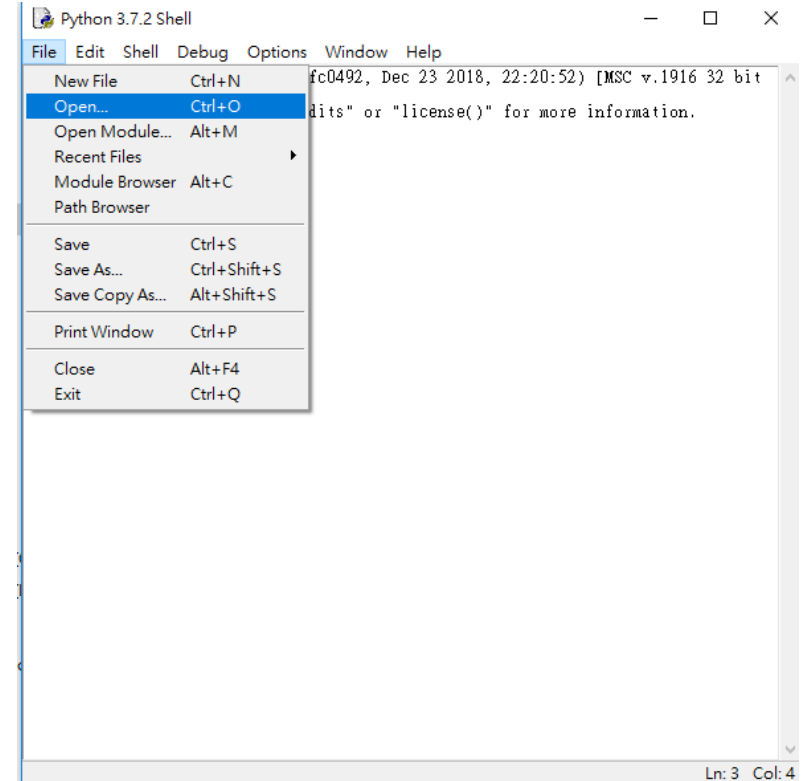
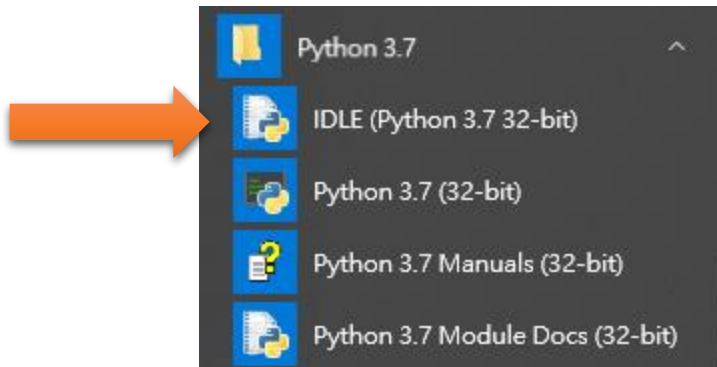
The Simplest Way: Python IDLE

- Download Python first (latest preferred)
 - <https://www.python.org/downloads/>



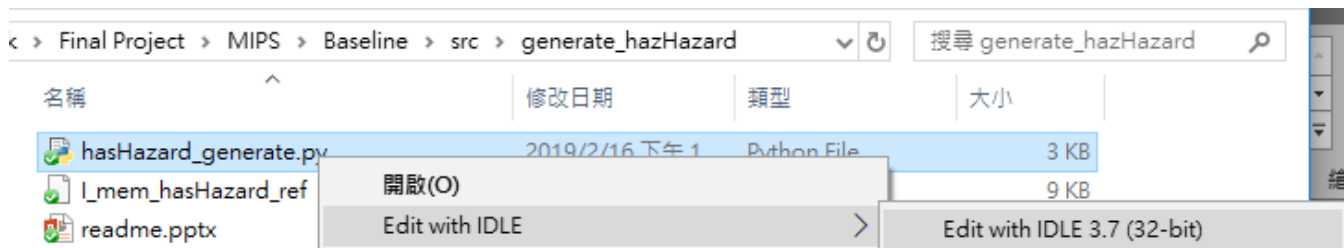
Open File: Method 1

- Choose IDLE
- File → Open...



Open File: Method 2

- Right click the file
- Ex: hasHazard_generate.py




- And you will see the code:

```
def fib(n):  
    assert(n >= 3)  
    output = [0, 1]  
    for i in range(2,n):  
        a = output[i-2]  
        b = output[i-1]  
        output = output + [a+b]  
    return output  
  
# Modify number of sequence here  
# Note: nb >= 3 && nb <= 47 (if nb >= 48, there will be overflow)  
nb = 16
```

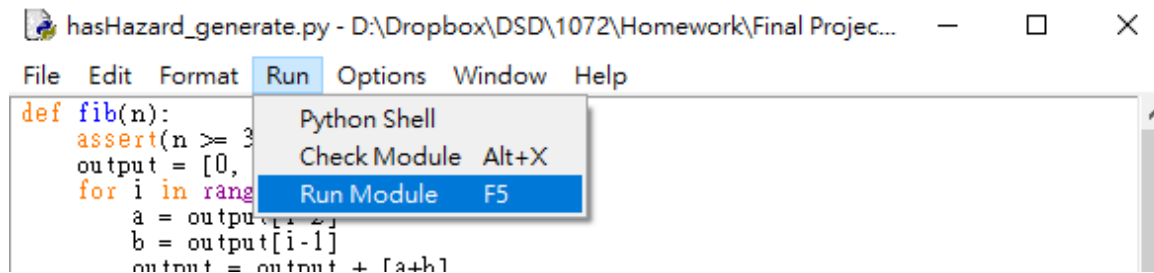
Modify and Run

- Change parameters (This case: nb = 16)



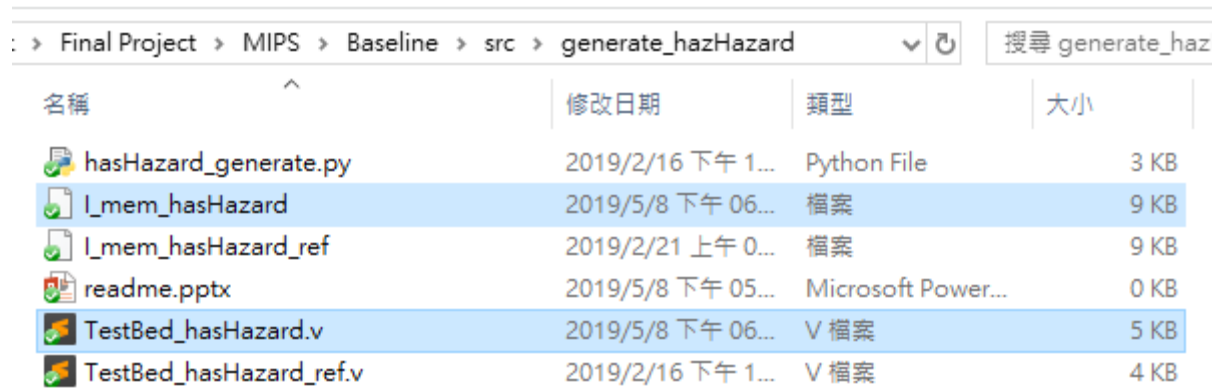




```
def fib(n):  
    assert(n >= 3)  
    output = [0, 1]  
    for i in range(2,n):  
        a = output[i-2]  
        b = output[i-1]  
        output = output + [a+b]  
    return output  
  
# Modify number of sequence here  
# Note: nb >= 3 && nb <= 47 (if nb >= 48, there will be overflow)  
nb = 16
```

- Run Module



Simulation

- New files (testbench and pattern) are constructed

: > Final Project > MIPS > Baseline > src > generate_hazHazard				搜尋 generate_haz
名稱	修改日期	類型	大小	
 hasHazard_generate.py	2019/2/16 下午 1...	Python File	3 KB	
 l_mem_hasHazard	2019/5/8 下午 06...	檔案	9 KB	
 l_mem_hasHazard_ref	2019/2/21 上午 0...	檔案	9 KB	
 readme.pptx	2019/5/8 下午 05...	Microsoft Power...	0 KB	
 TestBed_hasHazard.v	2019/5/8 下午 06...	V 檔案	5 KB	
 TestBed_hasHazard_ref.v	2019/2/16 下午 1...	V 檔案	4 KB	

- Run your Verilog simulation
- Have fun!