How to Use Generate?

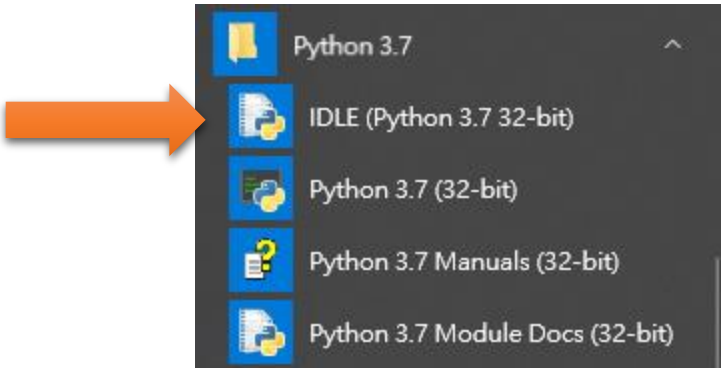
Example: hasHazard_generate.py

The Simplest Way: Python IDLE

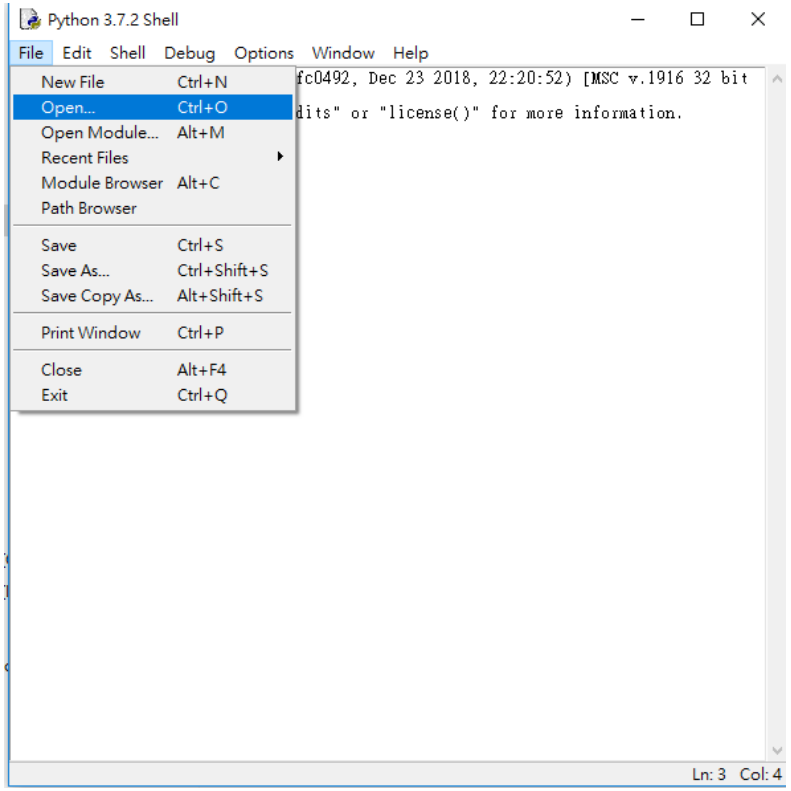
- Download Python first (latest preferred)
  - https://www.python.org/downloads/

Open File: Method 1

- Choose IDLE

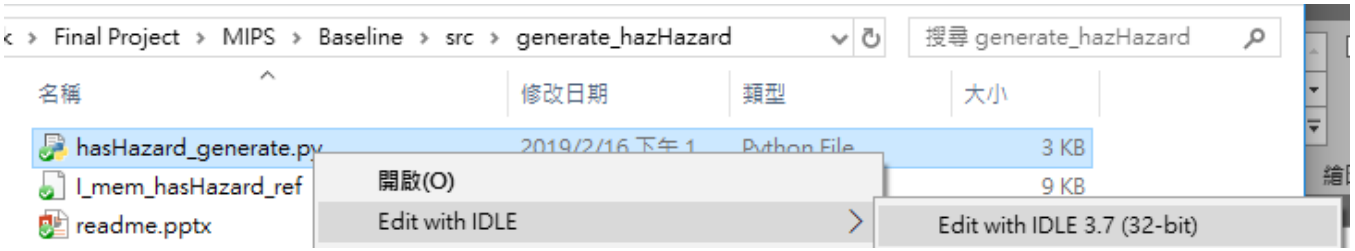


- File → Open…



Open File: Method 2

- Right click the file
- Ex: hasHazard_generate.py



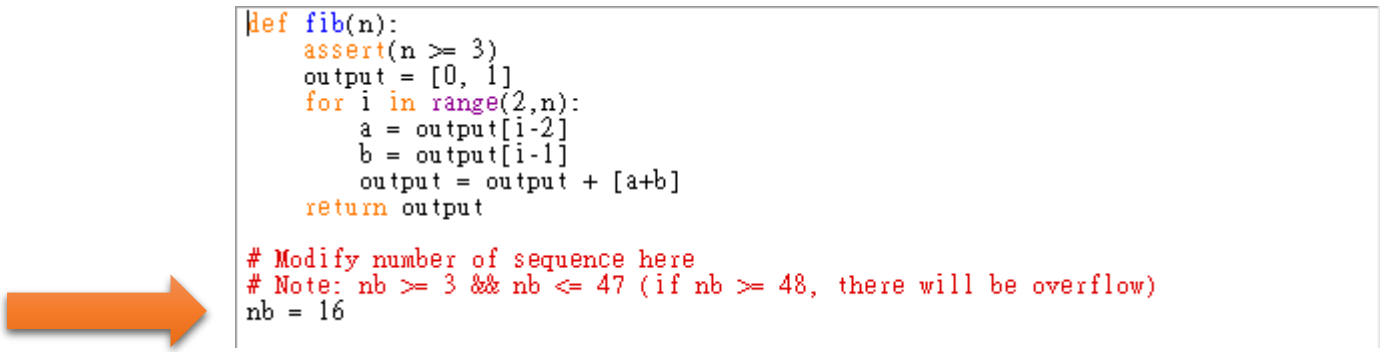
- And you will see the code:

```
def fib(n):
    assert(n >= 3)
    output = [0, 1]
    for i in range(2,n):
        a = output[i-2]
        b = output[i-1]
        output = output + [a+b]
    return output

# Modify number of sequence here
# Note: nb >= 3 && nb <= 47 (if nb >= 48, there will be overflow)
nb = 16
```

Modify and Run

- Change parameters (This case: nb = 16)



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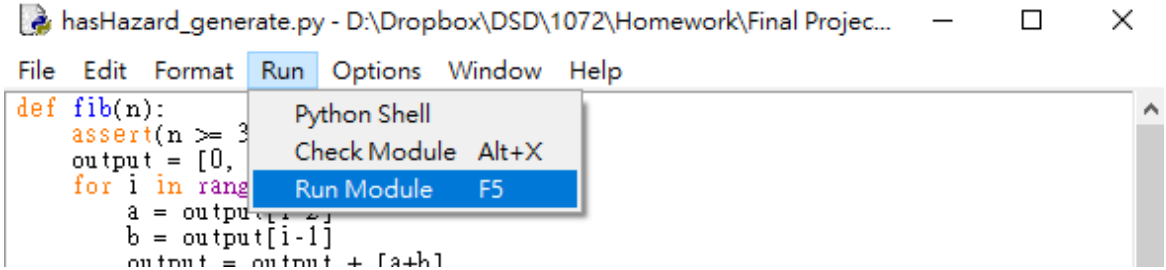
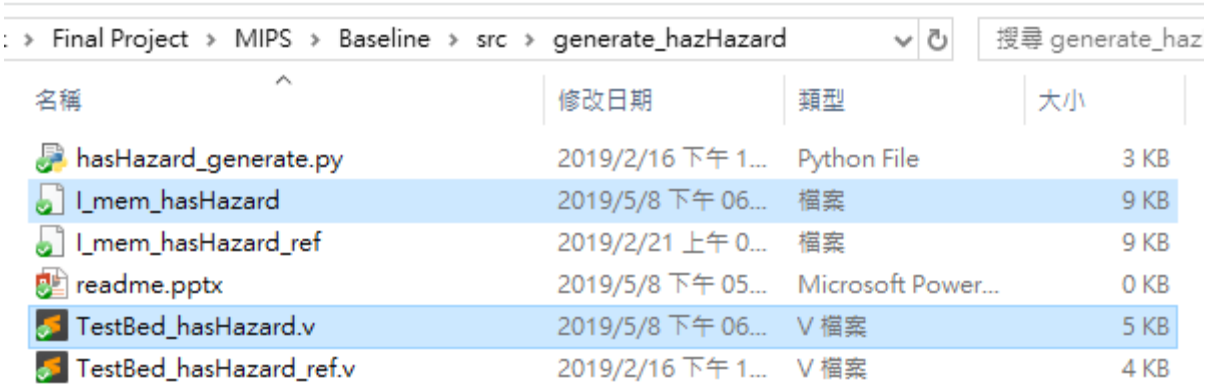
- Run Module



Simulation

- New files (testbench and pattern) are constructed



- Run your Verilog simulation
- Have fun!