Dedicated Pin	100-Pin TQFP	100-Pin FBGA	100-Pin MBGA	144-Pin TQFP	256-Pin FBGA	256-Pin MBGA
IO/GCLK0	12	E2	F2	18	H5	K1
IO/GCLK1	14	E1	E1	20	J5	L1
IO/GCLK2	62	F8	F10	89	J12	M20
IO/GCLK3	64	E10	G11	91	H12	L20
IO/DEV_OE	43	J7	L8	60	M8	W12
IO/DEV_CLRn	44	K9	K8	61	M9	Y13
TDI	23	H2	J2	34	L6	U2
TMS	22	J1	J1	33	N4	T3
TCK	24	H3	K1	35	P3	W2
TDO	25	J2	K2	36	M5	V2
GNDINT	11, 37, 65, 90	F5, H5, E6, C5	G4, J5, E8, C5	17, 54, 92, 128	H7, H9, J8, J10	J4, U12, M17, D12
GNDIO	10, 32, 46, 60, 79, 93	E5, G5, G7, F6, D7, D5	E4, H5, H7, G8, D7, D5	10, 26, 47, 65, 83, 99, 115, 135	A1, A16, B2, B15, G7, G8, G9, G10, K7, K8, K9, K10, R2, R15, T1, T16	H3, J3, M4, N3, U9, V8, V9, V13, H18, J17, N18, C8, D9, C12, C13, M18
VCCINT (1)	13, 39, 63, 88	F4, H6, E7, C6	G3, J7, E9, C7	19, 56, 90, 126	H8, H10, J7, J9	K4, U11, L17, D11
VCCIO1 (2)	9, 31, 45	E4, G4, G6	E3, J4, J8	9, 25, 46, 64	C1, H6, J6, P1, T3, L8, L9, T14	K3, L3, L4, M3, U10, V10, V11, V12
VCCIO2 (2)	59, 80, 94	F7, D6, D4	G9, C8, C4	82, 100, 116, 136	P16, J11, H11, C16, A14, F9, F8, A3	J18, K17, K18, L18, C9, C10, D10, C11,
No Connect (N.C.)	-	-	-	-	D6, D7, D8, D9, D10, E5, E6, E7, E8, E9, E10, E11, E12, F4, F5, F6, F7, F10, F11, F12, G4, G5, G6, G11, G12, G13, H4, H13, J4, J13, K4, K5, K6, K11, K12, K13, L5, L7, L10, L11, L12, M6, M7, M10, M11, M12, N6, N7, N8, N9, N10, N11	D5, C7, D8, D14, C14, C4, D6, C6, B10, B11, D16, D15, F18, D4, H4, G4, D7, D13, G17, D17, E4, G3, F4, H17, G18, F17, K2, K19, L2, L19, R4, P4, N4, N17, P18, R17, P3, U8, U16, T17, P17, U6, U7, U13, U14, U15, U5, V7, W9, W10, V15, V14
Total User I/O Pins	76	76	76	116	160	160

Notes:
1. For EPM570 devices, all VCCINT pins must be connected to either 3.3 V or 2.5 V, but not a combination of both.
   For EPM570G devices, all VCCINT pins must be connected to 1.8 V.
2. Each set of VCCIO pins (VCCIO1 or VCCIO2) can be connected to 3.3 V, 2.5 V, 1.8 V, or 1.5 V.

Bank Number	Pad Number Orientation	Pin/Pad Function	Optional Function(s)	100-Pin TQFP	100-Pin FBGA	100-Pin MBGA	144-Pin TQFP	256-Pin FBGA	256-Pin MBGA
B1	0	VCCIO1							
B1	1	GNDIO							
B1	2	IO						C3	D3
B1	3	IO					1	C2	C2
B1	4	IO		2	C2	B1	2	D3	E3
B1	5	IO						D1	C1
B1	6	IO		3	B1	C2	3	D2	D2
B1	7	IO						E1	D1
B1	8	IO		4	C1	C1	4	E4	C3
B1	9	IO						F2	F2
B1	10	IO		5	D3	D3	5	E3	H2
B1	11	IO		6	D2	D2	6	F1	E1
B1	12	IO		7	D1	D1	7	E2	B1
B1	13	IO		8	E3	E2	8	G2	G2
B1	14	IO						F3	F3
B1	15	IO						G1	E2
B1	16	VCCIO1							
B1	17	GNDIO							
B1	18	IO					11	G3	J2
B1	19	IO					12	H2	G1
B1	20	IO					13	H3	F1
B1	21	IO					14	H1	H1
B1	22	IO					15	J3	M2
B1	23	IO					16	J1	J1
	24	GNDINT							
B1	25	IO	GCLK0	12	E2	F2	18	H5	K1
	26	VCCINT							
B1	27	IO	GCLK1	14	E1	E1	20	J5	L1
B1	28	IO		15	F2	F1	21	K3	N2
B1	29	IO		16	F3	G1	22	J2	M1
B1	30	IO		17	F1	G2	23	L3	T4
B1	31	IO		18	G1	F3	24	K1	N1
B1	32	VCCIO1							
B1	33	GNDIO							
B1	34	IO						L4	R3
B1	35	IO					27	K2	P1
B1	36	IO						M2	U1
B1	37	IO					28	L1	R1
B1	38	IO					29	M3	R2
B1	39	IO						L2	P2
B1	40	IO		19	H1	H1	30	M4	V3
B1	41	IO						M1	T1
B1	42	IO		20	G2	H3	31	N2	W1

Bank Number	Pad Number Orientation	Pin/Pad Function	Optional Function(s)	100-Pin TQFP	100-Pin FBGA	100-Pin MBGA	144-Pin TQFP	256-Pin FBGA	256-Pin MBGA
B1	43	IO						N1	V1
B1	44	IO		21	G3	H2	32	N3	T2
B1	45	IO						P2	U3
B1	46	TMS		22	J1	J1	33	N4	T3
B1	47	TDI		23	H2	J2	34	L6	U2
B1	48	TCK		24	H3	K1	35	P3	W2
B1	49	TDO		25	J2	K2	36	M5	V2
B1	50	VCCIO1							
B1	51	GNDIO							
B1	52	N.C. (1)							
B1	53	IO					37	R3	W4
B1	54	IO					38	R1	W3
B1	55	IO						P4	V4
B1	56	IO					39	T2	Y1
B1	57	IO						R4	Y2
B1	58	IO		26	K1	L1	40	T4	W6
B1	59	IO		27	J3	L2	41	N5	W5
B1	60	IO						T5	Y4
B1	61	IO		28	K2	K3	42	P5	V5
B1	62	IO		29	K3	L3	43	R6	W7
B1	63	IO		30	H4	K4	44	R5	Y3
B1	64	IO						T6	Y5
B1	65	IO						P6	U4
B1	66	IO					45	R7	Y6
B1	67	VCCIO1							
B1	68	GNDIO							
B1	69	IO					48	P7	V6
B1	70	IO					49	T7	Y7
B1	71	IO		33	J4	L4	50	P8	W8
B1	72	IO		34	K4	K5	51	R8	Y8
B1	73	IO		35	J5	L5	52	P9	W11
B1	74	IO		36	K5	L6	53	T8	Y9
	75	GNDINT							
B1	76	IO		38	K6	K6	55	T9	Y10
	77	VCCINT							
B1	78	IO		40	J6	J6	57	R9	Y11
B1	79	IO		41	K7	L7	58	P10	W14
B1	80	IO		42	K8	K7	59	T10	Y12
B1	81	IO	DEV_OE	43	J7	L8	60	M8	W12
B1	82	IO	DEV_CLRn	44	K9	K8	61	M9	Y13
B1	83	IO					62	P11	W13
B1	84	IO					63	R10	Y14
B1	85	VCCIO1							

Bank Number	Pad Number Orientation	Pin/Pad Function	Optional Function(s)	100-Pin TQFP	100-Pin FBGA	100-Pin MBGA	144-Pin TQFP	256-Pin FBGA	256-Pin MBGA
B1	86	GNDIO							
B1	87	IO						R12	W16
B1	88	IO		47	H7	L9	66	T11	Y15
B1	89	IO		48	J8	K9	67	P12	V17
B1	90	IO		49	H8	L10	68	R11	Y16
B1	91	IO						N12	V16
B1	92	IO		50	K10	K10	69	T12	W15
B1	93	VCCIO1							
B1	94	GNDIO							
B1	95	IO					70	R13	Y18
B1	96	IO						T13	Y17
B1	97	IO						P13	V18
B1	98	IO		51	J9	L11	71	T15	W17
B1	99	IO						R14	Y19
B1	100	IO					72	R16	W18
B1	101	VCCIO1							
B1	102	GNDIO							
B2	103	VCCIO2							
B2	104	GNDIO							
B2	105	IO					73	P14	W19
B2	106	IO		52	H9	K11	74	N15	Y20
B2	107	IO		53	J10	J10	75	P15	V19
B2	108	IO						N16	T19
B2	109	IO		54	H10	J11	76	N13	U18
B2	110	IO						M15	V20
B2	111	IO						N14	U19
B2	112	IO		55	G8	H9	77	M16	R19
B2	113	IO						M13	R18
B2	114	IO		56	G9	H10	78	L15	U20
B2	115	IO		57	G10	H11	79	M14	T18
B2	116	IO		58	F10	G10	80	L16	T20
B2	117	IO					81	L13	U17
B2	118	IO						K15	P19
B2	119	VCCIO2							
B2	120	GNDIO							
B2	121	IO					84	L14	W20
B2	122	IO					85	K16	R20
B2	123	IO		61	F9	F9	86	K14	N19
B2	124	IO					87	J15	P20
B2	125	IO					88	J14	M19
B2	126	IO	GCLK2	62	F8	F10	89	J12	M20
	127	VCCINT							
B2	128	IO	GCLK3	64	E10	G11	91	H12	L20

Bank Number	Pad Number Orientation	Pin/Pad Function	Optional Function(s)	100-Pin TQFP	100-Pin FBGA	100-Pin MBGA	144-Pin TQFP	256-Pin FBGA	256-Pin MBGA
	129	GNDINT							
B2	130	IO		66	E9	F11	93	J16	N20
B2	131	IO		67	E8	E11	94	H14	J19
B2	132	IO		68	D10	E10	95	H16	K20
B2	133	IO					96	G14	E17
B2	134	IO					97	H15	J20
B2	135	IO					98	F14	H19
B2	136	GNDIO							
B2	137	VCCIO2							
B2	138	IO					101	G16	H20
B2	139	IO						F13	C18
B2	140	IO		69	C10	D9	102	G15	G20
B2	141	IO		70	D9	D11	103	E14	D18
B2	142	IO						F16	G19
B2	143	IO						E13	E18
B2	144	IO		71	D8	D10	104	F15	F20
B2	145	IO		72	B10	C11	105	D14	B20
B2	146	IO						E16	E20
B2	147	IO		73	C9	C10	106	D13	C19
B2	148	IO						E15	F19
B2	149	IO		74	C8	B11	107	C15	E19
B2	150	IO						D16	D20
B2	151	IO		75	B9	B10	108	C14	D19
B2	152	IO						D15	C20
B2	153	N.C. *(1)*							
B2	154	VCCIO2							
B2	155	GNDIO							
B2	156	IO						B14	A19
B2	157	IO		76	A10	A11	109	B16	A20
B2	158	IO		77	A9	A10	110	C13	C16
B2	159	IO		78	B8	B9	111	A15	B17
B2	160	IO						B13	A18
B2	161	IO					112	A13	A17
B2	162	IO						C12	B16
B2	163	IO					113	B12	B15
B2	164	IO						D12	C15
B2	165	IO					114	A12	B14
B2	166	IO						C11	B18
B2	167	GNDIO							
B2	168	VCCIO2							
B2	169	IO		81	A8	A9	117	B11	A16
B2	170	IO		82	C7	B8	118	D11	B19
B2	171	IO					119	A11	B13

Bank Number	Pad Number Orientation	Pin/Pad Function	Optional Function(s)	100-Pin TQFP	100-Pin FBGA	100-Pin MBGA	144-Pin TQFP	256-Pin FBGA	256-Pin MBGA
B2	172	IO					120	C10	C17
B2	173	IO		83	B7	A8	121	B10	A15
B2	174	IO		84	A7	B7	122	C9	B12
B2	175	IO		85	A6	A7	123	A10	A14
B2	176	IO		86	B6	C6	124	C8	B9
B2	177	IO		87	A5	B6	125	B9	A13
	178	VCCINT							
B2	179	IO		89	B5	A6	127	A9	A12
	180	GNDINT							
B2	181	IO					129	A8	A11
B2	182	IO					130	C7	B8
B2	183	IO					131	B8	A10
B2	184	IO					132	C6	B2
B2	185	IO		91	A4	A5	133	A7	A9
B2	186	IO		92	B4	B5	134	B5	A5
B2	187	GNDIO							
B2	188	VCCIO2							
B2	189	IO		95	C4	A4	137	B7	A8
B2	190	IO		96	A3	B4	138	C5	B3
B2	191	IO		97	A2	A3	139	A6	A7
B2	192	IO						D5	C5
B2	193	IO		98	B3	B3	140	B6	B7
B2	194	IO		99	C3	A2	141	B4	B6
B2	195	IO						A5	A6
B2	196	IO		100	A1	B2	142	C4	A3
B2	197	GNDIO							
B2	198	VCCIO2							
B2	199	IO						A4	A4
B2	200	IO						D4	B4
B2	201	IO		1	B2	A1	143	A2	B5
B2	202	IO						B3	A2
B2	203	IO					144	B1	A1
B2	204	VCCIO2							
B2	205	GNDIO							

Note:

1. No Connect

Pin Name	Pin Type	Pin Description
		Supply and Reference pins
VCCIO[1..2]	Power	I/O supply voltage pins for banks 1 through 2. Each VCCIO bank supports a different voltage level with the VCCIO pins providing power for the input and output buffers within that particular I/O bank. Each VCCIO bank can be powered with either 3.3 V, 2.5 V, 1.8 V, or 1.5 V.
GNDIO	Ground	Ground pins for all the I/O banks.
VCCINT	Power	Voltage supply pins for the device.
GNDINT	Ground	Ground pins for the internal supply.
NC	No Connect	Do not drive signals into these pins.
		Programming and JTAG pins
DEV_CLRn	I/O	Dual-purpose pin that can override all clears on all device registers. All registers are cleared when the pin is driven low and all registers behave as defined in the design when this pin is driven high. If not used for its dual-purpose function, this pin is a regular I/O.
DEV_OE	I/O	Dual-purpose pin that can override all tri-states on the device. All output pins are tri-stated when the pin is driven low and all output pins behave as defined in the design when this pin is driven high. If not used for its dual-purpose function, this pin is a regular I/O.
TCK	Input	Dedicated JTAG input pin.
TDI	Input	Dedicated JTAG input pin.
TMS	Input	Dedicated JTAG input pin.
TDO	Output	Dedicated JTAG output pin.
		Clock Pins
GCLK [0..3]	I/O	Dual-purpose clock pins that connect to the global clock network. If not used for its dual-purpose function, this pin is a regular I/O.

Figure 1. MAX II EPM570 / EPM570G T100 Device Top View Package Diagram and Bank Information
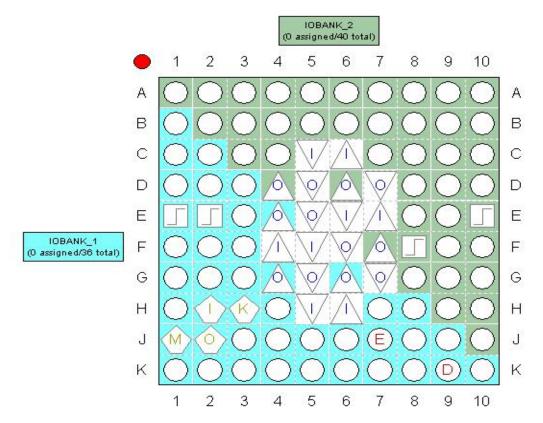
Figure 2. MAX II EPM570 / EPM570G F100 Device Top View Package Diagram and Bank Information
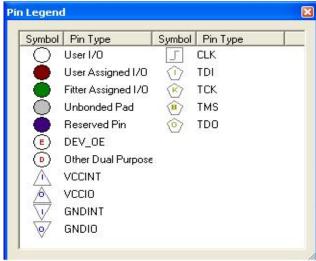
Figure 3. MAX II EPM570 / EPM570G M100 Device Top View Package Diagram and Bank Information
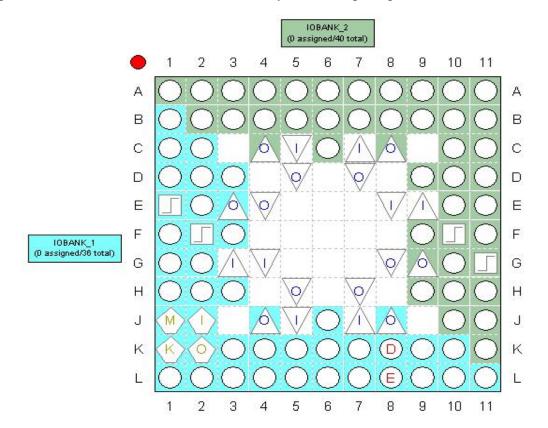
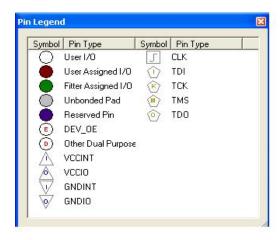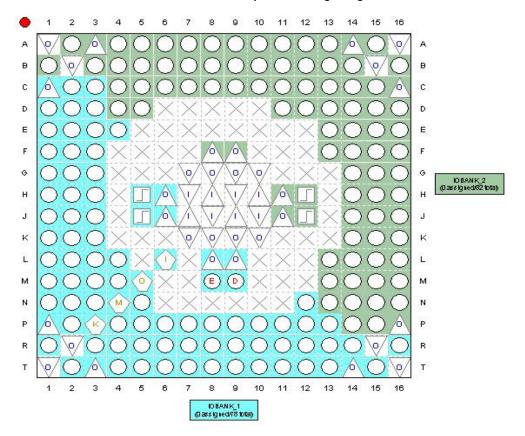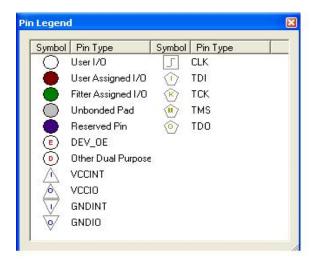*Figure 4. MAX II EPM570 / EPM570G T144 Device Top View Package Diagram and Bank Information*

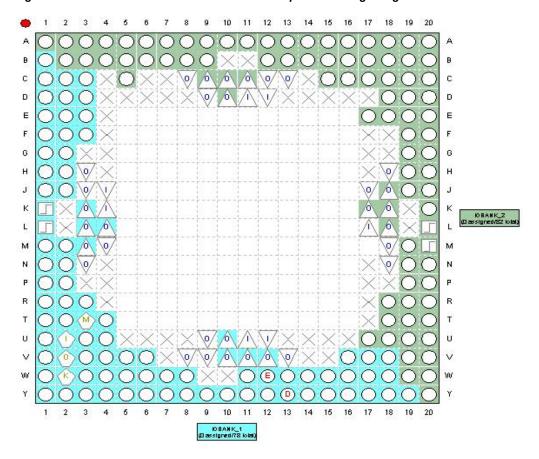*Figure 5. MAX II EPM570 / EPM570G F256 Device Top View Package Diagram and Bank Information*

Figure 6. MAX II EPM570 / EPM570G M256 Device Top View Package Diagram and Bank Information

Date	Version	Changes Made
Sep-07	1.4	Added support for F100, M100, and M256 packages in the EPM570G device
Apr-06	1.3	Added F100, M100, and M256 packages
Jan-05	1.2	Added MAX IIG device naming to titles, notes, and figures
Jul-04	1.1	Added package diagram and bank information figures for each package
May-04	1.0	Initial release