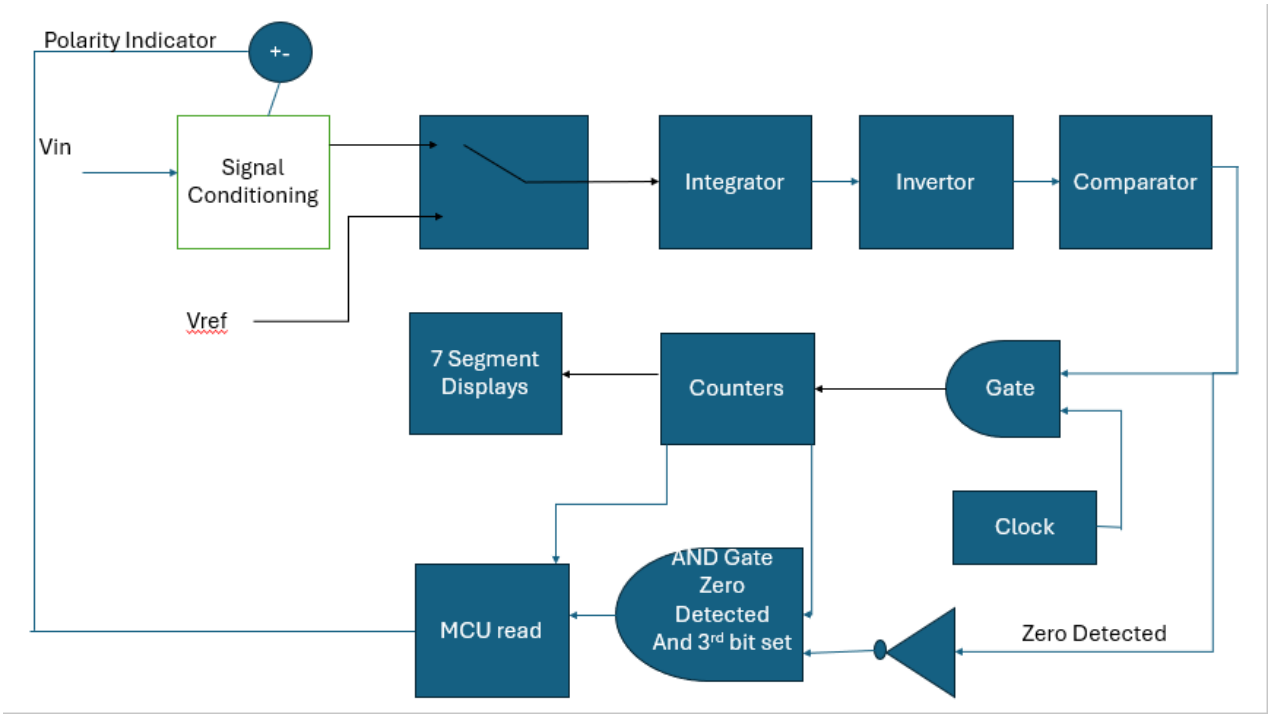
Dual Slope Integrating ADC



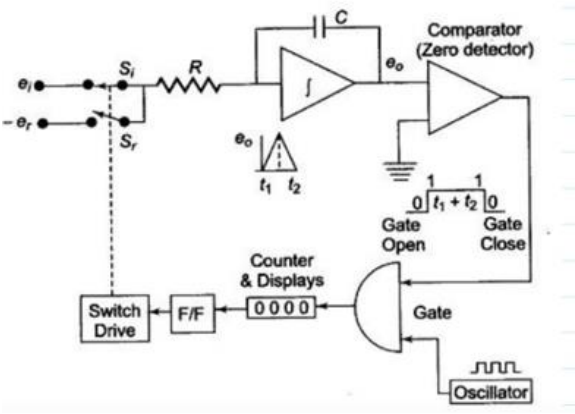
The purpose of this unit will be to perform the dual integration operation. It should also be able to indicate the appropriate polarity and transfer it to the microcontroller digital pin. The microcontroller will receive the appropriate measurement in the form of a count, which it interprets as voltage. It will also make use of 7-segment displays so as to keep track of the counted value for appropriate programmatic calibration. The 7-segment display value will also indicate where there need to be appropriate adjustments to the practical circuit to achieve the correct measurements in case non-ideal effects should arise during construction.

Dual Slope integration operation

Theoretical discussion:

The dual slope integration operation involves the use of an op-amp as an integrator to integrate the input voltage to be read and then subsequently using a reference voltage to infer the unknown input voltage. This second reference voltage is also integrated.

The following figure shows a dual-slope voltmeter:



Integrating a constant DC voltage results in a linear output at the integrate with a slope of magnitude:

$|m| = \frac{1}{RC}$

The output integrator voltage that will result is obtained by the following equation when integrating Vin:

$$V_{out} = \frac{-1}{RC}\int_0^{T1} V_{in}\, dt + Voi = \frac{-V_{in}T1}{RC} + Voi\,,$$

Where Voi is the initial output of the integrator. In most applications, this value is zero.

Now it is assumed that the integrator output is initially zero.

T1 is chosen arbitrarily to be the initial time to integrate the input signal. Once integration has occurred at the fixed time interval T1, the input to the integrator changes to Vref. This results in the integration of the second input signal. Hence, for the second integration, the output at the integrator is obtained by the following equation:

We let Vout from the first integration be V_A. Using the aforementioned equation:

$$V_{out2} = \frac{-1}{RC}\int_0^{T2} V_{ref}\, dt + Voi = \frac{-V_{ref}T2}{RC} + V_A$$

Now, in this case, Vref must be of the opposite polarity to the initial input voltage, and the output voltage must be zero. Hence the following simplified equation is obtained:

$$V_{out2} = \frac{-V_{ref}T2}{RC} + V_A = 0$$

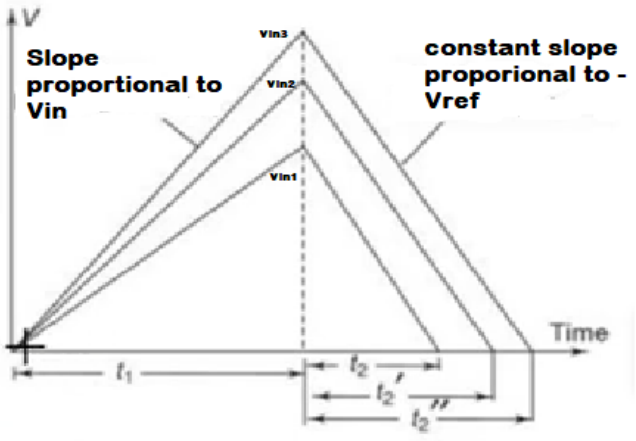
Now to obtain the unknown reference voltage, Vin, the following resultant equation is obtained by manipulation:

$$\frac{-V_{ref}T2}{RC} + \left(\frac{-V_{in}T1}{RC} + Voi\right) = 0,$$

Assuming Voi is zero and substituting results in the following equation:

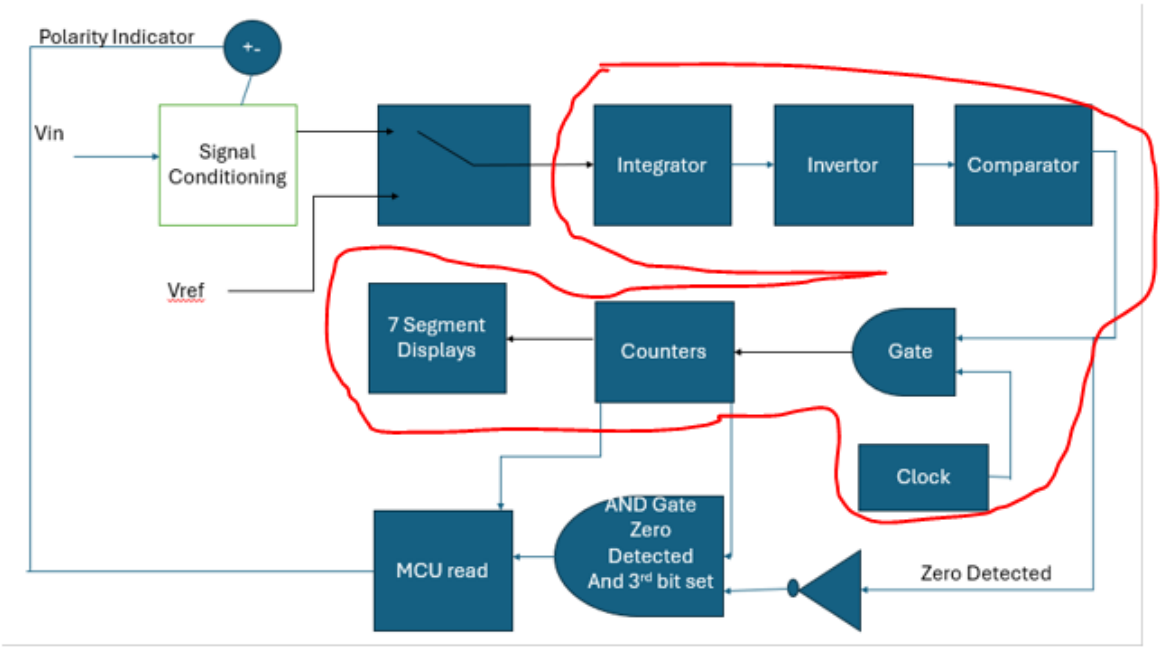
$$V_{in} = \frac{-V_{ref}T2}{T1}$$

An example of the resultant curves for different voltages that may arise from dual slope integration is shown in the following figure:



Noted from the preceding figure is that higher voltages result in a more elevated slope and a longer time T2.

Now instead of graphically solving for the voltage using an oscilloscope or an external instrument, the output of the integrator will be fed into a comparator that is connected to an AND gate and oscillator. The output of this AND gate is then fed into a counter that will count. It is by decoding this count, that the input voltage can be ascertained. This general scheme is shown in the following figure, in which the described configuration is encircled in red:



Designing the system:

As long as the output of the integrator is positive and greater than zero, the comparator will output a high output. In conjunction with the oscillator, it will trigger the counter via the AND gate. We may fix the initial count in the same way that time T1 is fixed.

For the design of this particular system, the time T1 is fixed at 0.8 seconds. The counter must count up to 100 before the Vref is selected for the second integration. Hence, the oscillator clock frequency is computed as follows:

$$Ncounter = \frac{T1}{(1/f_{clock})}$$

Therefore to obtain the appropriate frequency:

$$f_{clock} = \frac{Ncounter}{T1}$$

Substituting the chosen 0.8 seconds and a count of 100 yields an f_{clock} of 125Hz.

Once 100 has been reached, an electronic switch will be triggered to move the pole to Vref. This will cause the counter to count further from 100 until the second integration yields an output of zero. From the obtained final count, the input voltage can then be computed, thus:

$T2 = N_{final\ count} * (\frac{1}{flcock}) - 100 * (\frac{1}{f_{clock}})$,

Where $N_{final\ count}$ is the final count on the timer. This result is then used to solve the equation for Vin thus:

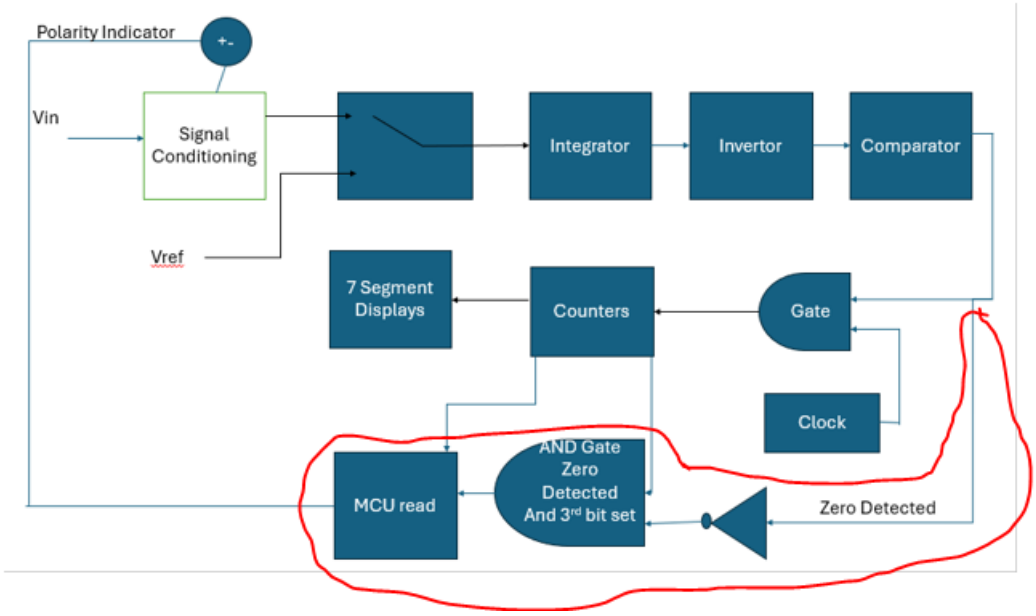
$$V_{in} = \frac{-V_{ref}T2}{T1}$$

Such an operation will be performed by the microcontroller unit and displayed accordingly on the GUI. However, the final count will be transferred to the microcontroller once the integration process is complete.

The completion of the integration process requires the fulfilment of 2 conditions:

1. The 3rd digit (the hundreds) unit is high.
2. The comparator picks up a zero at the output.

This is clarified in the block diagram by the section outlined in red:



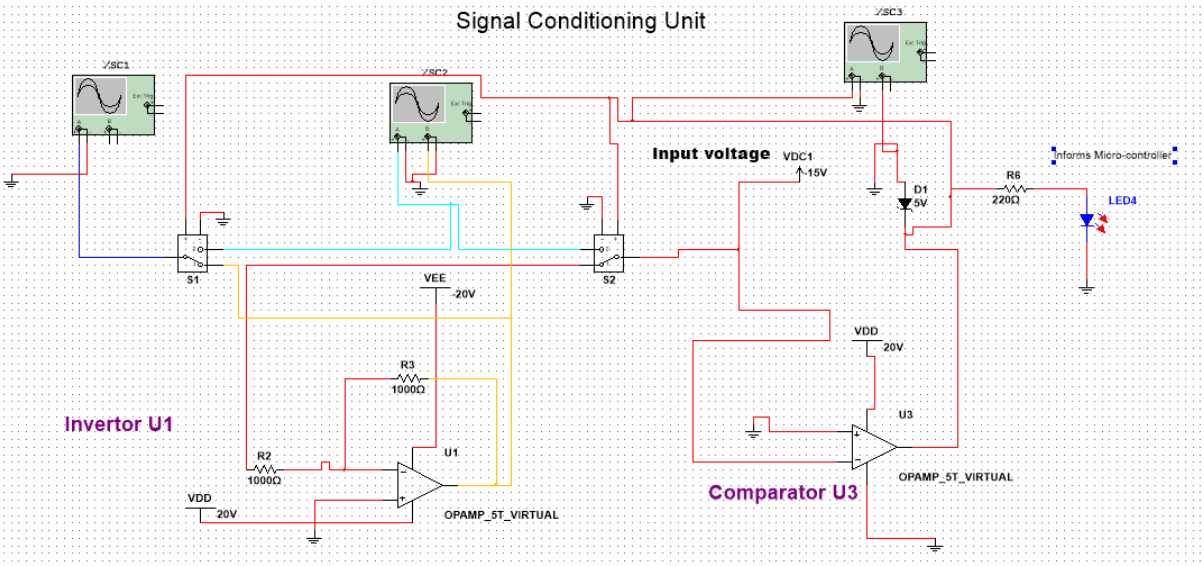
A signal is then sent to the microcontroller to register the final counter via its digital input pins.

Signal conditioning:

Now an important requirement of this design is the capability to measure negative voltages. It has already been stated the Vref is fixed and must have a negative polarity. However, should a negative voltage be detected, Vref and Vin will have the same polarity. Consequently, a signal conditioning block was added to accomplish the following:

1. Invert a negative voltage.
2. Notify the microcontroller that the voltage being read is negative via its input pins.

The following schematic helps to accomplish these stated objectives:



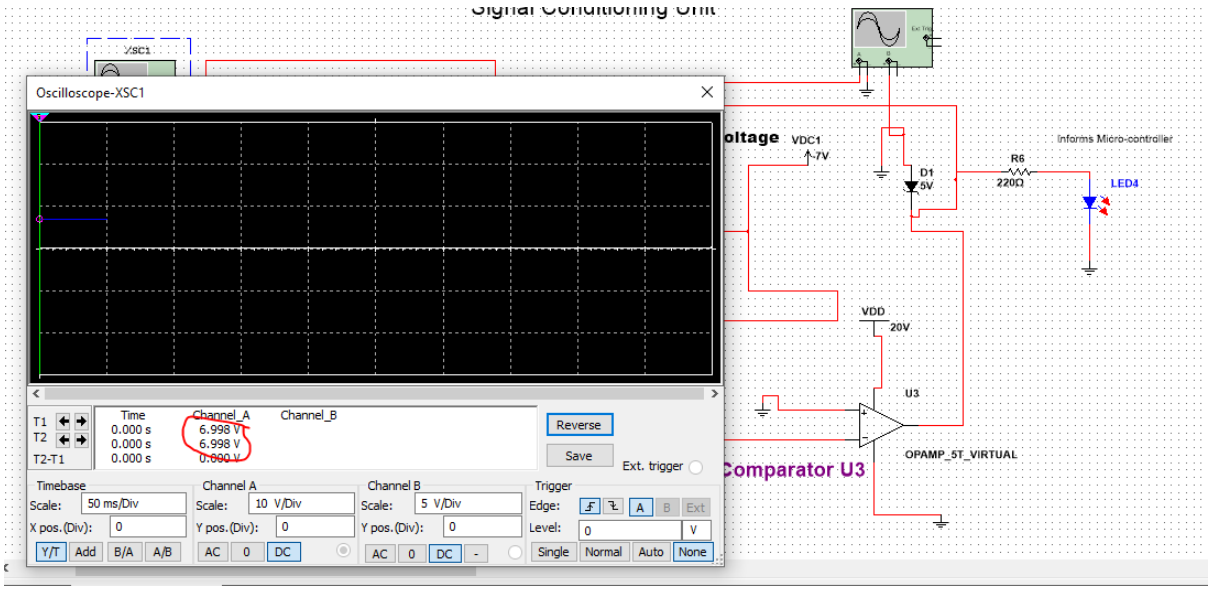
The mechanism is as follows: If the comparator label U3 detects that the input voltage is lower than 0, then it will output a high signal. This signal will then be regulated by Zener diode D1. This regulated signal will:

1. Be sent to the microcontroller to inform it that a negative voltage is being read.
2. Be used to turn on an electronic switch or relay to allow for inversion via the invertor labelled U1.

If, however, the comparator does not detect a negative value, then the electronic switch is not triggered, and no inversion takes place. The input to the microcontroller is also low, indicating that a positive signal is being measured.

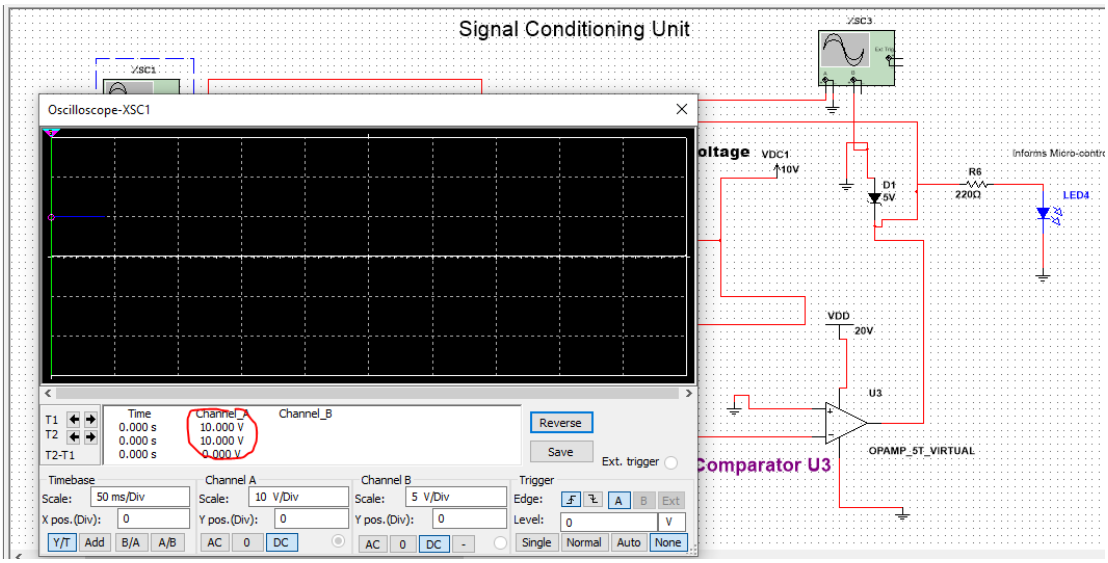
A few simulation results to demonstrate the working of this unit are shown as follows:

Assume initially -7 Volts is being read. The following result is obtained:



The voltage is inverted accordingly, and a high signal is sent to the mcu (shown by the LED4) to indicate a negative value is being read.

For a test voltage of 10 volts:



No inversion takes place, and LED4 is not turned on, indicating an ordinary positive voltage is being read.

The voltage from the signal conditioning unit is now positive and is fed into the integrator as Vin.

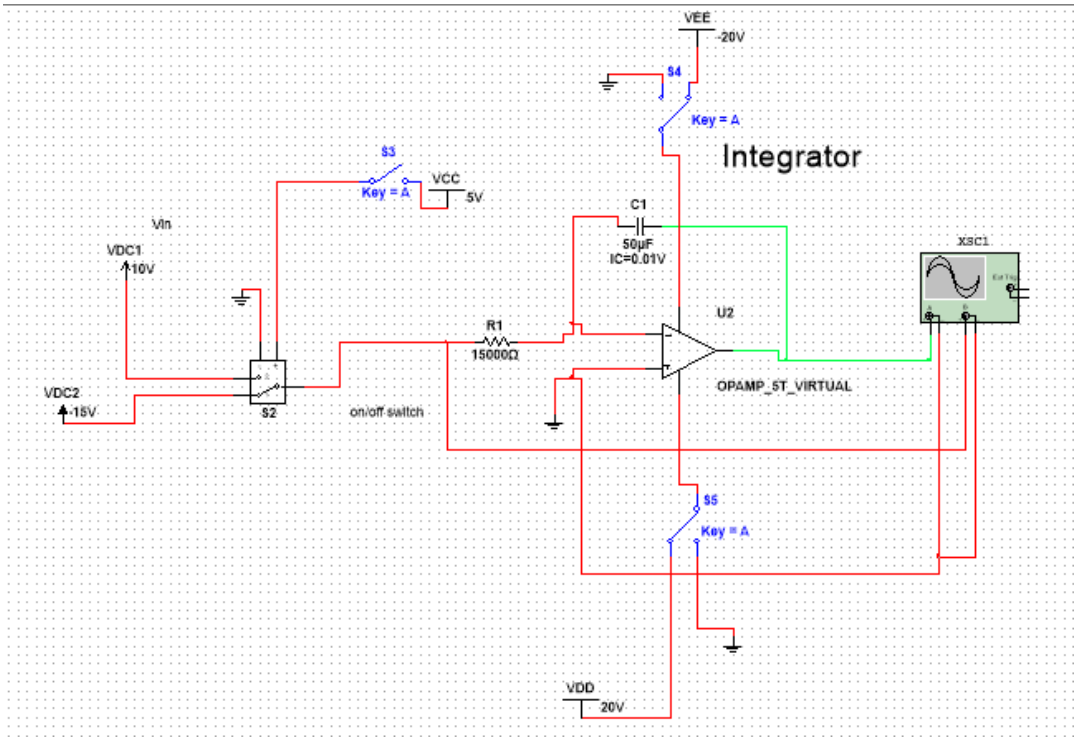
Designing the integrator:

From the established theory, I wish to achieve a maximum integration time of 1 second. That is to say, I want the op-amp to saturate at 1 second to -20V. Therefore, choosing a standard capacitance value of 50 microfarads and a maximum of 15 volts and using the equation:

$$V_{out} = \frac{-1}{RC}\int_0^{T1} V_{in}\,dt = \frac{-V_{in}T1}{RC},$$

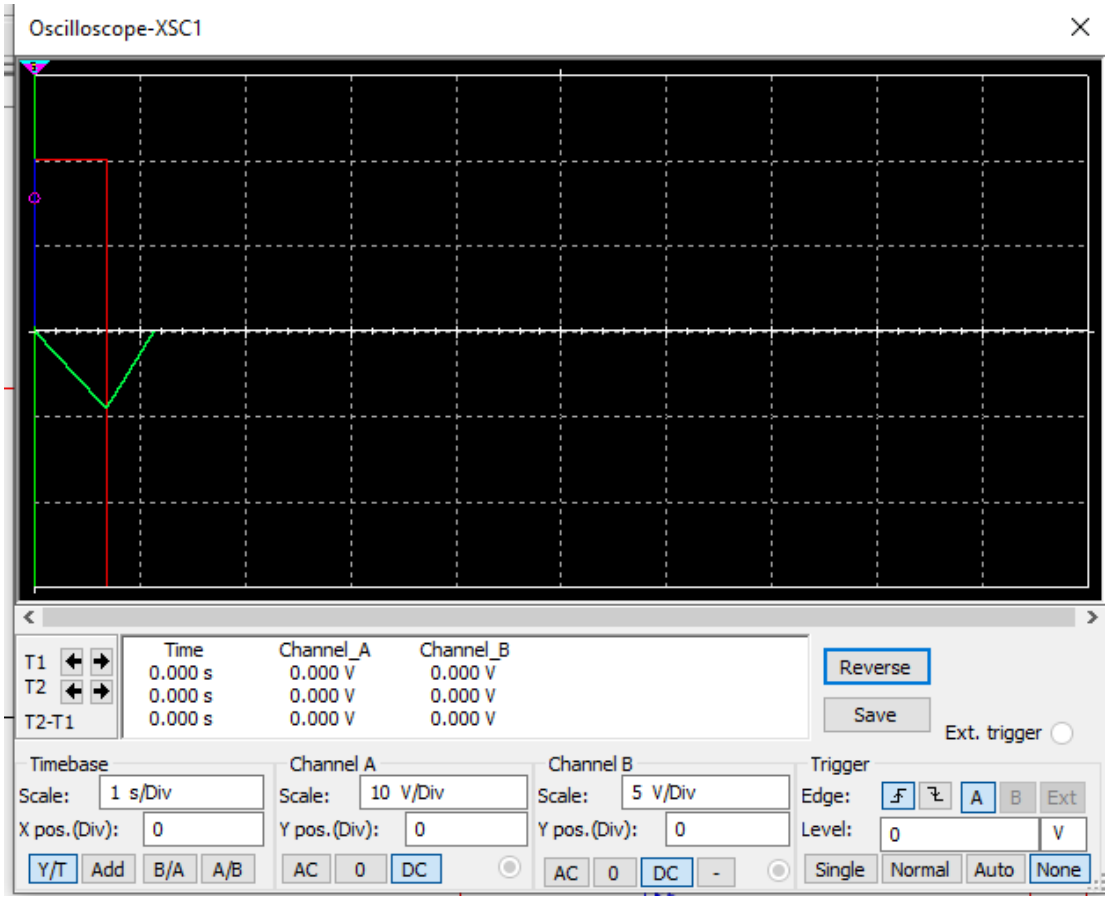
Yields a resistance value of 15 kilo ohms. Of course, I wish to avoid saturation and hence will stop the initial integration at 0.8 seconds instead. This will cause the maximum voltage to be -16V in 0.8 seconds.

The following circuit schematic is provided as a test circuit:



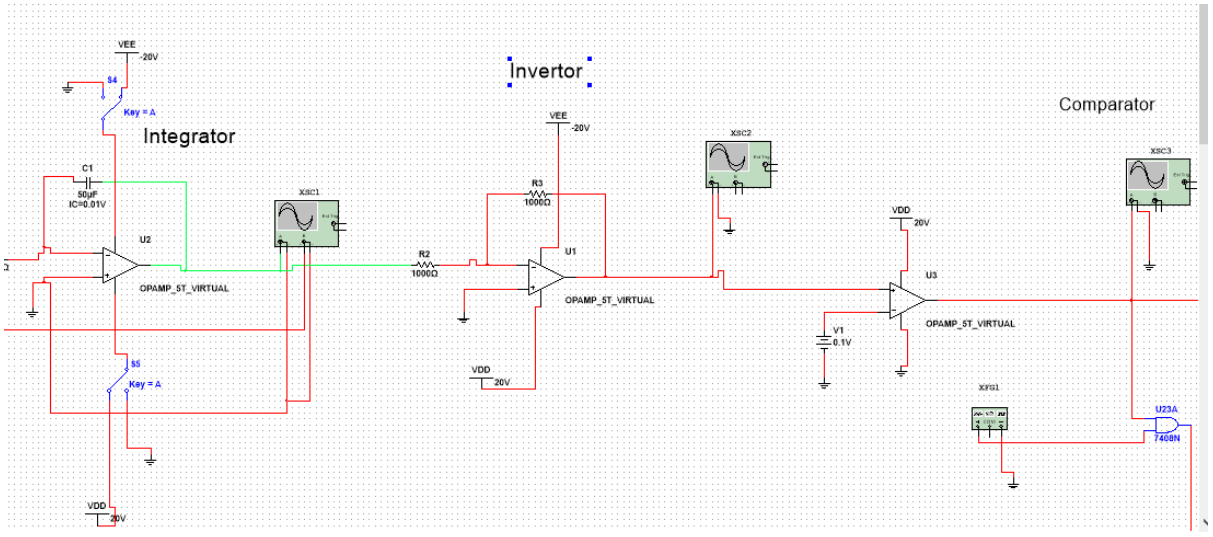
Switch s2 and s3 are used to select between Vref and Vin. Vdc1 in the diagram case is Vin. Vdc2 is the reference voltage, Vref.

When switch s3 is open, VDC1 is chosen, and the first integration takes place. When s3 is closed, the second integration takes place as VDC2, or the reference voltage will be selected. Hence a standard dual integration graph is obtained as shown in the following diagram:



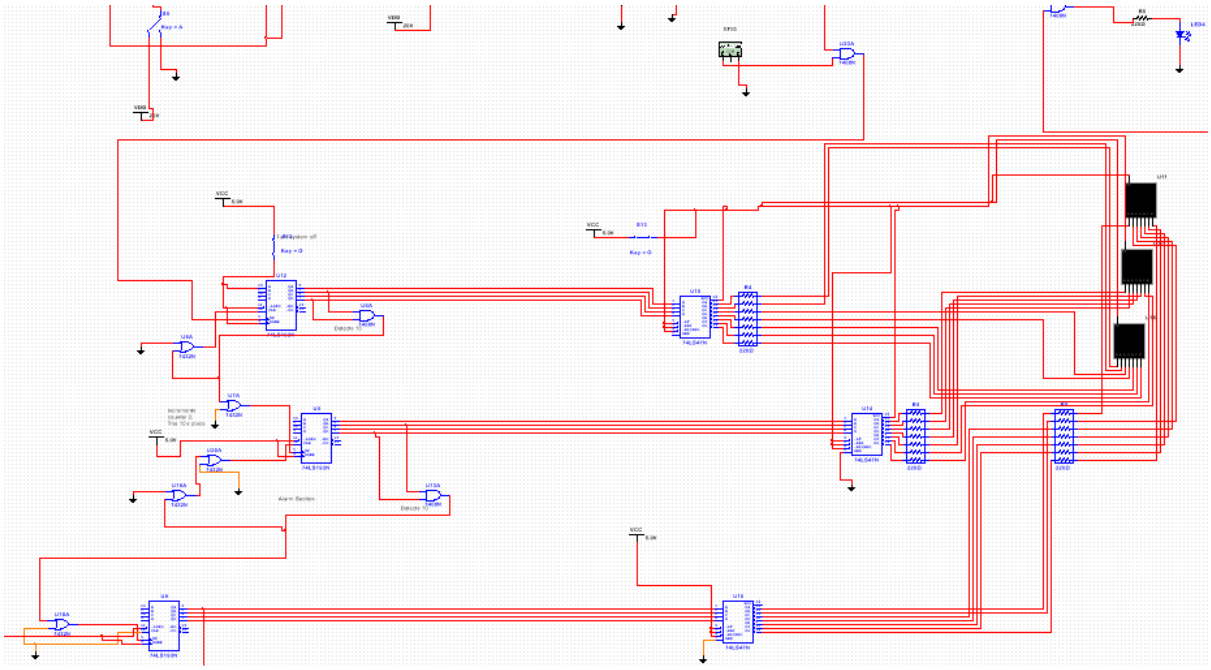
The switch S3 will be controlled by the third digit of the timer. In other words, when the count reaches 100, the third digit becomes 1, closing the switch and triggering the reference voltage accordingly.

It is important to note that the output shown in the figure is negative. To pass it through the comparator, the signal must be inverted. Therefore, an inverter is used, as depicted in the following schematic:

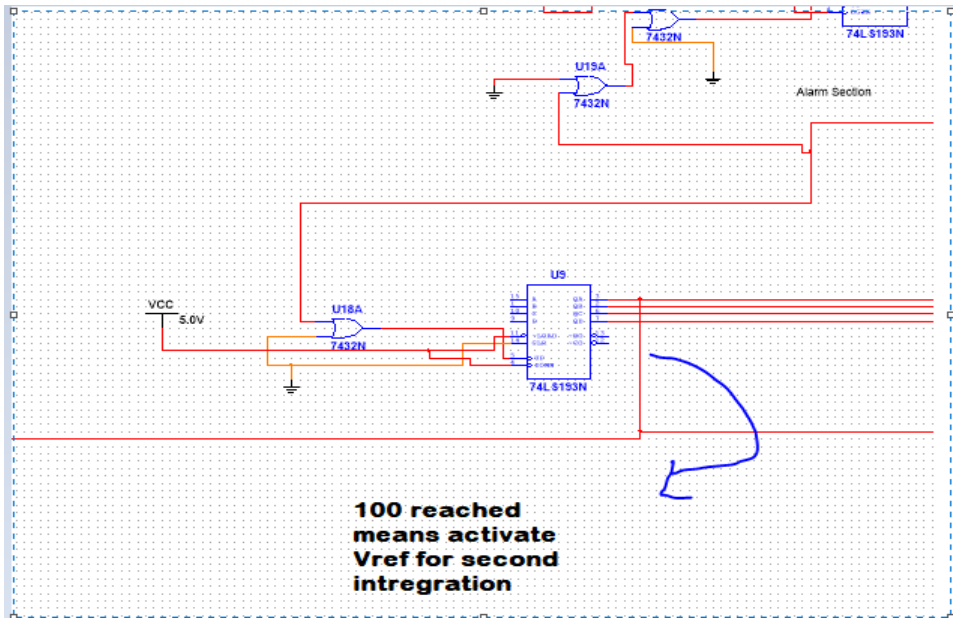


A 125 Hz frequency source is then applied to the input of an AND gate, in conjunction with the comparator output as discussed in the theoretical section.

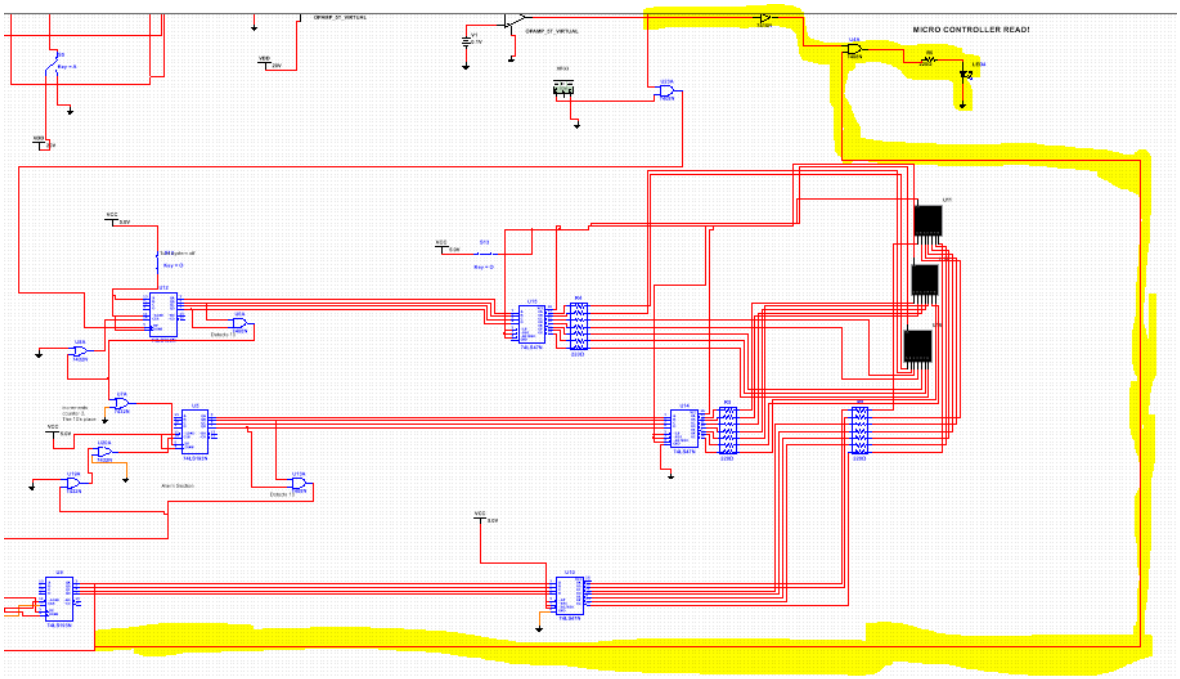
Next, the counter circuitry and 7-segment displays are connected to complete the overall circuit.



There are now three 4-bit counters. The third counter will trigger the switch that selects the reference voltage (Vref) for the second integration. This process is illustrated in the following diagram:

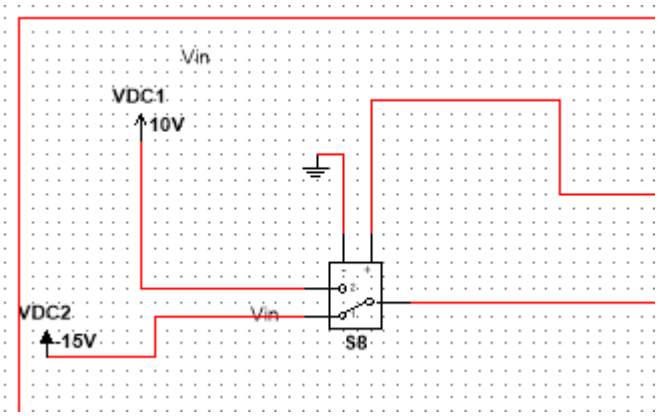


Now to finally indicate to the microcontroller that integration is complete, the 1st bit of the 3rd counter must be high and the comparator must detect zero volts. The following highlighted circuitry implements this idea:

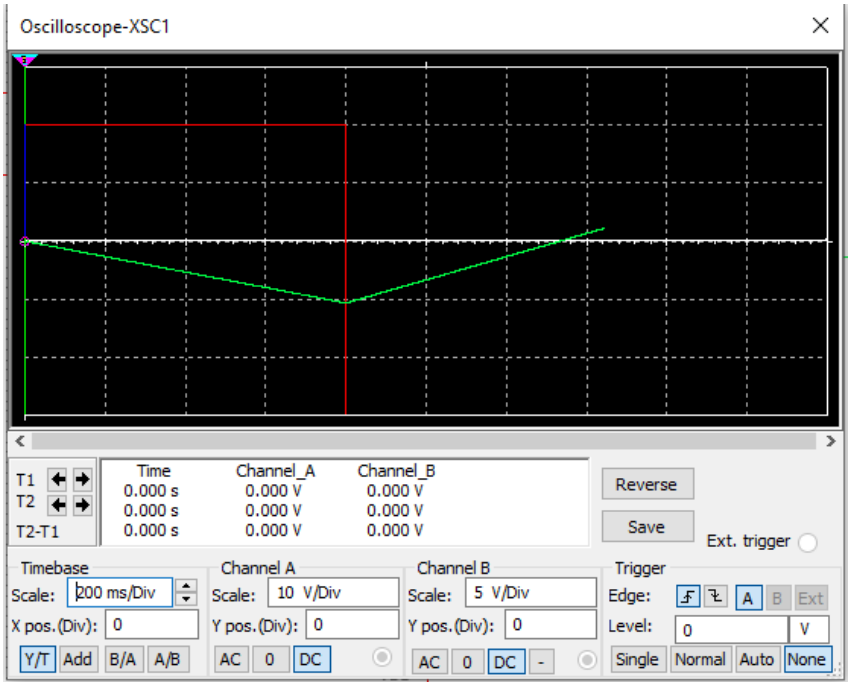


And now for a simulated demonstration of a test input voltage, dual slope plot, and final count:

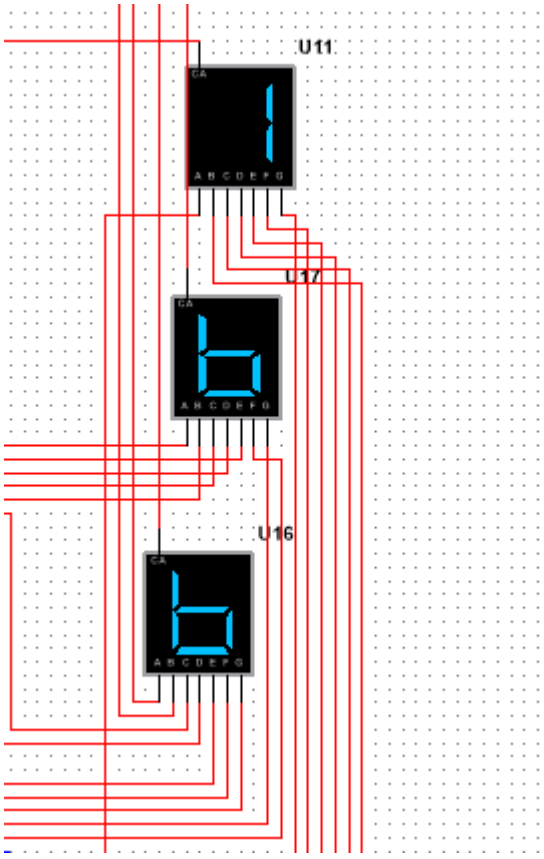
Input voltage of 10 V:



The obtained Dual slope curve after zero has been reached:



The final count on the 7 segment displays is 166:



Using the count to obtain the “unknown” input voltage by substituting into our derived equations:

$$T2 = N_{final\ count} * (\frac{1}{flcock}) - 100 * (\frac{1}{f_{clock}})$$

$T2 = 166 * (\frac{1}{125}) - 100 * (\frac{1}{125})$= 0.528 seconds

Theref0ore

$$V_{in} = \frac{-V_{ref}T2}{T1}$$

$V_{in} = \frac{-(-15)(0.528)}{0.8}$ = 9.9 Volts

The computed voltage from the count is off by 0.1 V. This constitutes an error of 1%. This is reasonably satisfactory, and the small error can mostly likely be attributed to losses and non-ideal effects of the components.

Drawback of Design:

The primary drawback is that the design does not reset automatically after reading. Hence, the system power has to be manually shut down and the capacitor discharged to allow for the reading of a subsequent voltage. The design also seems to require a lot of components. Perhaps a more simplified and innovative approach might be recommended.

Concluding Remarks

The design, although requiring a lot of components, seems to accurately measure the input voltage with a 2% margin of error. It can accomplish the measurement in less than 2 seconds. The design is reasonably thought out but complex and requires a lot of components. This could result in a greater margin of error when implementing the circuit in practice.