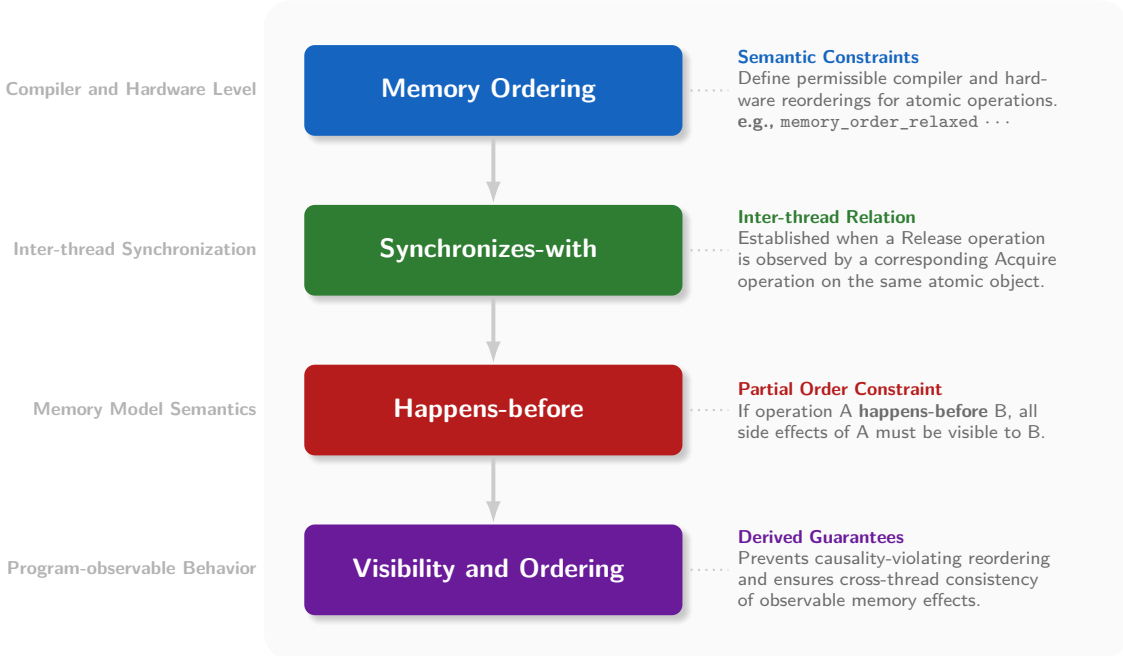
Compiler and Hardware Level
Memory Ordering
Semantic Constraints
Define permissible compiler and hardware reorderings for atomic operations.
e.g., memory_order_relaxed ···
Inter-thread Synchronization
Synchronizes-with
Inter-thread Relation
Established when a Release operation is observed by a corresponding Acquire operation on the same atomic object.
Memory Model Semantics
Happens-before
Partial Order Constraint
If operation A happens-before B, all side effects of A must be visible to B.
Program-observable Behavior
Visibility and Ordering
Derived Guarantees
Prevents causality-violating reordering and ensures cross-thread consistency of observable memory effects.