COMP4300

Lab Exercise One, FA19

Objective

This lab is aimed at getting you familiar with using the ModelSim simulator. The circuits you will be simulating should be familiar to you from ELEC2200.

Instructions

Write a VHDL program consisting of a single entity whose architecture is a single process that implments a full adder. That is, a circuit with the following truth table:

inputs			outputs	
a_in	b_in	carry_in	sum	carry_out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Use exactly the names given above for the signals. Your process should not use the '+' symbol anywhere. All your signals should be of type `bit` (NOT integer).

Deliverables

Please turn in the following things for this lab:

- The file with your VHDL code.
- A screen shot of your exhaustive simulation.
- A screen shot of a successful compilation of your code.

Due Date

Jan 31, 2019, 11:59pm