ISL6236A Project

Variant Name = 5V Variant

Friday, February 23, 2018 V1I1

RELEASED 23-FEB-2018

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DESIGN CONSIDERATION

DESIGN NOTE: Example text for informational design notes.

DESIGN NOTE: Example text for cautionary design notes. DESIGN NOTE: Example text for debug notes.

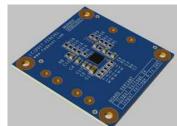
DESIGN NOTE: Example text for critical design notes.

DESIGN NOTE: Example text for critical layout guidelines.

TOP VIEW



BOTTOM VIEW

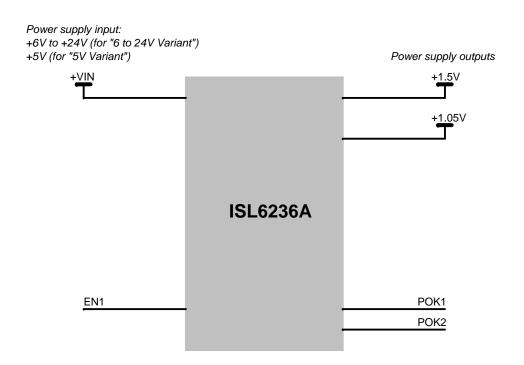




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Title:		Variant:			
ISL6236A Project		<core design=""></core>			
Page:		Checked by:			
01) COVER PAGE		<checked by=""></checked>			
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Custom	LEOA	Robert Feranec	V1I1		

ISL6236A PROJECT (Block Diagram)





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 Title:
 Variant:

 ISL6236A Project
 5V Variant

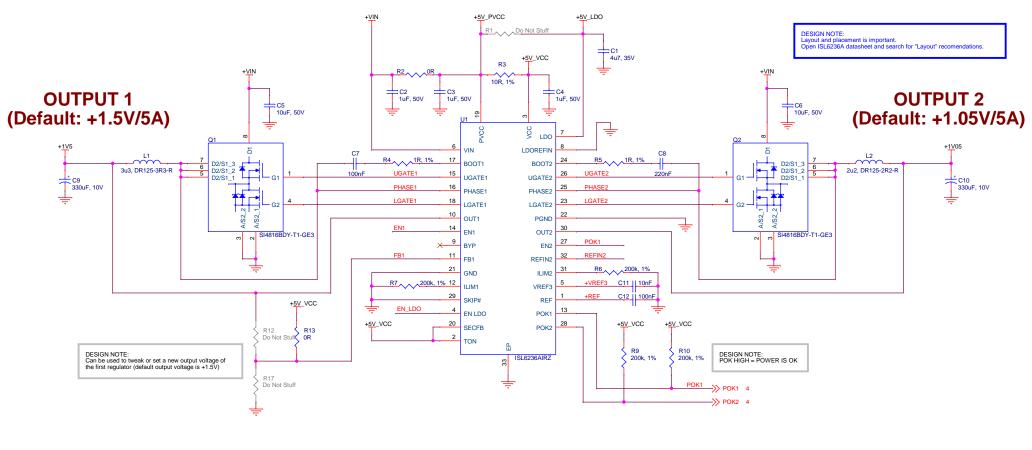
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 02 BLOCK DIAGRAM
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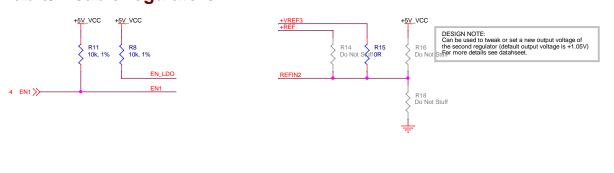
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1.5V / 1.05V POWER SUPPLY



Enable/Disable regulators



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03) +1.5V / +1.05V POWER SUPPLY		<checked by=""></checked>					
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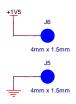
PADS, TESTPOINTS, MECHANICAL

Soldering pads for input and output wires

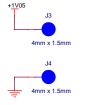
+VIN: Main input power (Default from +6V to +24V)



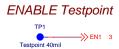
Power supply output 1 (Default +1.5V)



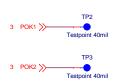
Power supply output 2 (Default +1.05V)



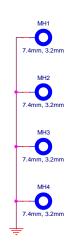
Testpoints



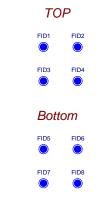
POK Testpoints



Mounting holes



Fiducials



PCB





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Page: 04) PAE	DS,TESTPOINTS, MECHANICAL	Checked by: <checked by=""></checked>					
Size: Custom	Document: LEOA	Designed by: Robert Feranec				Rev: V1I1	
Date:	Wednesday, February 21, 2018	Sheet:	4	of	5		

REVISION HISTORY

01-NOV-2017: Put here a brief info about the change

Detailed description of all the changes - Testing Lite



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Wednesday, February 21, 2018 Sheet: