Universidade Federal do Rio Grande do Norte
Centro de Tecnologia
Departamento de Engenharia Elétrica
ELE0623 - Circuitos para comunicação - 2020.2
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Second laboratory: **S-parameters and Smith chart**

1 Problem 1

The objective of this problem is to work with the Smith chart in the ADS. The line characteristic impedance is considered to be $Z_0 = 50\Omega$

Given $Z = 25 + j30\Omega$, the normalised impedance is: $\frac{Z}{Z_0} = 0.5 + j0.6$, so the reflection coefficient ρ_L can be found considering the point of intersection between the circle 0.5 of constant resistance and the circle 0.6 of constant reactance. So the reflection coefficient a.k.a $S(1,1)$, regarding the S-parameters is: $\rho_L = S(1,1) = -0.149 + j0.46$, according to the figure 1 in the marker *rhoL_1*.

It is also asked to find the impedance for a $rho_L = 0.5 + j0.1$. Once ρ_L is located according to rectangular coordinates in the complex plane, one way to find the impedance is insert the coordinates $(0.5, 0.1)$ in the complex plane of the Smith chart and observe the normalised impedance obtained, therefore $Z_{\rho_L = 0.5 + j0.1} = 2.846 + j0.769$, as seen in the figure 1 in the marker *rhoL_2*.

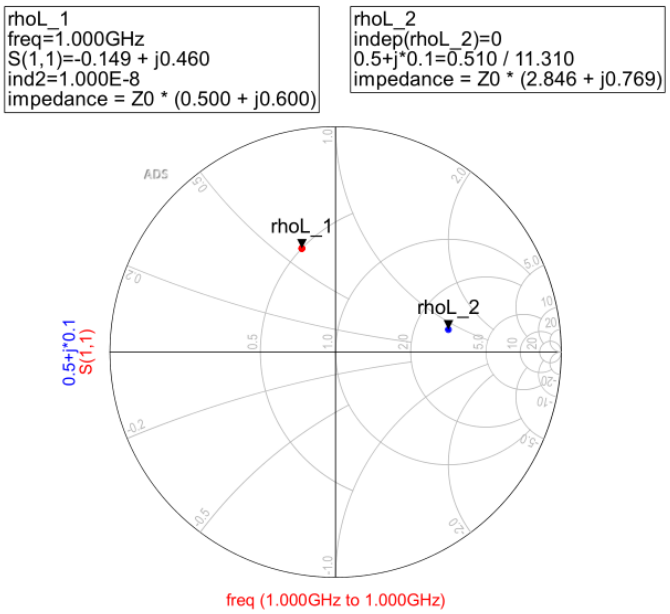


Figure 1: Smith chart for the first half of problem 1.

The second half of the first problem issues the circuits of the figure 2. In both it is asked to use a frequency of $1GHz$ and to sweep the values of reactance.

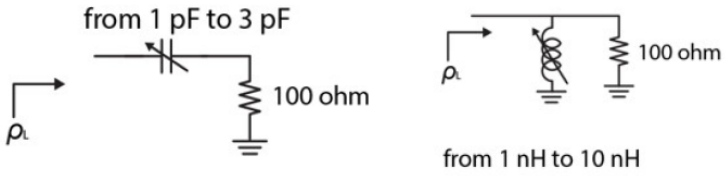


Figure 2: Circuits for problem 1.

The circuit at the left have a capacitor in series with a resistor, when varying the capacitance value, the Smith chart in figure 3 (a) will have the reflection coefficients varying in the circle of constant resistance. The figure 3 (b) show the same circuit for the admittance chart and it is clearly seen that the circuit behaviour is not easily observed by this kind of chart.

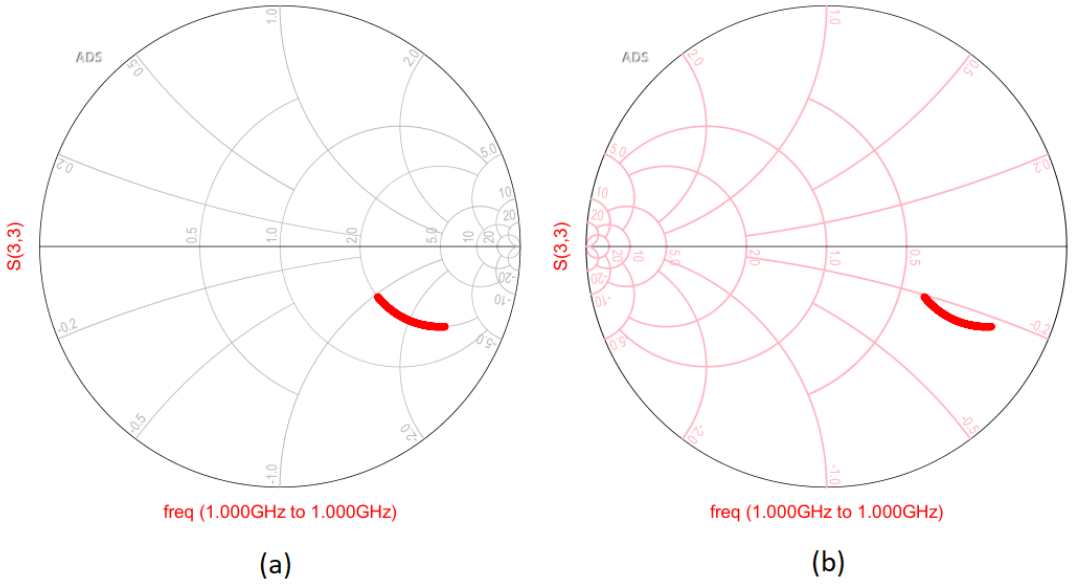


Figure 3: Smith chart for the RC series circuit.

On the contrary, the circuit at the right have a inductance in parallel with a resistor and when varying the inductance, a most convenient way to observe the variation of the reflection coefficient is by the admittance chart in the figure 4 (a), since the markers walk in the circle of constant conductance.

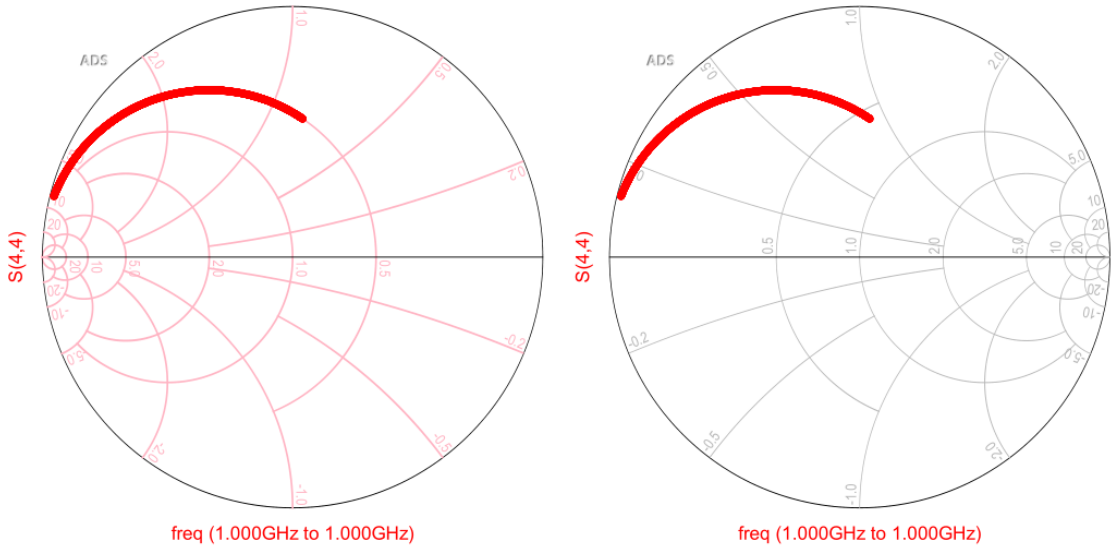
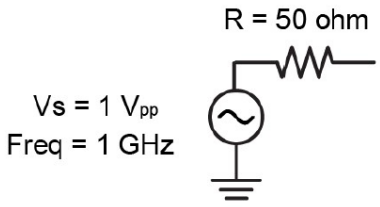


Figure 4: Smith chart for the RL parallel circuit.

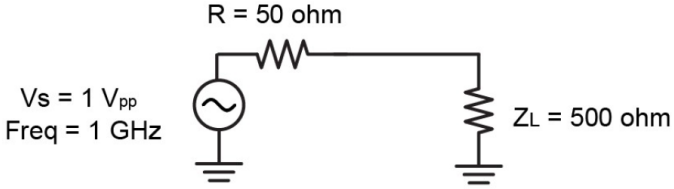
2 Problem 2

Considering the expression 1 for the power available by the source, where V_S is the peak source voltage and R is the source series resistance with the values observed in the figure below we can obtain a power of $P_{av\_s} = \frac{|0.5|^2}{8 \times 50} = 0.625mW$. The only way to extract all the power from the source is terminating the circuit of the figure below with a load whose resistance matches the source series resistance, in other words a load of $Z_L = 50\Omega$.



$$P_{av\_s} = \frac{|V_S|^2}{8R} \tag{1}$$

Despite the previous results, the circuit was terminated with a load of $Z_L = 500\Omega$ as seen in the circuit of the figure below.



The voltage at the load terminals will obey a simple voltage divider, so that:

$$V_L = \frac{Z_L}{R + Z_L} V_S = \frac{500}{50 + 500} \times 1 = 0.91 V_{pp}$$

In this way the power at the load considering the peak voltage is:

$$P_L = \frac{V_L^2}{Z_L} = \frac{0.455^2}{2 \times 500} = 0.2mW$$

It is clearly seen that the power supplied to the load is way bellow the power available by the source ($P_L < P_{av\_s}$) since there is no match between the source and load impedance.

An inefficient match can be achieved associating a resistor in parallel with the load to guarantee that the equivalent of the load impedance is 50Ω. The value of the resistor R_A can be founded by the equation below:

$$\frac{Z_L R_A}{Z_L + R_A} = 50$$

In the way that $R_A = 55.55\Omega$. Once the match is achieved the load voltage will be $V_L = \frac{V_S}{2} = 0.5 V_{pp}$, but since $R_A < Z_L$, the current flowing through R_A will be higher than the load current and resulting in a loss of efficiency with energy being wasted. This can be shown by the power in each resistor, so that:

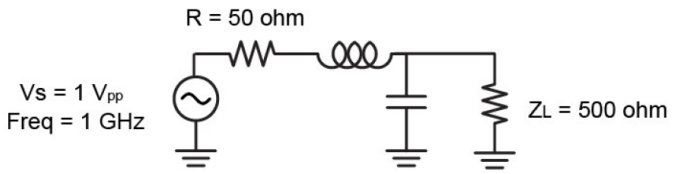
$$P_A = \frac{V_L^2}{2R_A} = \frac{0.25^2}{2 \times 55.55} = 0.562mW$$

and

$$P_L = \frac{V_L^2}{2Z_L} = \frac{0.25^2}{2 \times 500} = 0.0625mW$$

Therefore $P_L < P_A$. To confirm that all available power is being extracted from the source, simply add the powers resulting in: $P_L + P_A = 0.562 + 0.0625 \approx 0.625mW = P_{av\_s}$.

The correct way to ensure the match is with reactive components that, ideally, do not dissipate energy. The circuit of the figure below illustrates the desired matching network.



The values of capacitance (C) and inductance (L) can be found via the Smith chart. Resorting to the ADS, the algorithm 1 was used to find the values of C and L to guarantee that the normalised impedance (Z_{eq}) seen from the source is the real unit (of which

correspond to the centre of the chart):

Algorithm 1: How to find the LC impedance matching network via Smith chart

Result: L and C

Initialise L and C heuristically;

while $\Re\{Z_{eq}\} \neq 1$ **do**

  Keep value of L;

  Vary the value of C towards $\Re\{Z_{eq}\} = 1$;

  Find Z_{eq} for the new circuit configuration;

end

while $\Im\{Z_{eq}\} \neq 0$ **do**

  Keep value of C;

  Vary the value of L towards $\Im\{Z_{eq}\} = 0$;

  Find Z_{eq} for the new circuit configuration;

end

The algorithm above allowed us to determine a close match with $L = 24nH$ and $C = 0.95pF$, resulting in the Smith chart of the figure 5. Clearly this method does not allow a perfect match since it depends on graphical output, but can be set a admissible error to stop the while loops of the algorithm so convergence is guaranteed.

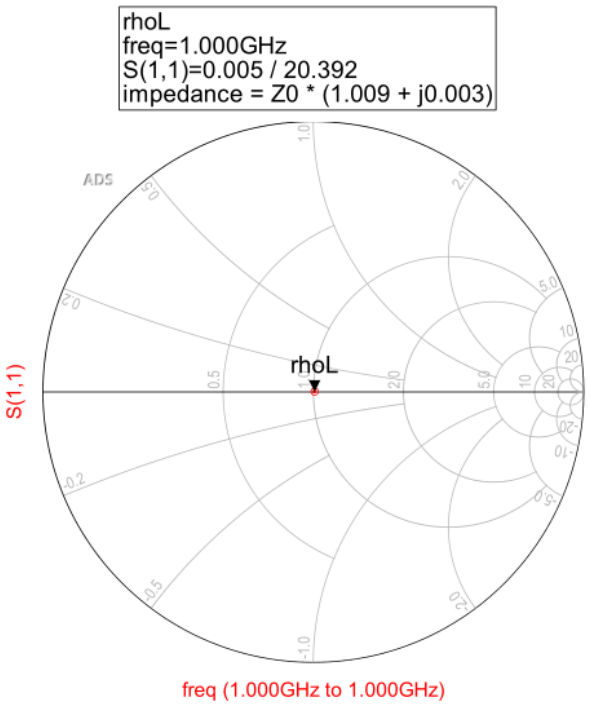


Figure 5: Smith chart for impedance matching in problem 2.

Regarding the voltage at the load its value over the transient simulation can be seen in the graph of the figure 6 as $V_L = 0.791V_p$. A curious fact is that the load voltage is higher than the source. This is a direct effect of the matching network that

the voltage wave resonates with the natural frequency of the system and provoke a rise in the load voltage. From the source point of view, the load impedance is masked with the same impedance as the source impedance, so even with $Z_L = 500\Omega$ the load will extract the total available power because the risen in the voltage will balance the power, so: $P_L = V_L^2/(2 \times Z_L) = (0.791)^2/(2 \times 500) = 0.625mW$

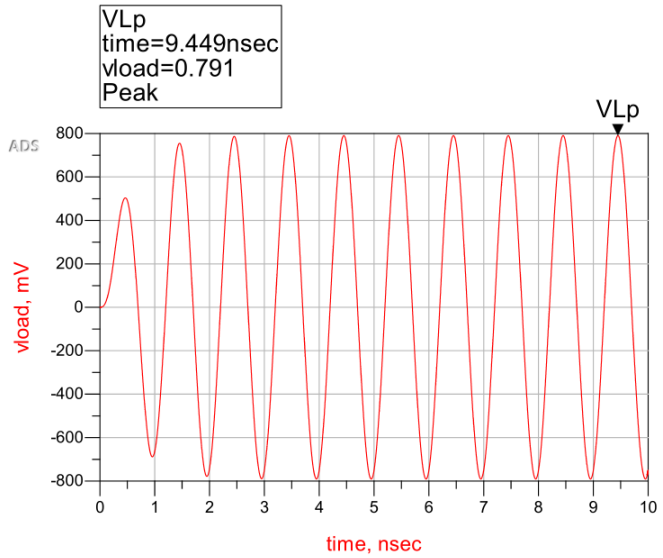


Figure 6: Transient simulation of previous circuit with matching network.

3 Problem 3

This problem will address the transmission line of figure 7. The objective of this problem is to validate the results of the S-parameters. First of all the calculations will consider terminations of $Z_S = Z_L = Z_0 = 50\Omega$, line characteristic impedance of $Z = 75\Omega$ and frequency of $1GHz$. Then after the frequency will seep between $500MHz$ and $1.5GHz$.

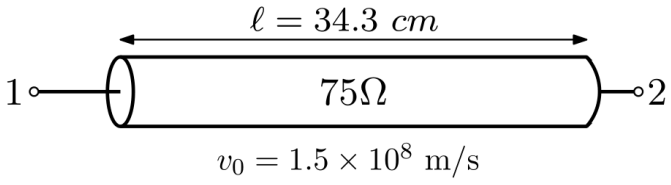


Figure 7: Transmission line for problem 3.

3.1 Theoretical values for S-parameters

Once the circuit is symmetrical, the input impedance seen in each port is the same and computed by the equation 2

$$Z_{in} = Z\frac{Z_0 + jZ\,tg(\beta l)}{Z + jZ_0\,tg(\beta l)} \tag{2}$$

Where $\beta = 2\pi/\lambda$ and $\lambda = v_0/f$, resulting in $Z_{in} = 107.52\angle -10.38°\Omega$.

So both the reflection coefficients and, therefore the coefficients of the S matrix main diagonal are:

$$|s_{11}| = |s_{22}| = \left|\frac{Z_{in} - Z_0}{Z_{in} + Z_0}\right| = 0.376 \;\; or \;\; -8.49dB \tag{3}$$

Considering a lossless line, the output power will be equal to the input power. But the input power is the total power available at the source subtracted the reflection losses, resulting in $P_{out} = P_{in} = P_{av,s} - P_r$. Since the reflection losses are a portion of the available power scaled by the reflection coefficient: $P_r = |s_{11}|^2 P_{av,s}$, the expression for the output power can be rewritten as: $P_{out} = P_{av,s}(1 - |s_{11}|^2)$; resulting in a power transmission coefficient of $|s_{21}|^2 = 1 - |s_{11}|^2$. The same can be deducted from the second port point of view resulting in $|s_{12}|^2 = 1 - |s_{22}|^2$. This results in the coefficients for the S matrix secondary diagonal at the equation 4.

$$s_{21} = s_{12} = \sqrt{1 - |s_{11}|^2} = \sqrt{1 - |s_{22}|^2} = 0.926 \;\; or \;\; -0.667dB \tag{4}$$

It is good to remember that the equations $|s_{11}|^2 + |s_{21}|^2 = 1$ and $|s_{22}|^2 + |s_{22}|^2 = 1$ are true in a lossless condition only.

3.2 Simulated values for S-parameters

Using the ADS to simulate the previous circuit in a S-parameters simulation, the curves for the magnitude of all matrix S coefficients as seen in figure 8 in a range of $500MHz$ to $1.5GHz$.

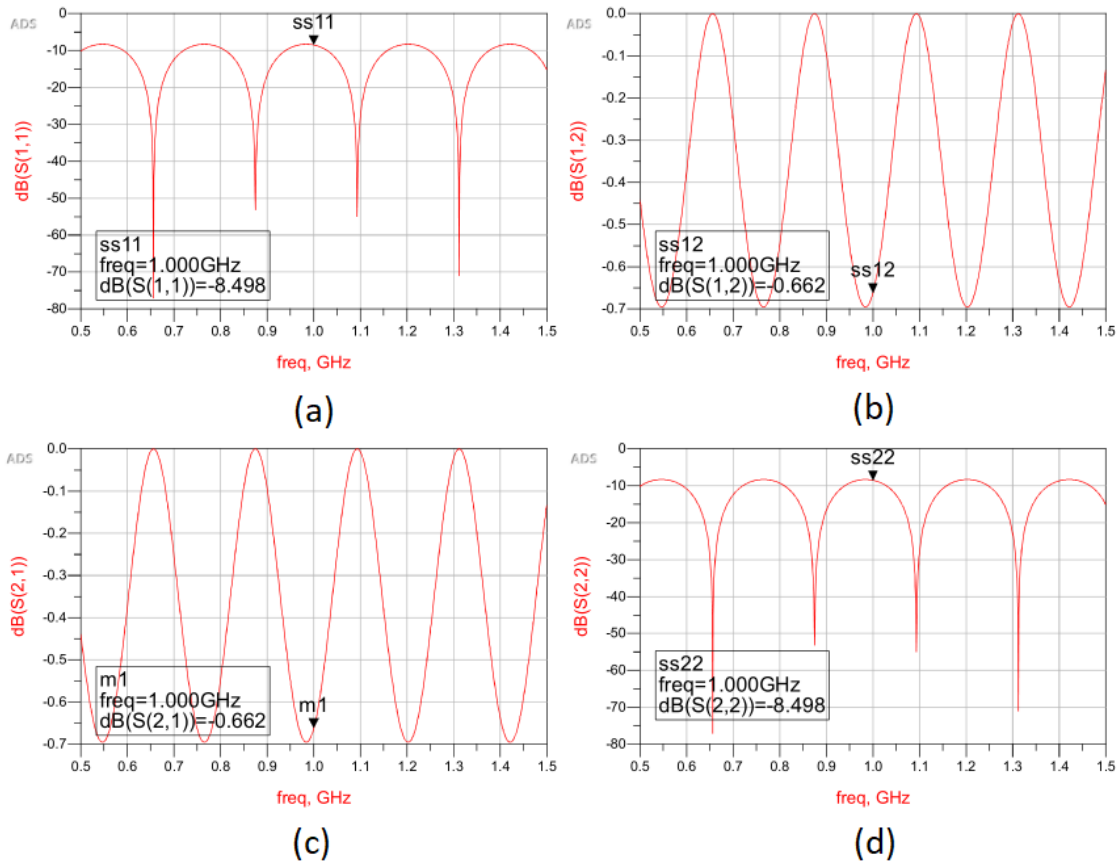


Figure 8: Problem 3 circuit S-parameters: (a) s_{11}, (b) s_{12}, (c) s_{21} and (d) s_{22}.

Observing the markers in figure 8 show the results for each one of the S-parameters at $1GHz$ in dB and they agree with the values obtained is the previous calculations expressed in the equations 3 and 4.

Regarding to the relation $|s_{11}|^2 + |s_{21}|^2 = 1$ explained before, it can be obtained in the ADS simulation and its veracity does not depend on the frequency, as seen in figure 9.

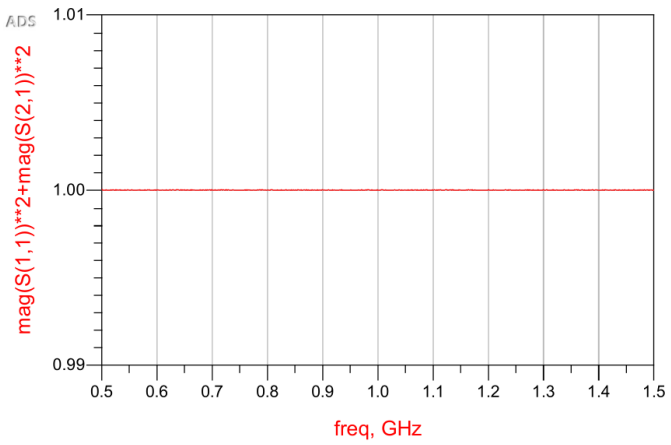


Figure 9: $|s_{11}|^2 + |s_{21}|^2 = 1$ relation in ADS.

4 Problem 4

This problem consists in the analysis of the scattering parameters for a common-emitter amplifier with BC549 as seen in figure 10.

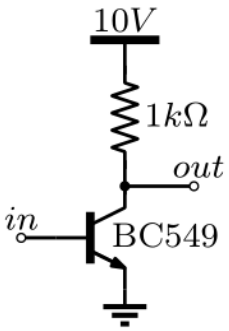


Figure 10: Common-emitter amplifier with a bipolar junction transistor BC549.

The circuit above was simulated via ADS with the conditions below:

- BJT polarized with $675mV$;
- Source and load impedance of $Z_L = Z_S = 50\Omega$;
- S-parameters simulation with frequency sweep between $1kHz$ and $1GHz$;

The ADS allow us to plot the behavior of each one of the scattering parameters considering 2 ports as seen in figure 11.

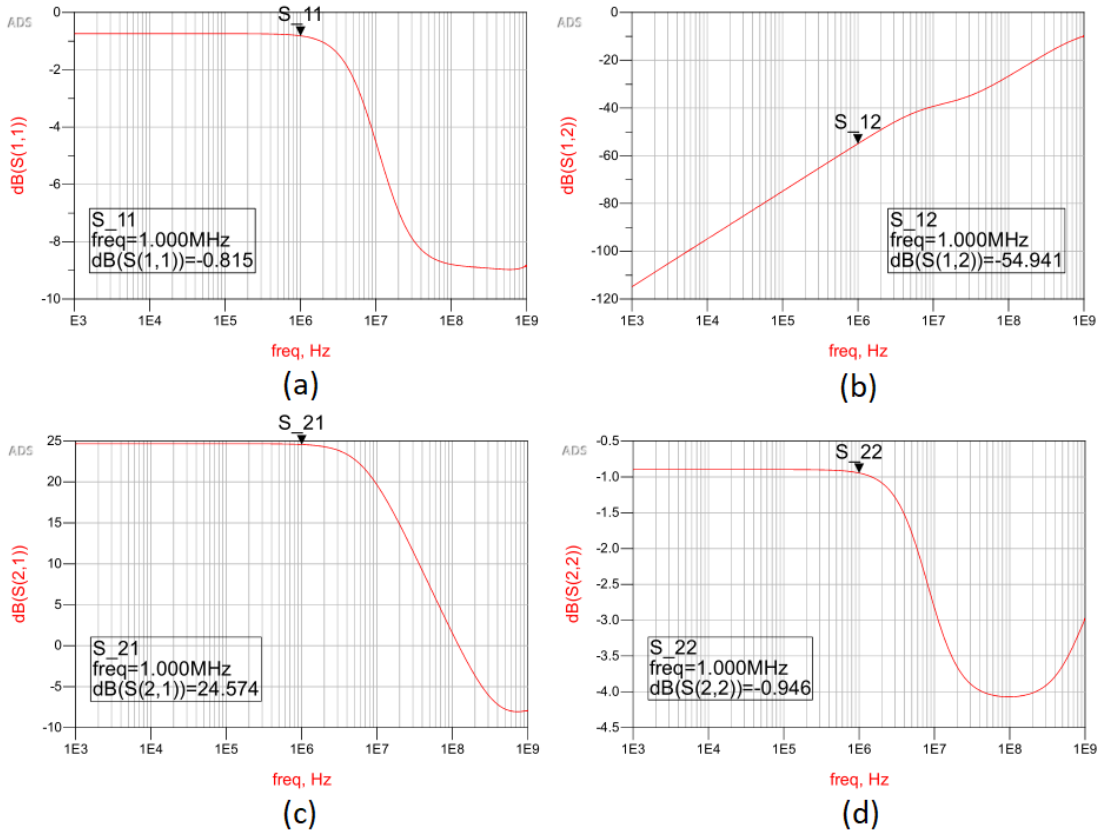


Figure 11: Common-emitter amplifier with BC549 scattering parameters magnitude: (a) s_{11}, (b) s_{12}, (c) s_{21} and (d) s_{22}.

Regarding the parameters s_{11} and s_{22} that denote the reflection coefficient in each port, we can observe by its magnitudes that they exert an approximately constant influence (but different between them) until the frequency of $1MHz$. For higher frequencies the values tend to reduce, meaning that the reflected waves with these frequencies will be less influential. Regarding the other parameters their behavior are quiet different. The magnitude of s_{21} (portion of the available power at the source [port 1] that was actually delivered to the load [port 2]) keeps approximately constant until $1MHz$ and then drops. The behavior of s_{11} and s_{22} beyond $1MHz$ are acceptable, but the effort is meaningless because of s_{21}, meaning that the reflected power is reduced as the transmitted power too.

Once the circuit is not symmetrical, all the parameters will differ. The parameter s_{12} have the oddest behavior, because it keeps risen but with no significant magnitude, meaning that the power flow from collector to base is nearly null but will rise due to the leakage current from the semiconductor junction reversed biased.

4.1 Transducer power gain vs. Power gain

The standard power gain is the relation between the output power (load power) with the input power $G_P = P_L/P_{in}$. But this relation does not take into account the power related to the reflected wave in the input port. So another metric is the transducer

power gain the relates the output power with the total power available at the source $G_T = P_L/P_{av,s}$. So this allow us to analyse the maximum power gain at a impedance match situation.

Considering that the load power is $P_L = P_{av,s} \times |s_{21}|^2$ it is clear to see that the transducer power gain is simply the equation 5. Once the input power will be the available power at the source deducted the reflection losses: $P_{in} = P_{av,s} - P_r$. The power reflected at port 1 is $P_r = P_{av,s} \times |s_{11}|^2$. Replacing the reflected power and the available power as a function of $P_{av,s} = P_L/|s_{21}|^2$ we obtain a expression that depends only on the scattering parameters for the power gain in the equation 6. The expression also shows that in a condition without reflection ($s_{11} = 0$) both the gains are equals.

$$G_T = \frac{P_L}{P_{av,s}} = |s_{21}|^2 \tag{5}$$

$$G_P = \frac{P_L}{P_{in}} = \frac{|s_{21}|^2}{1 - |s_{11}|^2} \tag{6}$$

In the previous simulation with load and source impedance of 50Ω and frequency of $100MHz$, we can see by the plot of figure 12 that $G_P = 1.648$ and $G_T = 1.43$. Since s_{11} is lower than the unit for each and all frequencies of the plot, it results in $G_P > G_T$ and this is a coherent result because $P_{av,s} > P_{in}$, remembering that the available power incorporates the input power and the losses.

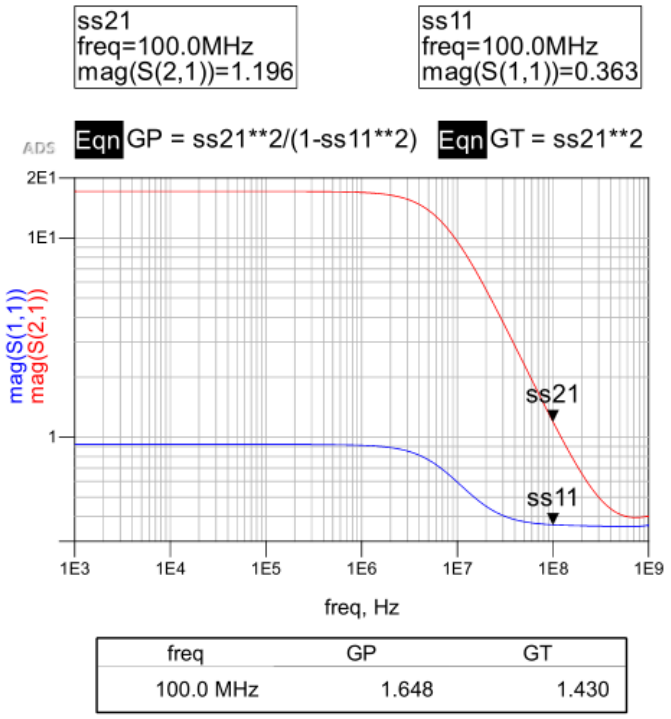


Figure 12: Common-emitter amplifier with BC549 transducer power gain (G_T) and power gain (G_P) at $100MHz$.

A practical way to prove this result is to feed the amplifier with a sine voltage of $1mV_p$ and $100MHz$ (same conditions of load and source impedance, polarization and transistor model) and check the power values. According to figure 13 the resulting gain is $G_T = 1.395$. It differs from the previous result because the latter was found by a transient simulation with a limited time step that reduces precision and has convergence problems and the other was found via a simulation of S-parameters in a single point of frequency.

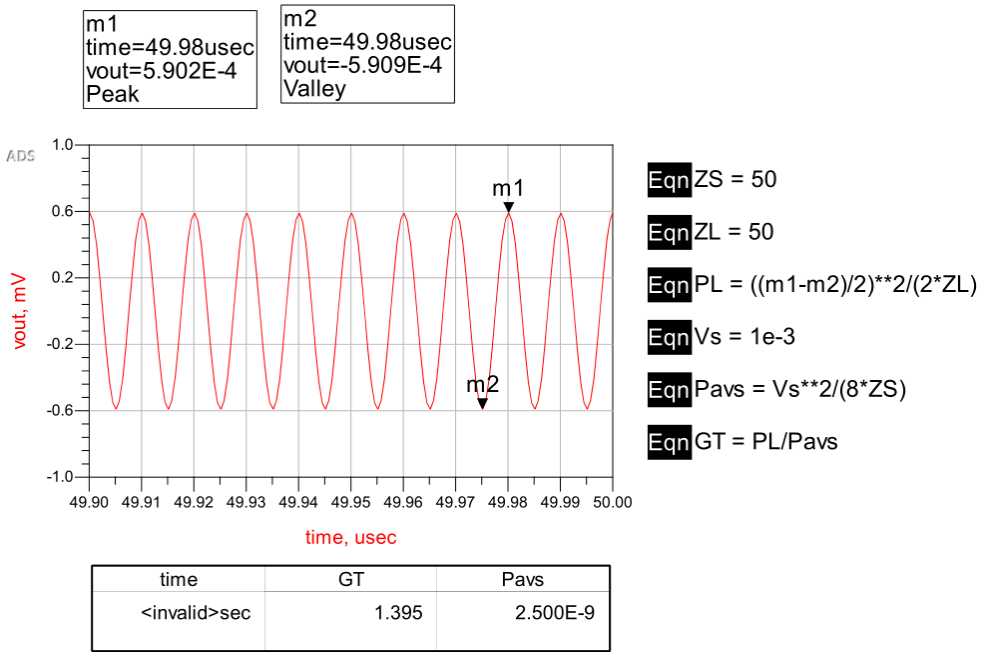


Figure 13: Proof of common-emitter amplifier with BC549 transducer power gain (G_T) at $100MHz$.

Another way to observe the transducer power gain is via a harmonic balance simulation at $100MHz$. In this case it will not be used the circuit with the BJT, but a two ports generic quadripole characterized by the S-parameters founded before. The figure 14 show the SParamChecker for the generic quadripole of which the S-parameters sampled at $100MHz$ matches the parameters obtained in the previous circuit like in figure 11.

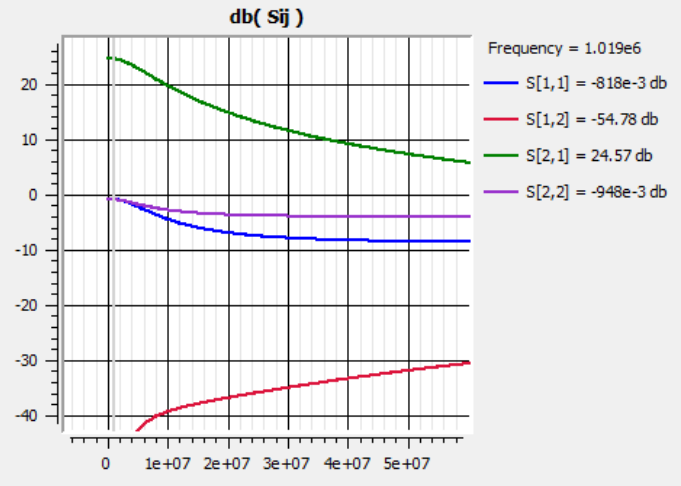


Figure 14: SParamChecker for generic quadripole.

Extracting the time domain signal from the load voltage in the harmonic balance (HB) simulation we observe the graphic in the figure 15. Despite feeding the quadripole with a $100MHz$ sinusoidal voltage like in the previous simulation, the result for the transducer power gain differs from the previous simulations.

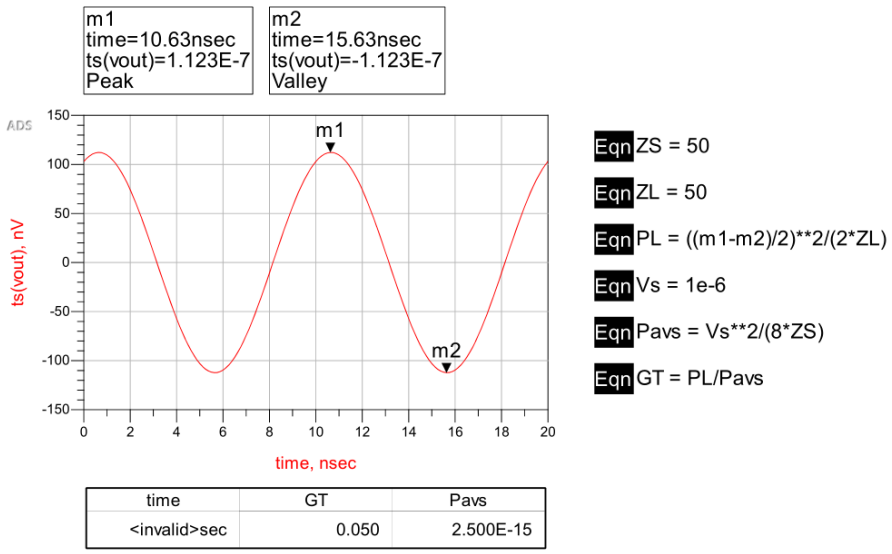


Figure 15: Time domain signal from HB simulation.

This problem might have occurred due to maladjustments in the circuit parameters.