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Centro de Tecnologia
Departamento de Engenharia Elétrica
ELE0623 - Circuitos para comunicação - 2020.2
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Fourth laboratory: **Noise**

1 Thermal noise in resistor

This section will issue the problem of thermal noise in resistors based on three different circuit topologies, which are:

- Single noisy resistor;
- Noisy resistor associated with an ideal resistor;
- Noisy resistor associated with an ideal capacitor;

1.1 Single noisy resistor

First of all the spot noise for a resistor of $R = 50\Omega$ at $T = 300K$ $(26.85°)$ is computed to serve as a theoretical basis. Therefore the noise power spectral density (PSD) is computed with the equation 1 ($k = 1.38064852 \times 10^{23}\, m^2\, kg\, s^{-2}\, K^{-1}$ it is the Boltzmann constant):

$$S_n(f) = 4kTR = 8.28 \times 10^{-19}\, V^2/Hz \tag{1}$$

So a transient simulation was executed for $1ms$ of duration with a max. time step of $1ns$. The temperature whose the resistor will operate was carefully set in the transient simulation options. The circuit setup follows the schematic of figure 1 so the noise voltage can be correctly measured.

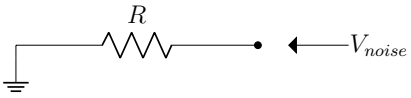


Figure 1: Circuit setup to measure single noisy resistor voltage. Source: own.

The figure 2 leads one to think that the noise has a high amplitude. But zooming in the plot to a shorter time range like in figure 2b, the low amplitude noise prevails and the high amplitude noise come to be only artifacts that appears sporadically.

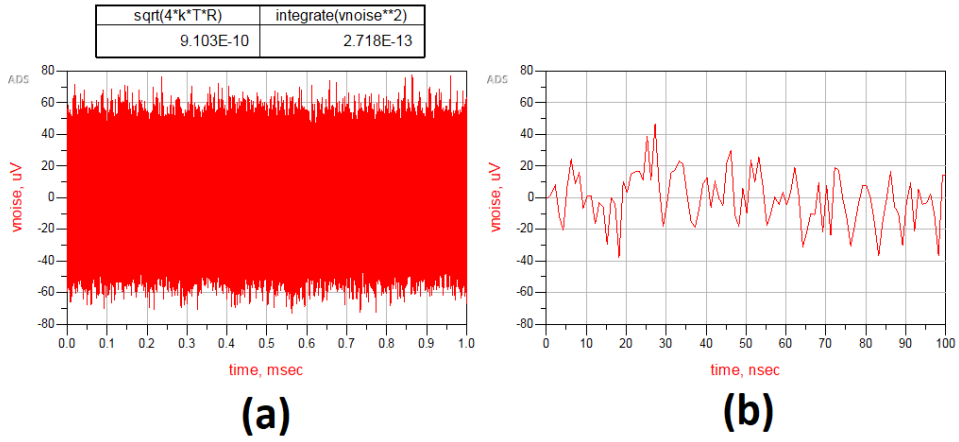


Figure 2: Noise voltage in the terminal of a single resistor.

In practice the values of noise power spectral density for a transient simulation in figure 2 does not match the theoretical one. This is explained by the inherent limitations of transient simulation.

Once the maximum time step was set to $1ns$, according to the Nyquist criterion, the highest frequency that can be reproduced in this simulation is equal to $f_N = \frac{1}{1 \times 10^{-9}} \times \frac{1}{2} = 500MHz$. Once the theoretical value takes into account the whole infinity spectrum, the simulation is limited to a small portion of it. Reducing the max. time step will improve results, but it will take too much time to simulate. A simpler solution is to perform an AC simulation, varying frequency instead of time.

Now with a AC simulation varying the frequency from 1 Hz to 100 GHz and same topology as figure 1, we may observe in figure 3 that the practical spot noise match the PSD theoretical value for both cases of $R = 50\Omega$ and $R = 200\Omega$. Also it prove that the PSD rises proportional to the resistance.

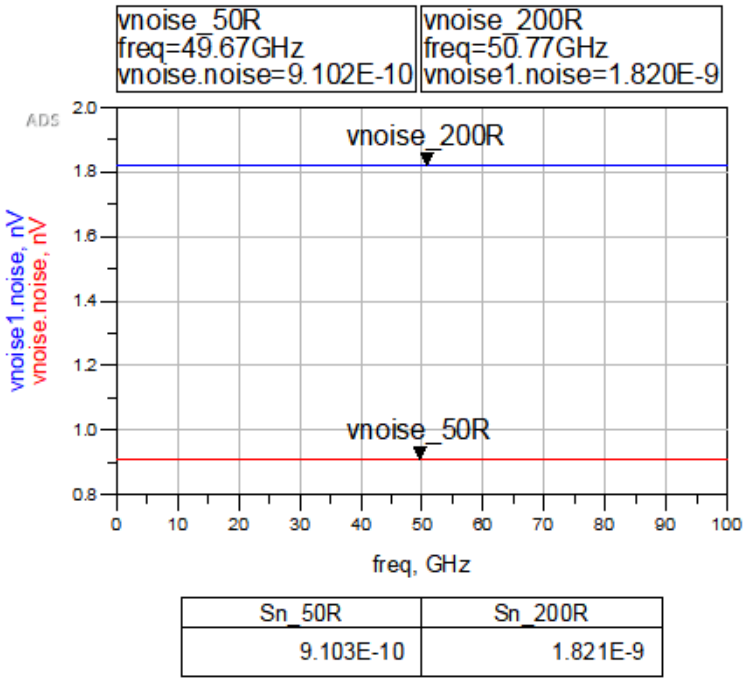


Figure 3: Noise PSD for single resistor in two resistance conditions: 50Ω and 200Ω.

1.2 Noisy resistor associated with an ideal resistor

From now on the transient simulation will not be used since the AC simulation show better results.

This section will work with a different circuit topology. As we can see in the schematic of figure 4 the circuit consists of two combined resistors, but only one generate thermal noise.

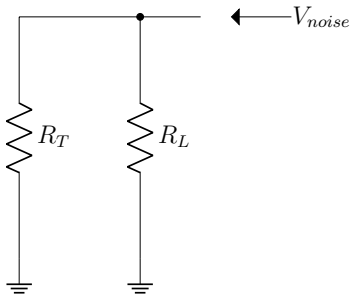
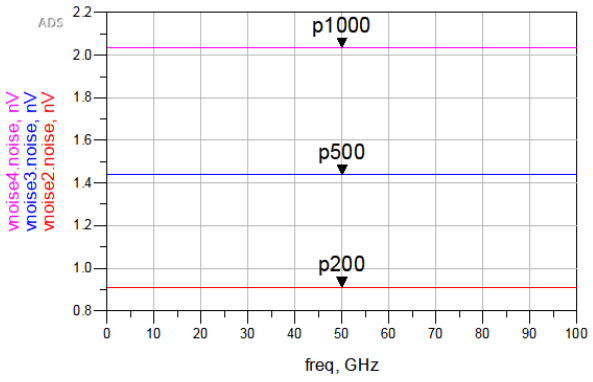


Figure 4: Circuit setup to measure noisy resistor voltage in a combination of resistors. Source: own.

According to the theory, considering the load resistor R_L without noise and the other R_T a resistor with noise, the expression for the available noise power density in given by 2. Considering both resistors to be equal $R = R_L = R_T$, the expression 2 becomes independent of the resistor value and depend only on the temperature.

$$\overline{v_{n,out}^2} = 4kT\left(\frac{R_L}{R_L + R_T}\right)^2 = 4kT\left(\frac{R}{2R}\right)^2 = kT \tag{2}$$

Simulating the circuit for $R = R_L = R_T = 200\Omega$ (and after for 500Ω and 1000Ω), the available noise power density becomes $\overline{v_{n,out}^2} = 1.38064852 \times 10^{23} \times 300 = 4.143 \times 10^{-21} V^2/Hz$. In practice, the figure 5 show the results for an AC simulation with same parameters as before,



freq	p200**2/200	p500**2/500	p1000**2/1000	k*T
49.99 GHz	4.142E-21	4.142E-21	4.142E-21	4.143E-21

Figure 5: Noise PSD for combination of equal resistance resistors, but one noise and the other not in three resistance conditions: 200Ω, 500Ω and 1000Ω.

Since the noise power density is non dependent on the resistance value (at least the resistors must to have the same resistance), we observe in the figure 5 that all the three circuits show the same noise level which is equal to the theoretical value.

1.3 Noisy resistor associated with an ideal capacitor

In this section the topology of the circuit to measure noise is as follows in the figure 6.

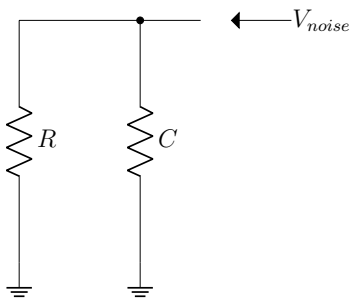


Figure 6: Circuit setup to measure noisy resistor voltage in a RC circuit with a ideal capacitor. Source: own.

In this case the total power must be $\overline{v_{n,out}^2} = \frac{kT}{C}$, so it is expected that the noise power drops with a risen capacitance and keeps the same with a varying resistance.

Simulating for $C = 100pF$ and the resistors varying from 50Ω, 200Ω and $1k\Omega$, the plot of figure 7 is obtained.

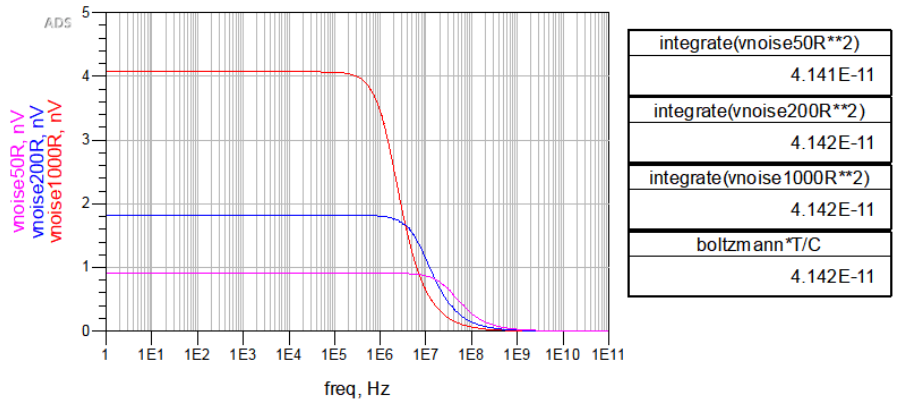


Figure 7: Noise voltage behaviour and total noise power for a RC circuit topology and three resistance conditions: 50Ω, 200Ω and $1k\Omega$.

The theoretical value for the total noise power is computed in the figure 7 along side of the practical results, and once they are equal, it became proved that the total noise power in this circuit topology is non dependent on the resistance value.

A curious fact is the noise voltage behaviour. In the pure R circuit the noise voltage kept constant along all frequencies, but in the case of a RC circuit the noise in higher frequencies is filtered due to the capacitor. In this case the circuit by itself get rid of the noise in higher frequencies, no needing any design intervention.

2 Thermal noise in BJT

This problem works with the BJT and the objective is to evaluate all three noises: thermal, flicker and shot.

First a simple circuit is assembled with the transistor BFU530 from NXP. Also it is applied two DC voltage sources to polarize the BJT. In this case with $V_{be} = 0.8V$ and $V_{ce} = 3V$. An AC simulation is executed from 1 Hz to 10 GHz.

Additionally two DC feeders are added in the connection of each voltage source to its respective BJT node (base and collector). The DC feeder prevent interference between the BJT own noise with another noise source.

First of all we observe in figure 8 the simulation results taking into account all noise sources combined. The first identified noise type is the flicker (or $1/f$ noise), that extends in all frequency range with a decaying characteristic. In $10^5 Hz$ there is a higher decaying rate in the PSD, this marks the end of the constant spot noise and the begin of the cutoff band from the filtering result by the parasite capacitances inherent to the BJT. Last, the thermal noise serves as a background offset the maintains approximately constant all over the frequency range.

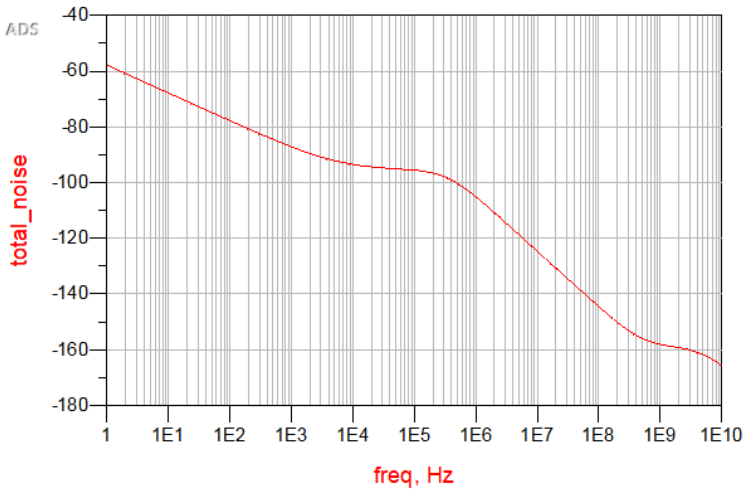


Figure 8: Noise PSD response for BJT BFU530 from NXP.

A better way to observe each noise source effect is disassembling each component and plotting each contribution separated. The figure 9 show each noise source influence. As mentioned before, the spot noise has a clear white behaviour until the parasite capacitances cutoff at $10^5 Hz$. Different from the spot noise, the thermal noise has a white behaviour that depends only on the temperature and the resistance and keeps constant until approximately $100THz$. The flicker noise has a $1/f$ behaviour before the cutoff and decays with a higher rate after it.

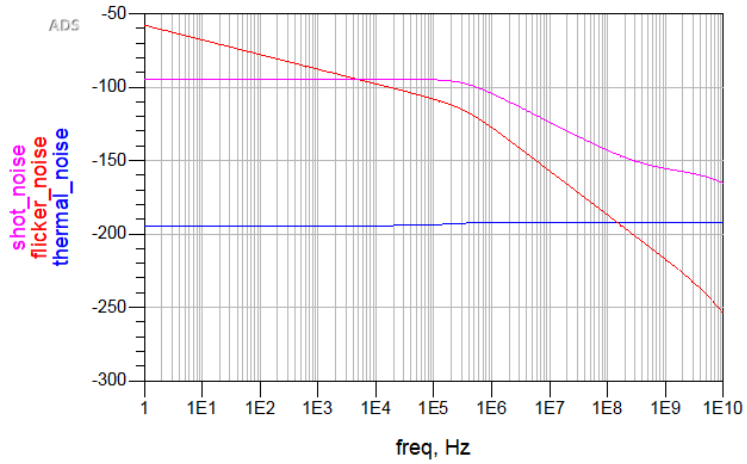


Figure 9: Disassembled noise PSD response for BJT BFU530 from NXP.

3 Low noise amplifier: matching for noise

This problem uses a NXP LNA model BGU6104. The objetive of this section is to compare matching networks for maximum power deliverance with networks to minimum noise figure.

The simulation imports the model as a quadripole with both ends terminations of 50Ω (optimal source impedance) and performs a S-param type simulation from 100 MHZ up to 3.5 GHz. It is important to point out that the model represents $V_{cc} = 3V$ and $I_{cc} = 6mA$, so we guarantee a solid basis of comparison between practical results and the datasheet.

There is a section showing dynamic characteristics in the BGU6104 datasheet, such as insertion power gain and minimum noise figure at a given frequency. So this values will be compared with the results of simulation in a proper table.

The first variable to compare is the insertion power gain $|s_{21}|^2$ which is represented in the plot of figure 10. Extracting the equivalent values from the datasheet, we obtain the table 1 with results very close to each other.

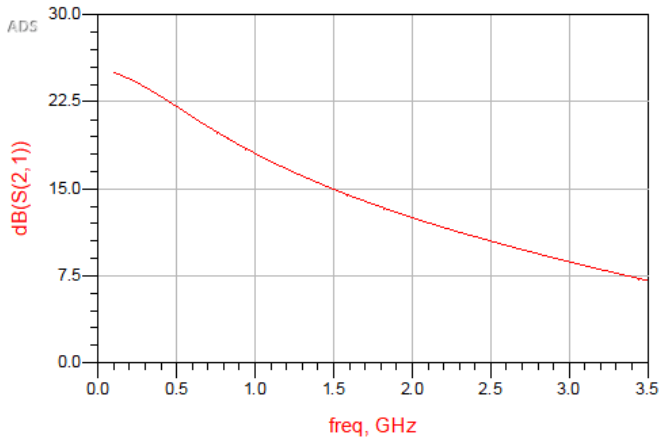


Figure 10: Insertion power gain for LNA without any matching network.

Table 1: Comparison between datasheet and simulation result for insertion power gain at $V_{cc} = 3V$ and $I_{cc} = 6mA$,

	Insertion power gain $\|s_{21}\|^2$ (dB)	
Frequency (MHz)	**Datasheet**	**Simulation**
100	25	24.964
150	24.5	24.765
450	22.5	22.511
900	18.5	18.753
1500	14.5	14.939
1900	12.5	12.939
2400	10.5	10.845
3500	7	7.054

The second variable for analysis is the noise figure NF and the minimum noise figure NF_{min} as shown in the plot of figure 11. Since there is no matching networks in this first circuit, the noise figure is way above its minimum, needing a matching for noise to reduce

it towards the minimum. The table 2 show the comparison results for the minimum noise figure with close values meaning that good results were obtained in the simulation.

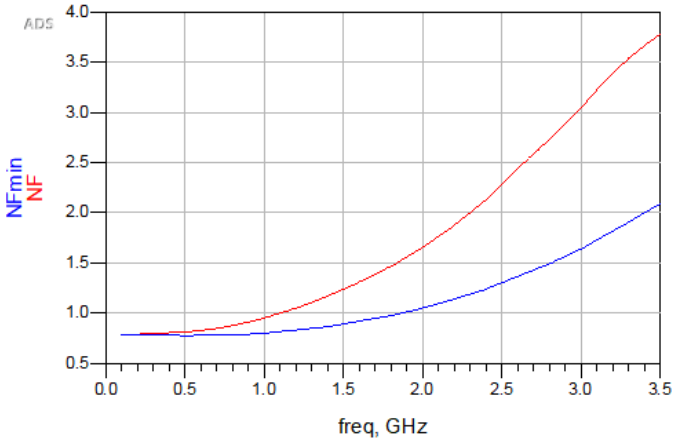


Figure 11: Noise figure and minimum noise figure for LNA without any matching network.

Table 2: Comparison between datasheet and simulation result for minimum noise figure at $V_{cc} = 3V$ and $I_{cc} = 6mA$,

	Insertion power gain NF_{min} (dB)	
Frequency (MHz)	**Datasheet**	**Simulation**
100	0.8	0.777
150	0.8	0.777
450	0.8	0.777
900	0.8	0.789
1500	0.9	0.892
1900	1	1.012
2400	1.2	1.242
3500	2.1	2.09

Despite the results match with the datasheet, however they does not represent intended characteristics in a practical application. Analysing at 2 GHz, we have the following results in the simulation e.g. $|s_{21}|^2 = 12.494dB$, $NF = 1.659dB$, $NF_{min} = 1.051dB$, meaning that with a proper matching network either the insertion power gain can be improved (power matching) at 2 GHz or the noise figure can be reduced towards the minimum (noise matching).

The first step to design the matching networks is to visualize the values of s_{11} and s_{opt} in the smith chart of figure 12. Using the input impedance associated with s_{11} we can design a matching network to maximize power, but using the one associated with s_{opt} we can design a matching network to minimize the noise figure.

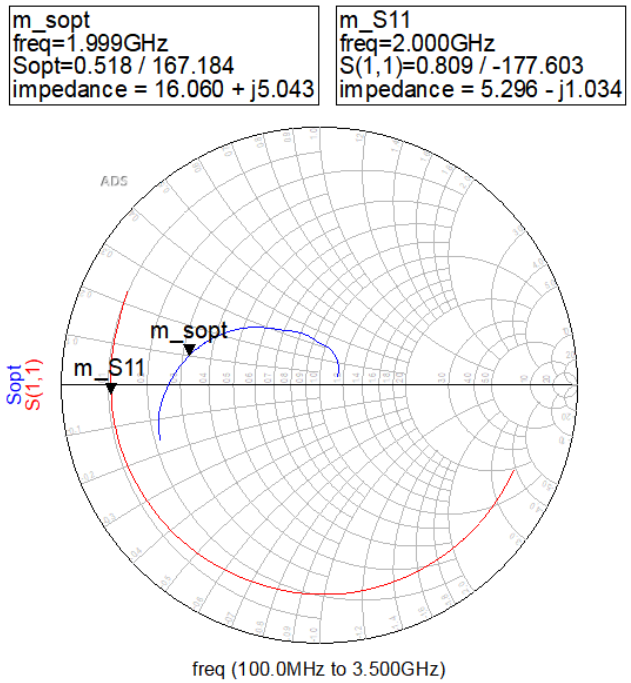


Figure 12: Smith chart containing the values of s_{11} and s_{opt} without any matching.

So, aiming a max. power matching it was designed a L network whose would consider the input impedance $5.2 - j1\ \Omega$ as in figure 12. The L network for min. noise matching was designed using the s_{opt} correspondent conjugate impedance of $16 - j5\ \Omega$ as in figure refsmith:1.

The figure 13 show both results for a matching network to achieve max. power transference 13(a) and min. noise figure 13(b). In 13(a) the insertion power gain of 17.1 dB is higher than the previous value of 12.49 dB denoting a good matching network. In the case of figure 13(b) the noise figure perfectly matches with the minimum value at the given frequency.

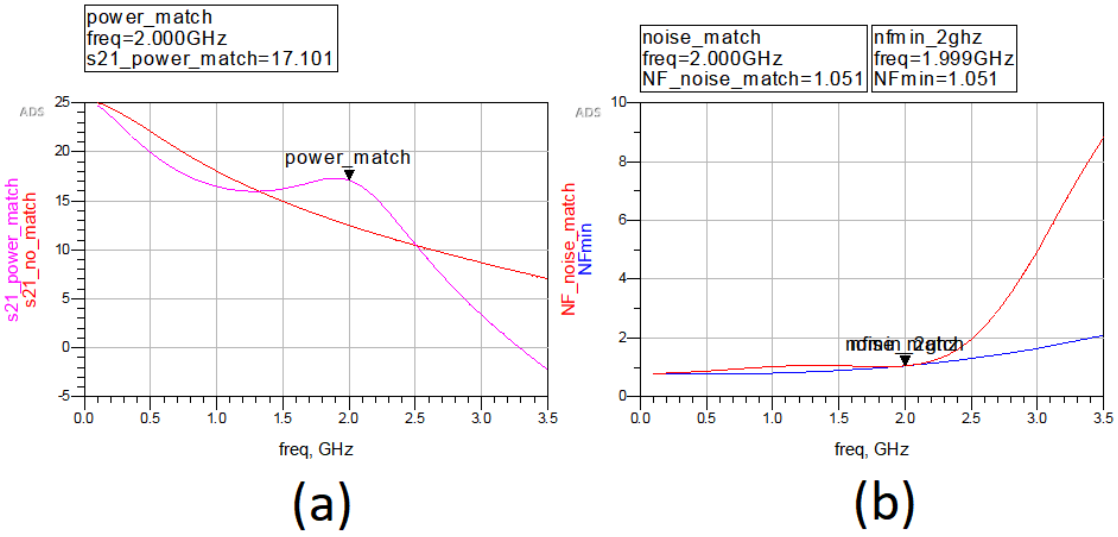


Figure 13: (a) Insertion power gain with max. power matching network to 2 GHz and (b) Noise figure with min. noise figure matching network to 2 GHz.

It is the designer choice to define if the circuit will care with a power matching or a noise matching, once that it has to bear in mind the objective and flaws of one's application.