Universidade Federal do Rio Grande do Norte
Centro de Tecnologia
Departamento de Engenharia Elétrica
ELE0623 - Circuitos para comunicação - 2020.2
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Third laboratory: **Impedance matching networks**

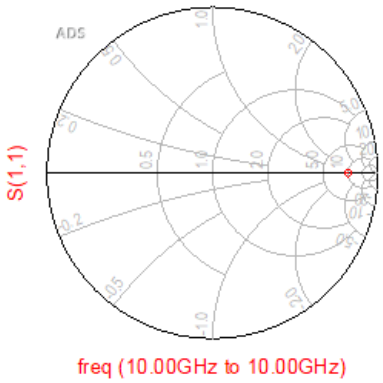
1 Problem 1

This problem will only address L type matching networks and work considering the load impedance higher than the source impedance ($R_L > R_S$). The second variant with $R_S > R_L$ will be addressed in the second problem.

1.1 Designing the matching network

The circuit without the matching network is a simple series association of a `Term` component representing the source and it has a impedance of $R_S = 10\Omega$ and another `Term` of impedance $R_L = 100\Omega$ representing the load. The desired resonance frequency must be $f_o = 10GHz$.

First of all we simulate the circuit as it is, only concluding by the smith chart of figure 1 ($|S_{11}| \neq 0$) and the value of input impedance that there is no match between the terminal impedances. The input impedance was found with the ADS function `stoz` using the reflection coefficient S_{11}.



freq	S(1,1)	Zin
10.00 GHz	0.818 / 0.000	100.000 / 0.000

Figure 1: Circuit $R_S = 10\Omega$ and $R_L = 100\Omega$ without matching network.

Since the input impedance seen from the source must be a lower value than the actual load impedance, the L network in figure 2 will promote a parallel to series impedance

transformation in a way that the load impedance seen from the source point-of-view is $R_{in} = R_S$.

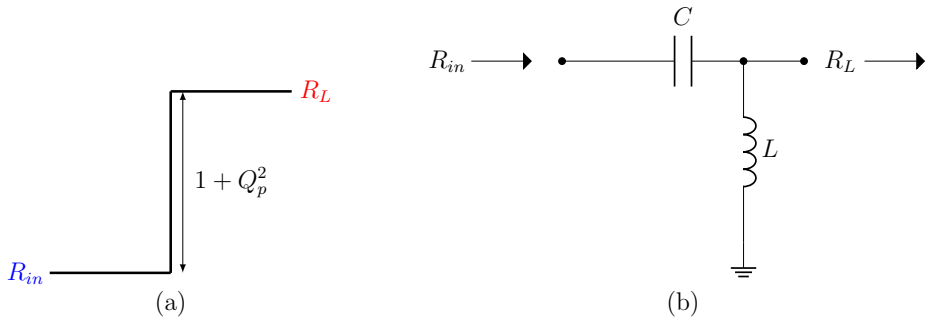


Figure 2: (a) Desired effect of impedance gain (b) L matching network for a parallel to serial transformation of load impedance. Source: own.

As seen in figure 2(a), the impedance gain must reduce the value of the load impedance such in equation 1.

$$R_{in} = \frac{R_L}{1 + Q_p^2} \tag{1}$$

The quality factor for the parallel association is 2:

$$Q_p = \sqrt{\frac{R_L}{R_{in}} - 1} = 3 \tag{2}$$

Since the inductance of the matching network is in parallel association with the load impedance, the parallel quality factor is also found as the relation between the resistance with the reactance, resulting in a expression for the network inductance 3.

$$Q_p = \frac{R_L}{L\omega_o} \Longrightarrow L = \frac{R_L}{Q_p\omega_o} = 0.53\,nH \tag{3}$$

To calculate the network capacitance we need to transform the parallel RL portion in a RL series association, transforming L in its series equivalent with equation 4.

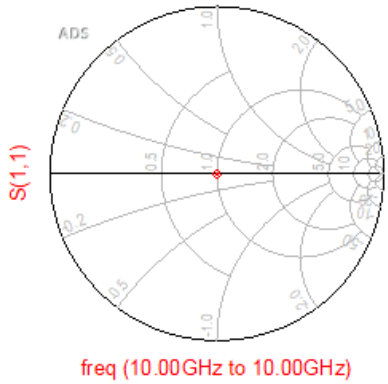
$$L_s = \frac{L}{1 + Qp^{-2}} = 477\,pH \tag{4}$$

The capacitance can be easily found by the resonance frequency expression 5.

$$\omega_o = \frac{1}{\sqrt{L_s C}} \Longrightarrow C = \frac{1}{L_s\omega^2} = 0.53\,pF \tag{5}$$

Despite finding a series inductance L_s, the network still be using the parallel L found before.

Using the same pattern of figure 1 we can produce a comparison with the results introducing the matching network found before, resulting in the figure 3.

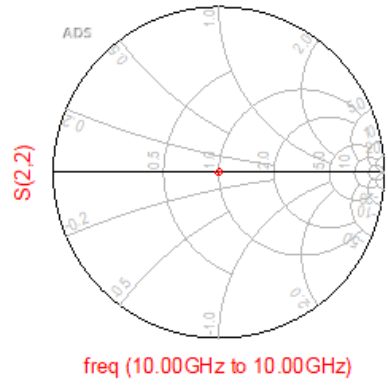


freq	S(1,1)	Zin
10.00 GHz	0.003 / -108.267	9.983 / -0.302

Figure 3: Circuit $R_S = 10\Omega$ and $R_L = 100\Omega$ with matching network.

As we can see from the values of the reflection coefficient and the input impedance, they do not represent a perfect match due to rounding errors in the computation, but they are a good approximation for $|S_{11}| \approx 0$ and $Z_{in} \approx 10\Omega$.

It is important to observe that the designed network has the capability of transform $R_L = 10\Omega$ in $R_S = 100\Omega$ just using the topology of figure 2 mirrored. The figure 4 illustrates the smith chart representing a match ($|S_{22}| \approx 0$) and the input impedance corresponding to the new source impedance $Z_{in} \approx 100\Omega$.



freq	S(1,1)	Zin2
10.00 GHz	0.003 / -108.267	100.174 / 0.302

Figure 4: Circuit $R_S = 100\Omega$ and $R_L = 10\Omega$ with matching network.

As a matter of comparison on future topics, we have designed a second L type matching network for a circuit with $R_S = 20\Omega$, $R_L = 100\Omega$ and $f_o = 10GHz$ using the same methodology as before and same matching network topology (like in figure 2), with quality factor $Q = 2$, inductance $L = 0.7958\,nH$ and capacitance $C = 0.3979\,pF$.

1.2 Bandwidth

To evaluate the different bandwidths from the circuits designed before we enumerated its terminals from 1 to 4. The circuit with a distinct $R_S = 10\Omega$ has a source terminal #1 and a load terminal #2. The circuit with a distinct $R_S = 20\Omega$ has a source terminal #3 and a load terminal #4.

In this way we can run a S-parameters simulation from 5 GHz up to 30 GHz and observe the -3dB and 90% bandwidth of $|S_{21}|^2$ and $|S_{43}|^2$.

1.2.1 -3dB bandwidth

The -3dB bandwidth is calculated observing the value of $|S_{21}|^2$ and $|S_{43}|^2$ in a dB scale. As we can see in figure 5 with both curves overlapping, the second circuit with $R_S = 20\Omega$ has a higher bandwidth, once the quality factor is lower than the other circuit and the bandwidth obey the relation $\Delta\omega_{-3dB} = \omega_o/Q = 3.33GHz$ for $Q = 3$ and $5GHz$ for $Q = 2$.

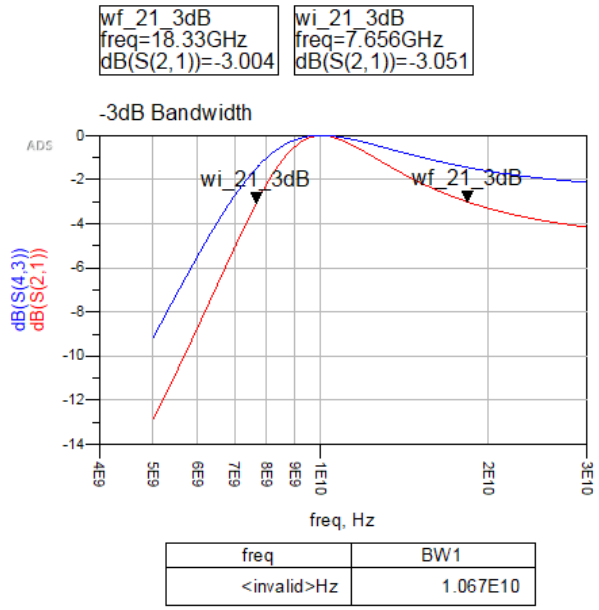


Figure 5: -3dB bandwidth for $|S_{21}|^2$ and $|S_{43}|^2$.

The value for the second circuit -3dB bandwidth was not determined since $|S_{43}|^2$ does not cross the -3dB value a second time.

1.2.2 90% bandwidth

The 90% bandwidth tends to be narrower than the -3dB, representing only a third of the previous value ($\Delta\omega_{90\%} = \Delta\omega_{-3dB}/3 = 1.11GHz$ for $Q = 3$ and $1.66GHz$ for $Q = 2$). In this case, the values of $|S_{21}|^2$ and $|S_{43}|^2$ are better seen in a linear scale since the limits of the 90%bandwidth will be 0.9. The figure 6 show the results.

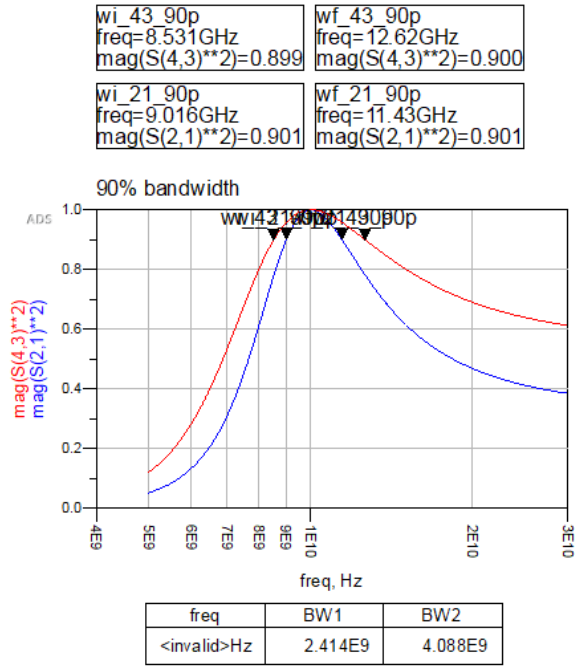


Figure 6: 90% bandwidth for $|S_{21}|^2$ and $|S_{43}|^2$.

The results allow us to define the bandwidths for both circuits. As mentioned in the previous topic, the bandwidth for the circuit with $R_S = 20\Omega$ still higher than the other circuit as expected.

1.2.3 Comparison

First comparing the -3dB theoretical bandwidth of 3.33 GHz with the value obtained in practice 10 GHz it is clearly seen a large discrepancy. This is explained once a additional source resistance is added to the RLC circuit, with both load and source resistance equal, thus resulting in two more times dissipated energy and halving the quality factor, resulting in the double of bandwidth in practice. The remaining discrepancy is explained once the quality factor definition relies on a RLC circuit, and when we associate the resistance of both source and load in different ends of the circuit with the matching network, we achieve a perfect RLC circuit no more . So the previous analysis for the quality factor only serves as approximation for what we can expect from this kind of circuit.

Now comparing the -3dB bandwidth of the circuit 1 in figure 5 with its equivalent in the 90% bandwidth in figure 6 we observe a scaling difference of 4.42 times, although it was expected a relation of 3. This behaviour is reminiscent of the problem above.

2 Problem 2

This problem address multiples matching networks topologies, still using a L network, but introducing the T network and a multiple sections matching network.

2.1 Designing the matching network

The circuit without the matching network is a simple series association of two `Term`s component representing the source with $R_S = 500\Omega$ and other representing the load with $Z_L = 50 + j15.9\Omega$ at $f_o = 1GHz$.

In a passive component representation, the load impedance can be seen as a series association of a resistance of $R_L = 50\Omega$ with a inductance of $L_L = X_L/w_o = 2.53\,nH$.

Since the input impedance seen from the source must be a higher value than the actual load impedance, the L network in figure 7 will promote a series to parallel impedance transformation in a way that the load impedance seen from the source point-of-view is $R_{in} = R_S$.

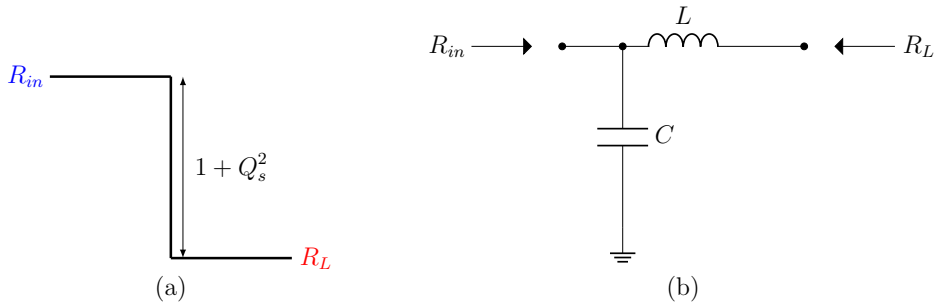


Figure 7: (a) Desired effect of impedance gain(b) L matching network for a serial to parallel transformation of load impedance. Source: own.

This circuit differs from the previous because it introduces a inductance in the load impedance. But this does not present any problem, since the network of figure 7 introduces a inductor in series with the load and its value can be found disregarding the load inductance and after concluding the project, the load inductance can be deducted from the network inductance.

As seen in figure 7(a), the impedance gain must amplify the value of the load impedance such in equation 6.

$$R_{in} = R_L(1 + Q_s^2) \tag{6}$$

The quality factor for the series association is 7:

$$Q_s = \sqrt{\frac{R_i n}{R_L} - 1} = 3 \tag{7}$$

Since the inductance of the matching network is in a series association with the load, the series quality factor is also found as the relation between the reactance with the resistance, resulting in a expression for the network inductance 8.

$$Q_s = \frac{L\omega_o}{R_L} \Longrightarrow L = \frac{Q_s R_L}{\omega_o} = 23.87\,nH \tag{8}$$

To calculate the network capacitance we need to transform the parallel L portion in a RLC series association, transforming L in its series equivalent with equation 9.

$$L_s = \frac{L}{1 + Qp^{-2}} = 26.53\,nH \tag{9}$$

The capacitance can be easily found by the resonance frequency expression 10.

$$\omega_o = \frac{1}{\sqrt{L_s C}} \Longrightarrow C = \frac{1}{L_s \omega^2} = 0.9549\,pF \tag{10}$$

Yet the true value of L was not found, and its results from subtracting the load inductance $L_L = 2.53\,nH$ from the result in 8, so we have $L = 21.34\,nH$.

The figure 8 illustrates the smith chart representing a match ($|S_{11}| \approx 0$) and the input impedance corresponding to the new source impedance $Z_{in} \approx 500\Omega$ at $1GHz$.

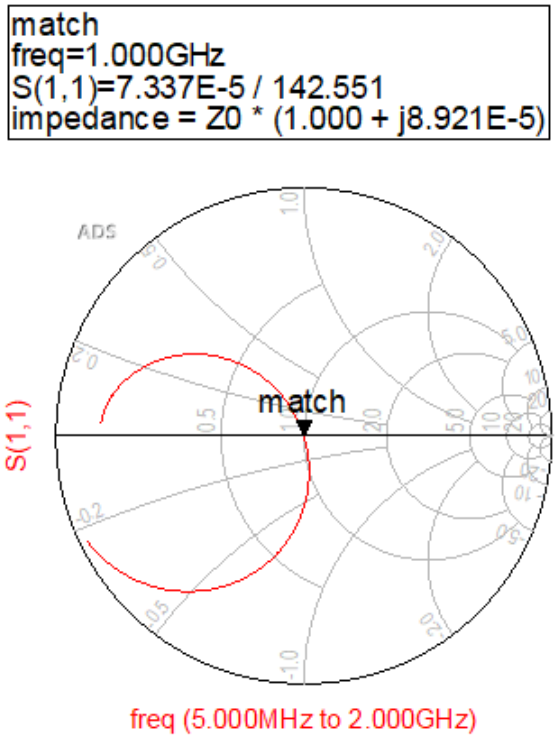


Figure 8: Circuit $R_S = 500\Omega$ and $R_L = 50\Omega$ with matching network.

As a matter of comparison on future topics, we have designed a second L type matching network for a circuit with $R_S = 20\Omega$, $R_L = 100\Omega$ and $f_o = 10GHz$ using the same methodology as before and same matching network topology (like in figure 2), with quality factor $Q = 2$, inductance $L = 0.7958\,nH$ and capacitance $C = 0.3979\,pF$.

2.2 Bandwidth comparison of matching network topologies

This section will compare the previous circuit bandwidth with new impedance matching networks. Aiming an easy design for these additional networks, we will use the ADS

impedance match tool `Impedance Matching`. The additional networks will obey the specifications below:

- T-network with intermediate impedance $R_i = 1k\omega$;
- T-network with intermediate impedance $R_i = 5k\omega$;
- Low-Q three sections network;

Both the T-networks were designed using two L-network impedance match blocks in a cascade association, carefully choosing the corresponding intermediate impedance of each block to correspond the specification.

It is interesting to see that both intermediate impedances from the T-networks have higher values than input impedance. Also the input impedance is higher than the load impedance. This allow us to analyze that the impedance gain in the L-section close to the load is higher than the other section and the input impedance behaviour is to rise above the desired value and drop to the source impedance. This design pattern can be observed in the figure 9. For a higher bandwidth the designer would want a minimum rise in the impedance in each section that allow a low-Q.

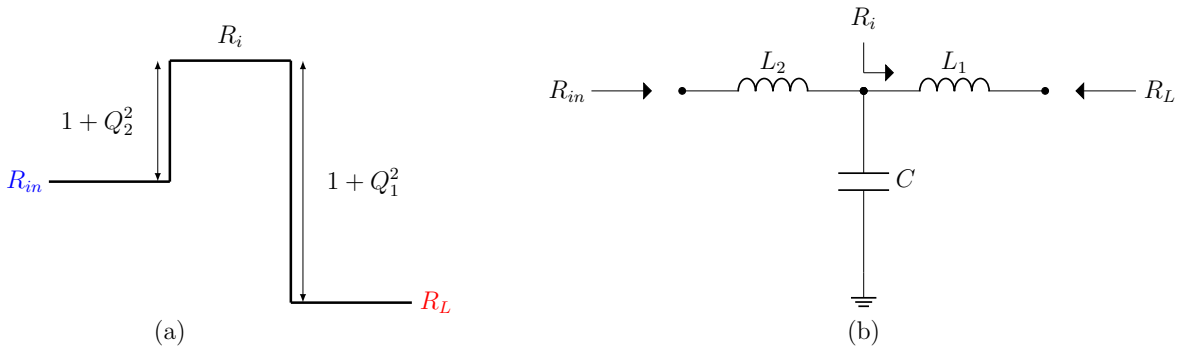


Figure 9: (a) Desired effect of impedance gain(b) T matching network for a serial to parallel transformation of load impedance. Source: own.

The low-Q three sections network is more complex since it has two intermediate impedance and these have to be found to minimize the steps in the input impedance in each given L-network, therefore ensuring the low-Q characteristic. Once we are using the ADS tool for impedance matching, there is only the need to find the set of intermediate impedance.

The overall low-Q three sections network is as seen in figure 10.

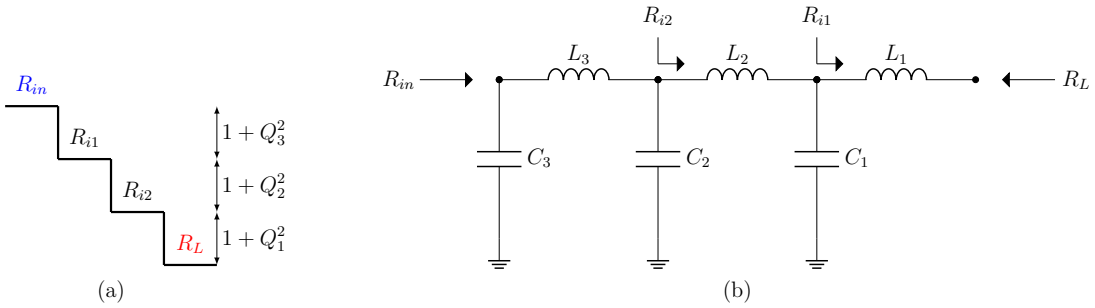


Figure 10: (a) Desired effect of impedance gain(b) Low-Q three sections network. Source: own.

The total gain correspond to the relation between input and output impedance:

$$m_{tot} = \frac{R_{in}}{R_L} = \frac{500}{50} = 10 \tag{11}$$

Once we are using a three section matching network ($n = 3$), the impedance gain in each section will be equal in between them and equal to the cube root of the total gain:

$$m = m_1 = m_2 = m_3 = \sqrt[n]{m_{tot}} = \sqrt[3]{10} = 2.1544 \tag{12}$$

So after each step the corresponding intermediate impedance and, therefore the input impedance will be:

$$\begin{aligned} R_{i1} &= mR_L = 107.72\,\Omega \\ R_{i2} &= mR_{i1} = 232.07\,\Omega \\ R_{in} &= mR_{i2} = 500\,\Omega \end{aligned} \tag{13}$$

The same reasoning can be applied for a matching network of p-th order.

Simulating all four networks together we obtain the graph in the figure 11. The first simulation regarding $S(2,1)$ in a solid red line refers to the first matching network designed in the begin of this problem and it is a L-network. Looking to the two T-networks with different intermediate impedances, one regarding $S(4,3)$ with a dot-dash black line and $R_i = 1k\Omega$ and the another network regarding $S(6,5)$ with a dashed blue line and $R_i = 5k\Omega$. We can see that the T-network insert a degree of freedom to manipulate the quality factor (therefore the bandwidth) without changing the impedance gain. This degree of freedom is does not exist in the L-network, so this topology do not allow a change in the bandwidth without changing the impedance gain.

When we rose the intermediate impedance from $1k\Omega$ to $5k\Omega$ in the T-network the bandwidth of the transmission coefficient became narrow, this is because we rose the quality factor turning the matching network more selective to the desired frequency.

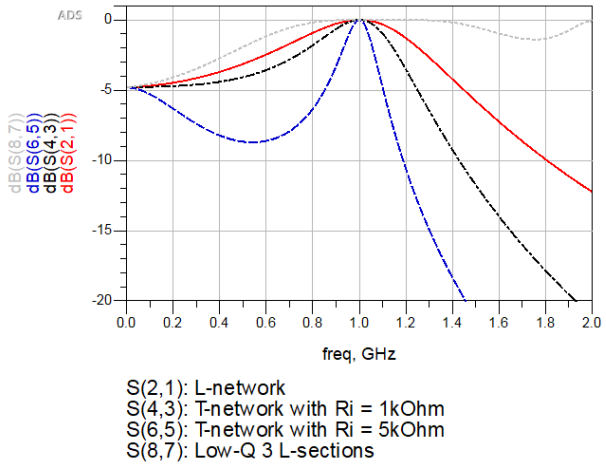


Figure 11: Circuit $R_S = 500\Omega$ and $R_L = 50\Omega$ with four different matching networks.

In the plot for the low-Q three L-sections network, regarding $S(6,5)$ with dotted cyan line, we can see a different effect from the one obtained before rising the intermediate impedances. In this case the bandwidth rose, since we are ensuring a low-Q.

The effect of a large or narrow bandwidth depends on application specifics and how to achieve this bandwidth is a matter of design to choose the ideal matching network topology to ensure a high quality product and lowest cost.