实验 2 带控制端的 8 位运算器设计

一、实验目的

(1) 掌握加法器的设计方法。

(2) 掌握测试文件的设计方法。

(3) 掌握 FPGA 技术的层次化设计方法。

(4) 掌握 FPGA 下载测试方法。

二、实验主要仪器设备

(1) FPGA 实验板

(2) FPGA 实验板配套软件，ModelSim 仿真软件

三、设计任务与要求

1. 基本任务及要求

（1）用 Verilog 设计一个带低有效控制端的一位全加器，再利用级联方法构成带低有效控制端的 8 位加法器。

（2）用 Verilog 测试文件，实现 ModelSim 时序仿真。

（3）根据 FPGA 开发板，配置输入和输出管脚，生成下载文那你件，实现下载测试。

2. 扩展任务及要求

（1）用 Verilog 设计带低有效控制端的 4 位并行进位加法器，再利用层次设计方法构成带低有效控制端的 8 位并行加法器。

（2）用 Verilog 设计加减运算器，通过控制端完成 8 位加法和 8 位减法的转换。

（3）用 Verilog 测试文件，实现 ModelSim 时序仿真。

（4）根据 FPGA 开发板，配置输入和输出管脚，生成下载文件，实现下载测试。

四、实验内容与步骤

1. 基本任务

(1) 带低有效控制端的 1 位全加器

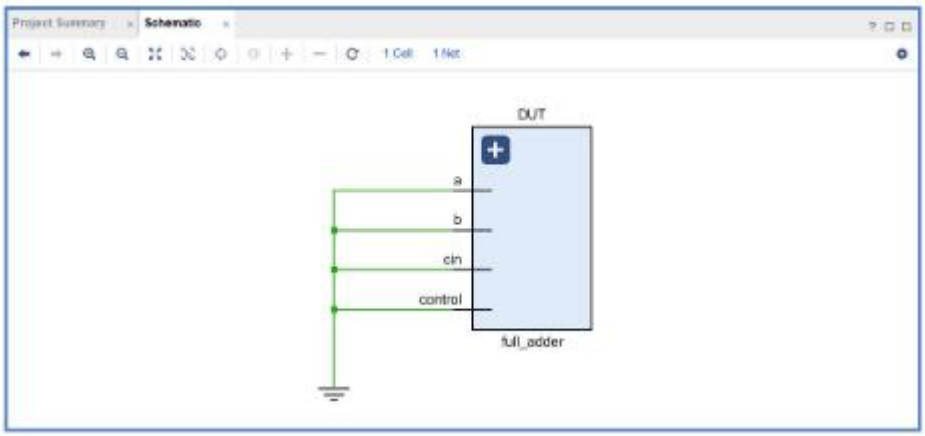
(a) 工作原理

用门电路实现两个二进制数相加并求出和的组合线路，可以处理低位进位，并输出本位加法进位。

(b) Verilog 源程序

```
module full_add(
    input wire Ai,
    input wire Bi,
    input wire Ci,
    input wire E,
    output reg Si,
    output reg Ciout
);
    wire S = Ci ^ Ai ^ Bi;
    wire C = Ai & Bi | (Ai ^ Bi) & Ci;

    always @ (*) begin
        if (E == 1'b0) begin
            Si = S;
            Ciout = C;
        end else begin
            Si = 1'bz;
            Ciout = 1'bz;
        end
    end
endmodule
```

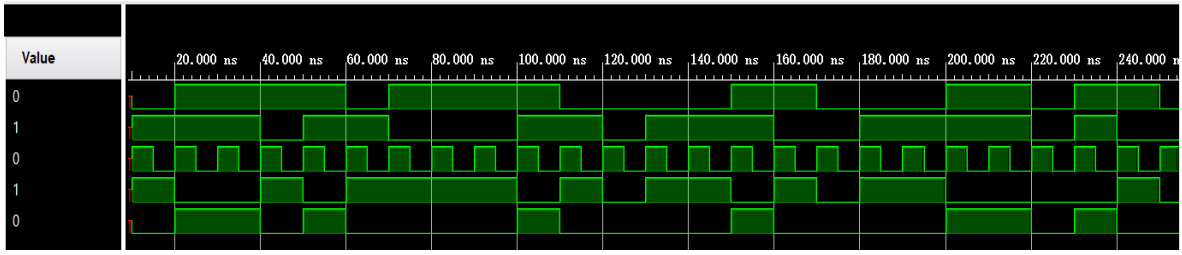
(c) RTL 视图



(d) ModelSim 源程序

```
module add_tb();
reg Ain,Bin;
reg clk;
wire sum1,cout1;
initial
    begin
        #10
        Ain=0;
        Bin=0;
        clk=0;
        end
always #5 clk = ~clk;
always @(posedge clk)
    begin
        Ain={$random}%2;
        Bin={$random}%2;
        end
add u1(.a(Ain),
.b(Bin),
.sum(sum1),
.cout(cout1));
endmodule
```

(d) ModelSim 仿真结果



(e) 下载测试结果

管脚配置

```
set_property -dict {PACKAGE_PIN B24 IOSTANDARD LVCMOS33} [get_ports {Si}]
set_property -dict {PACKAGE_PIN E21 IOSTANDARD LVCMOS33} [get_ports {Ciout}]
set_property -dict {PACKAGE_PIN T3 IOSTANDARD LVCMOS33} [get_ports {Ai}]
set_property -dict {PACKAGE_PIN J3 IOSTANDARD LVCMOS33} [get_ports {Bi}]
set_property -dict {PACKAGE_PIN M2 IOSTANDARD LVCMOS33} [get_ports {Ci}]
set_property -dict {PACKAGE_PIN P1 IOSTANDARD LVCMOS33} [get_ports {E}]
```

(2) 由 1 位全加器级联 8 位加法器

(a) 工作原理

八个一位全加器组级联

(b) Verilog 源程序

```
module full_add(
    input wire Ai,
    input wire Bi,
    input wire Ci,
    input wire E,
    output reg Si,
    output reg Ciout
);
    wire S = Ci ^ Ai ^ Bi;
    wire C = Ai & Bi | (Ai ^ Bi) & Ci;
```

```
    always @ (*) begin
        if (E == 1'b0) begin
            Si = S;
            Ciout = C;
        end else begin
            Si = 1'bz;
            Ciout = 1'bz;
        end
    end
endmodule

module add(
    input wire [7:0] A,
    input wire [7:0] B,
    input wire E,
    input wire C0,
    output wire [7:0] S,
    output wire C8
);
    wire C1, C2, C3, C4, C5, C6, C7;

    full_add f0(
```

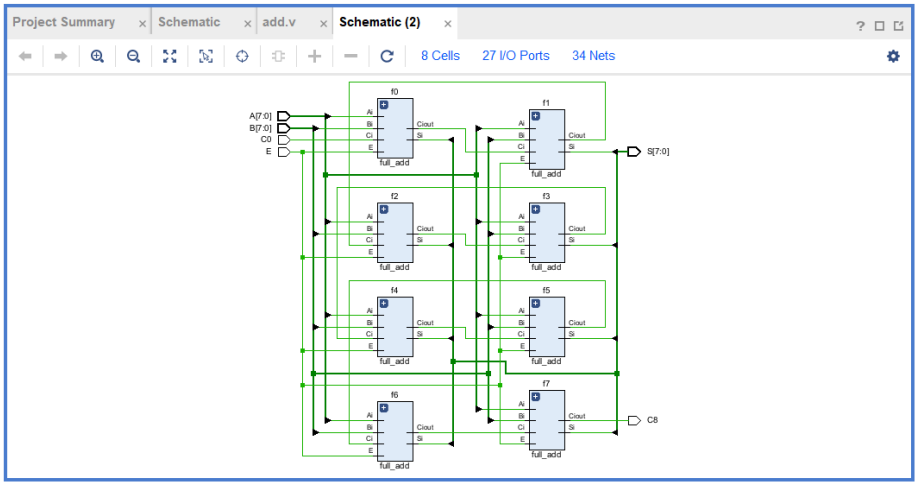
```
        .Ai(A[0]),
        .Bi(B[0]),
        .Ci(C0),
        .E(E),
        .Si(S[0]),
        .Ciout(C1)
);

full_add f1(
        .Ai(A[1]),
        .Bi(B[1]),
        .Ci(C1),
        .E(E),
        .Si(S[1]),
        .Ciout(C2)
);

full_add f2(
        .Ai(A[2]),
        .Bi(B[2]),
        .Ci(C2),
        .E(E),
        .Si(S[2]),
```

```
        .Ciout(C3)
);

full_add f3(
        .Ai(A[3]),
        .Bi(B[3]),
        .Ci(C3),
        .E(E),
        .Si(S[3]),
        .Ciout(C4)
);

full_add f4(
        .Ai(A[4]),
        .Bi(B[4]),
        .Ci(C4),
        .E(E),
        .Si(S[4]),
        .Ciout(C5)
);

full_add f5(
        .Ai(A[5]),
```

```
        .Bi(B[5]),
        .Ci(C5),
        .E(E),
        .Si(S[5]),
        .Ciout(C6)
);

full_add f6(
        .Ai(A[6]),
        .Bi(B[6]),
        .Ci(C6),
        .E(E),
        .Si(S[6]),
        .Ciout(C7)
);

full_add f7(
        .Ai(A[7]),
        .Bi(B[7]),
        .Ci(C7),
        .E(E),
        .Si(S[7]),
        .Ciout(C8)
```

```
    );

endmodule
```

(c) RTL 视图

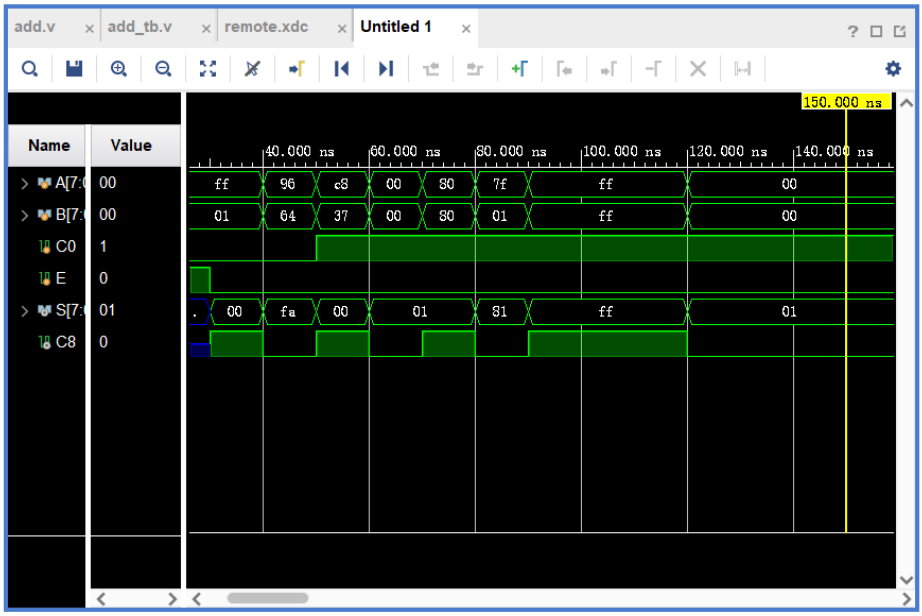


(d) ModelSim 源程序

```
module add_tb;
    reg [7:0] A, B;
    reg C0;
    reg E;
    wire [7:0] S;
    wire C8;

    add uut (
        .A(A),
        .B(B),
        .C0(C0),
        .E(E),
        .S(S),
        .C8(C8)
    );

    initial begin
        E = 1;
        A = 0;
        B = 0;
```

```
        C0 = 0;

        #10 A = 8'd50; B = 8'd70;
        #10 A = 8'd255; B = 8'd1;
        #10 E = 1'b0;
        #10 A = 8'd150; B = 8'd100;
        #10 A = 8'd200; B = 8'd55; C0 = 1'b1;
        #10 A = 8'd0; B = 8'd0;
        #10 A = 8'd128; B = 8'd128;
        #10 A = 8'd127; B = 8'd1;
        #10 A = 8'd255; B = 8'd255;

        #30 A = 1'd0; B = 1'd0;
    end
endmodule
```

(d) ModelSim 仿真结果



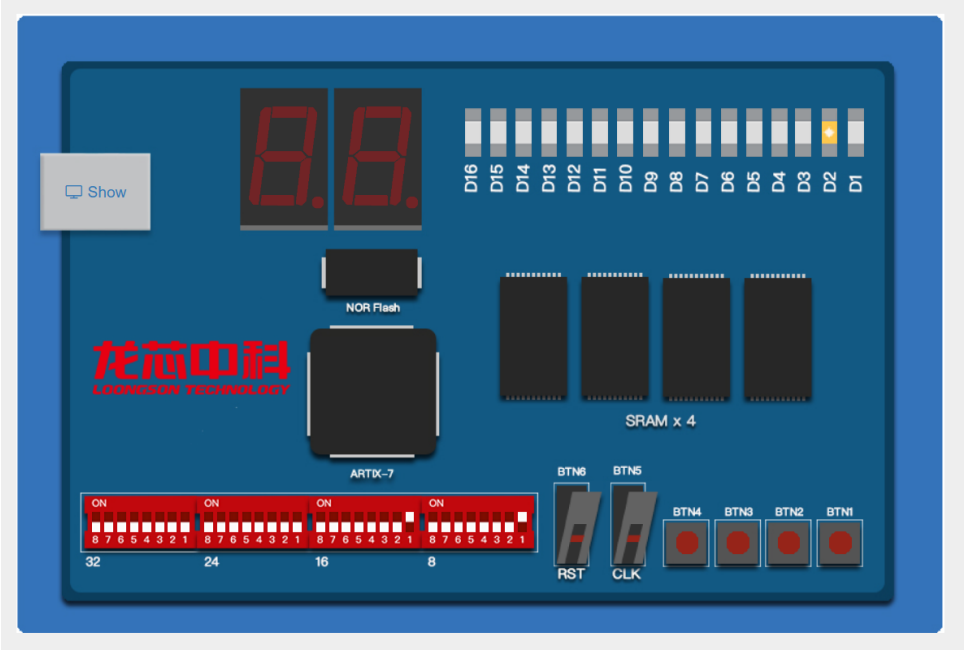
(e) 下载测试结

管脚配置

```
set_property -dict {PACKAGE_PIN B24 IOSTANDARD LVCMOS33} [get_ports {S[0]}]
set_property -dict {PACKAGE_PIN E21 IOSTANDARD LVCMOS33} [get_ports {S[1]}]
set_property -dict {PACKAGE_PIN A24 IOSTANDARD LVCMOS33} [get_ports {S[2]}]
set_property -dict {PACKAGE_PIN D23 IOSTANDARD LVCMOS33} [get_ports {S[3]}]
set_property -dict {PACKAGE_PIN C22 IOSTANDARD LVCMOS33} [get_ports {S[4]}]
```

```
set_property -dict {PACKAGE_PIN C21 IOSTANDARD LVCMOS33} [get_ports {S[5]}]
set_property -dict {PACKAGE_PIN E20 IOSTANDARD LVCMOS33} [get_ports {S[6]}]
set_property -dict {PACKAGE_PIN B22 IOSTANDARD LVCMOS33} [get_ports {S[7]}]
set_property -dict {PACKAGE_PIN C23 IOSTANDARD LVCMOS33} [get_ports {C8}]
set_property -dict {PACKAGE_PIN T3 IOSTANDARD LVCMOS33} [get_ports {A[0]}]
set_property -dict {PACKAGE_PIN J3 IOSTANDARD LVCMOS33} [get_ports {A[1]}]
set_property -dict {PACKAGE_PIN M2 IOSTANDARD LVCMOS33} [get_ports {A[2]}]
set_property -dict {PACKAGE_PIN P1 IOSTANDARD LVCMOS33} [get_ports {A[3]}]
set_property -dict {PACKAGE_PIN P4 IOSTANDARD LVCMOS33} [get_ports {A[4]}]
set_property -dict {PACKAGE_PIN L5 IOSTANDARD LVCMOS33} [get_ports {A[5]}]
set_property -dict {PACKAGE_PIN L3 IOSTANDARD LVCMOS33} [get_ports {A[6]}]
set_property -dict {PACKAGE_PIN N6 IOSTANDARD LVCMOS33} [get_ports {A[7]}]
set_property -dict {PACKAGE_PIN M6 IOSTANDARD LVCMOS33} [get_ports {B[0]}]
set_property -dict {PACKAGE_PIN N7 IOSTANDARD LVCMOS33} [get_ports {B[1]}]
set_property -dict {PACKAGE_PIN M7 IOSTANDARD LVCMOS33} [get_ports {B[2]}]
set_property -dict {PACKAGE_PIN L7 IOSTANDARD LVCMOS33} [get_ports {B[3]}]
set_property -dict {PACKAGE_PIN M5 IOSTANDARD LVCMOS33} [get_ports {B[4]}]
set_property -dict {PACKAGE_PIN K3 IOSTANDARD LVCMOS33} [get_ports {B[5]}]
set_property -dict {PACKAGE_PIN J1 IOSTANDARD LVCMOS33} [get_ports {B[6]}]
set_property -dict {PACKAGE_PIN L2 IOSTANDARD LVCMOS33} [get_ports {B[7]}]
set_property -dict {PACKAGE_PIN K2 IOSTANDARD LVCMOS33} [get_ports {E}]
set_property -dict {PACKAGE_PIN K1 IOSTANDARD LVCMOS33} [get_ports {C0}]
```

测试图



2. 扩展任务

（1）

源程序

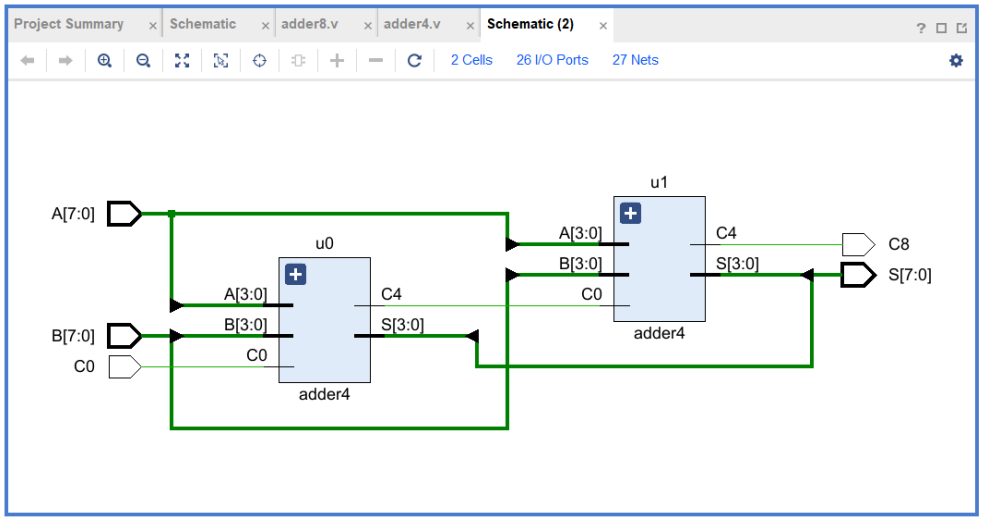
```
module adder4(
    input wire C0,
    input wire [3:0] A,
    input wire [3:0] B,
    output wire C4,
    output wire [3:0] S);
    wire C1,C2,C3;
    wire G0,G1,G2,G3;
    wire P0,P1,P2,P3;
    assign P0=A[0]|B[0];
    assign P1=A[1]|B[1];
    assign P2=A[2]|B[2];
    assign P3=A[3]|B[3];
    assign G0=A[0]&B[0];
    assign G1=A[1]&B[1];
    assign G2=A[2]&B[2];
    assign G3=A[3]&B[3];
    assign C1=G0|(C0&P0);
    assign C2=G1|(C1&P1);
    assign C3=G2|(C2&P2);
    assign C4=G3|(C3&P3);
```

```
    assign S[0]=A[0]^B[0]^C0;
    assign S[1]=A[1]^B[1]^C1;
    assign S[2]=A[2]^B[2]^C2;
    assign S[3]=A[3]^B[3]^C3;
endmodule

module adder8(
    input wire C0,
    input wire [7:0] A,
    input wire [7:0] B,
    output wire [7:0] S,
    output wire C8);
    wire C4,C8;
    adder4 u0(
    .C0(C0),
    .A(A[3:0]),
    .B(B[3:0]),
    .S(S[3:0]),
    .C4(C4));
    adder4 u1(
    .C0(C4),
    .A(A[7:4]),
    .B(B[7:4]),
    .S(S[7:4]),
```

.C4(C8));

Endmodule

RTL 视图



仿真源程序

module add_tb;

reg [7:0] A, B;

reg C0;

reg E;

wire [7:0] S;

wire C8;

add uut (

.A(A),

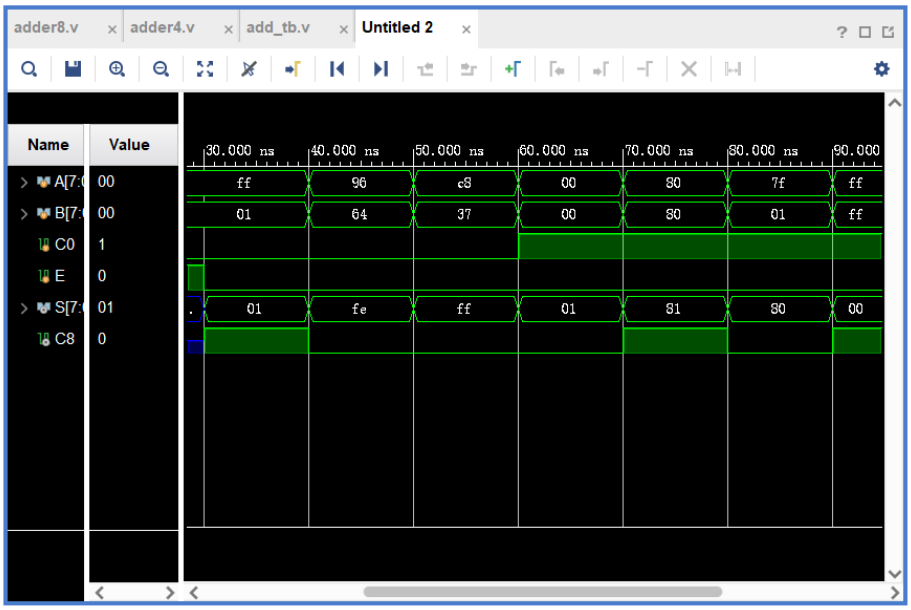
.B(B),

.C0(C0),

.E(E),

```
        .S(S),
        .C8(C8)
    );

    initial begin
        E = 1;
        A = 0;
        B = 0;
        C0 = 0;
        #10 A = 8'd50; B = 8'd70;
        #10 A = 8'd255; B = 8'd1;
        #10 E = 1'b0;
        #10 A = 8'd150; B = 8'd100;
        #10 A = 8'd200; B = 8'd55;
        #10 A = 8'd0; B = 8'd0; C0 = 1;
        #10 A = 8'd128; B = 8'd128;
        #10 A = 8'd127; B = 8'd1;
        #10 A = 8'd255; B = 8'd255;
        #10 A = 1'd0; B = 1'd0;
        #10 $stop;
        end
endmodule
```

仿真截图



管脚配置

#LEDS

set_property -dict {PACKAGE_PIN B24 IOSTANDARD LVCMOS33} [get_ports {S[0]}]

set_property -dict {PACKAGE_PIN E21 IOSTANDARD LVCMOS33} [get_ports {S[1]}]

set_property -dict {PACKAGE_PIN A24 IOSTANDARD LVCMOS33} [get_ports {S[2]}]

set_property -dict {PACKAGE_PIN D23 IOSTANDARD LVCMOS33} [get_ports {S[3]}]

set_property -dict {PACKAGE_PIN C22 IOSTANDARD LVCMOS33} [get_ports {S[4]}]

set_property -dict {PACKAGE_PIN C21 IOSTANDARD LVCMOS33} [get_ports {S[5]}]

set_property -dict {PACKAGE_PIN E20 IOSTANDARD LVCMOS33} [get_ports {S[6]}]

set_property -dict {PACKAGE_PIN B22 IOSTANDARD LVCMOS33} [get_ports {S[7]}]

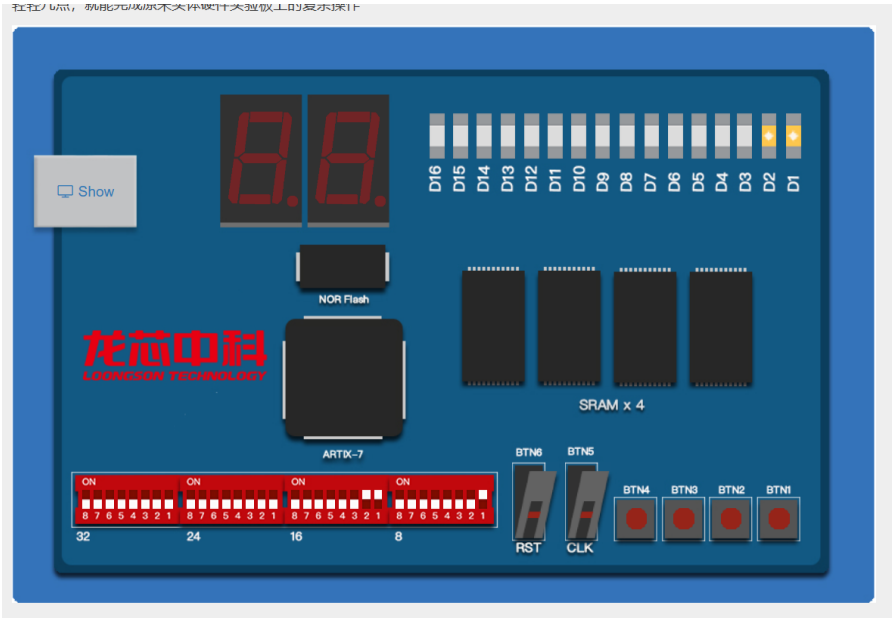
set_property -dict {PACKAGE_PIN C23 IOSTANDARD LVCMOS33} [get_ports {C8}]

#DIP_SW

set_property -dict {PACKAGE_PIN T3 IOSTANDARD LVCMOS33} [get_ports {A[0]}]

```
set_property -dict {PACKAGE_PIN J3 IOSTANDARD LVCMOS33} [get_ports {A[1]}]

set_property -dict {PACKAGE_PIN M2 IOSTANDARD LVCMOS33} [get_ports {A[2]}]

set_property -dict {PACKAGE_PIN P1 IOSTANDARD LVCMOS33} [get_ports {A[3]}]

set_property -dict {PACKAGE_PIN P4 IOSTANDARD LVCMOS33} [get_ports {A[4]}]

set_property -dict {PACKAGE_PIN L5 IOSTANDARD LVCMOS33} [get_ports {A[5]}]

set_property -dict {PACKAGE_PIN L3 IOSTANDARD LVCMOS33} [get_ports {A[6]}]

set_property -dict {PACKAGE_PIN N6 IOSTANDARD LVCMOS33} [get_ports {A[7]}]

set_property -dict {PACKAGE_PIN M6 IOSTANDARD LVCMOS33} [get_ports {C0}]

set_property -dict {PACKAGE_PIN N7 IOSTANDARD LVCMOS33} [get_ports {B[0]}]

set_property -dict {PACKAGE_PIN M7 IOSTANDARD LVCMOS33} [get_ports {B[1]}]

set_property -dict {PACKAGE_PIN L7 IOSTANDARD LVCMOS33} [get_ports {B[2]}]

set_property -dict {PACKAGE_PIN M5 IOSTANDARD LVCMOS33} [get_ports {B[3]}]

set_property -dict {PACKAGE_PIN K3 IOSTANDARD LVCMOS33} [get_ports {B[4]}]

set_property -dict {PACKAGE_PIN J1 IOSTANDARD LVCMOS33} [get_ports {B[5]}]

set_property -dict {PACKAGE_PIN L2 IOSTANDARD LVCMOS33} [get_ports {B[6]}]

set_property -dict {PACKAGE_PIN K2 IOSTANDARD LVCMOS33} [get_ports {B[7]}]

#set_property -dict {PACKAGE_PIN K1 IOSTANDARD LVCMOS33} [get_ports {C0}]
```

测试



（2）

源程序

```
module full_add(
    input wire Ai,
    input wire Bi,
    input wire Ci,
    output reg Si,
    output reg Ciout
);
    wire S = Ci ^ Ai ^ Bi;
    wire C = Ai & Bi | (Ai ^ Bi) & Ci;
    always @ (*) begin
        Si = S;
        Ciout = C;
    end
endmodule
```

```
module add(
    input wire [7:0] A,
    input wire [7:0] B,
    input wire C0,
    output wire [7:0] S,
    output wire C8
);
    wire C1, C2, C3, C4, C5, C6, C7;
    full_add f0(
        .Ai(A[0]),
        .Bi(B[0]),
        .Ci(C0),
        .Si(S[0]),
        .Ciout(C1)
    );
    full_add f1(
        .Ai(A[1]),
        .Bi(B[1]),
        .Ci(C1),
        .Si(S[1]),
        .Ciout(C2)
    );
    full_add f2(
```

```
        .Ai(A[2]),
        .Bi(B[2]),
        .Ci(C2),
        .Si(S[2]),
        .Ciout(C3)
);
full_add f3(
        .Ai(A[3]),
        .Bi(B[3]),
        .Ci(C3),
        .Si(S[3]),
        .Ciout(C4)
);
full_add f4(
        .Ai(A[4]),
        .Bi(B[4]),
        .Ci(C4),
        .Si(S[4]),
        .Ciout(C5)
)
full_add f5(
        .Ai(A[5]),
        .Bi(B[5]),
```

```
        .Ci(C5),
        .Si(S[5]),
        .Ciout(C6)
    );
    full_add f6(
        .Ai(A[6]),
        .Bi(B[6]),
        .Ci(C6),
        .Si(S[6]),
        .Ciout(C7)
    );
    full_add f7(
        .Ai(A[7]),
        .Bi(B[7]),
        .Ci(C7),
        .Si(S[7]),
        .Ciout(C8)
    );
endmodule
module full_sub(
    input wire A,
    input wire B,
    input wire Cin,
```

```
    output reg D,
    output reg Co
);
    always @ (*) begin
        D = A ^ (B ^ Cin);
        Co = ~A & (B ^ Cin) | Cin & B;
    end
endmodule


module sub(
    input wire [7:0] A,
    input wire [7:0] B,
    input wire C0,
    output wire [7:0] D,
    output wire B8
);
    wire B1, B2, B3, B4, B5, B6, B7;
    full_sub s0(
        .A(A[0]),
        .B(B[0]),
        .Cin(C0),
        .D(D[0]),
        .Co(B1)
```

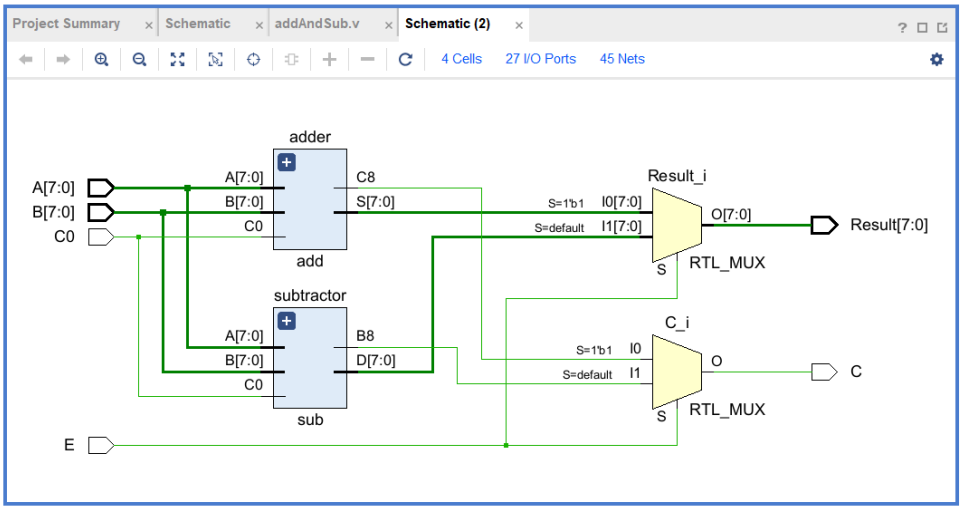
```
);
full_sub s1(
    .A(A[1]),
    .B(B[1]),
    .Cin(B1),
    .D(D[1]),
    .Co(B2)
);
full_sub s2(
    .A(A[2]),
    .B(B[2]),
    .Cin(B2),
    .D(D[2]),
    .Co(B3)
);
full_sub s3(
    .A(A[3]),
    .B(B[3]),
    .Cin(B3),
    .D(D[3]),
    .Co(B4)
);
full_sub s4(
```

```
        .A(A[4]),
        .B(B[4]),
        .Cin(B4),
        .D(D[4]),
        .Co(B5)
    );
    full_sub s5(
        .A(A[5]),
        .B(B[5]),
        .Cin(B5),
        .D(D[5]),
        .Co(B6)
    );
    full_sub s6(
        .A(A[6]),
        .B(B[6]),
        .Cin(B6),
        .D(D[6]),
        .Co(B7)
    );
    full_sub s7(
        .A(A[7]),
        .B(B[7]),
```

```
        .Cin(B7),
        .D(D[7]),
        .Co(B8)
    );
endmodule
module addAndSub(
    input wire [7:0] A,
    input wire [7:0] B,
    input wire E,   // 控制信号，1 表示加法，0 表示减法
    input wire C0,
    output wire [7:0] Result,
    output wire C
);
    wire [7:0] sum;
    wire [7:0] diff;
    wire sum_carry;
    wire borrow;
    add adder(
        .A(A),
        .B(B),
        .C0(C0),
        .S(sum),
        .C8(sum_carry)
```

```
    );

    sub subtractor(

        .A(A),

        .B(B),

        .C0(C0),

        .D(diff),

        .B8(borrow)

    );

    assign Result = (E) ? sum : diff;

    assign C = (E) ? sum_carry : borrow;

endmodule
```

RTL 视图



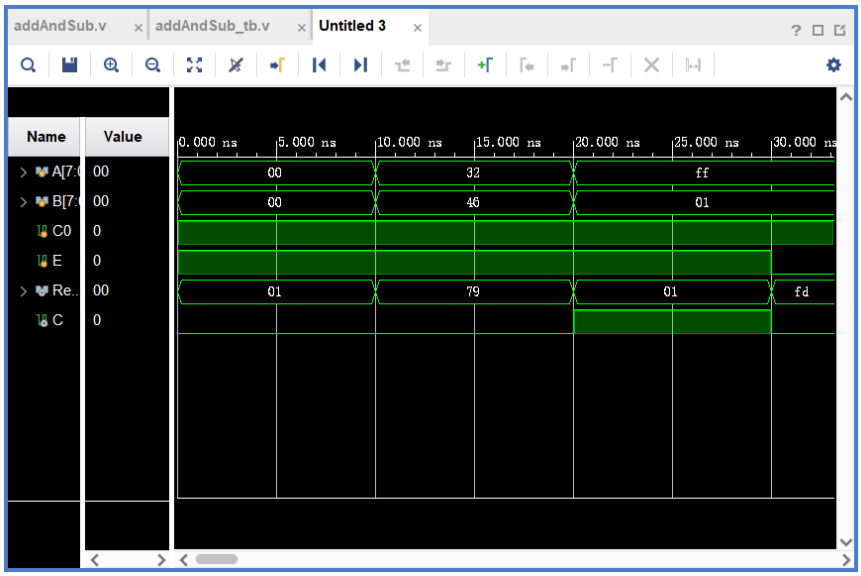
仿真程序

```
module addAndSub_tb;

    reg [7:0] A, B;

    reg C0;
```

```
reg E;

wire [7:0] Result;

wire C;

addAndSub uut (

    .A(A),

    .B(B),

    .C0(C0),

    .E(E),

    .Result(Result),

    .C(C)

);

initial begin

    E = 1;

    A = 0;

    B = 0;

    C0 = 1;

    #10 A = 8'd50; B = 8'd70;

    #10 A = 8'd255; B = 8'd1;

    #10 E = 1'b0;

    #10 A = 8'd150; B = 8'd100;

    #10 A = 8'd200; B = 8'd55;

    #10 A = 8'd0; B = 8'd0; C0 = 0;

    #10 A = 8'd128; B = 8'd128; C0 = 1;
```

```
        #10 A = 8'd127; B = 8'd1;

        #10 A = 8'd255; B = 8'd255;

        #10 A = 1'd0; B = 1'd0;

    end

endmodule
```

仿真截图

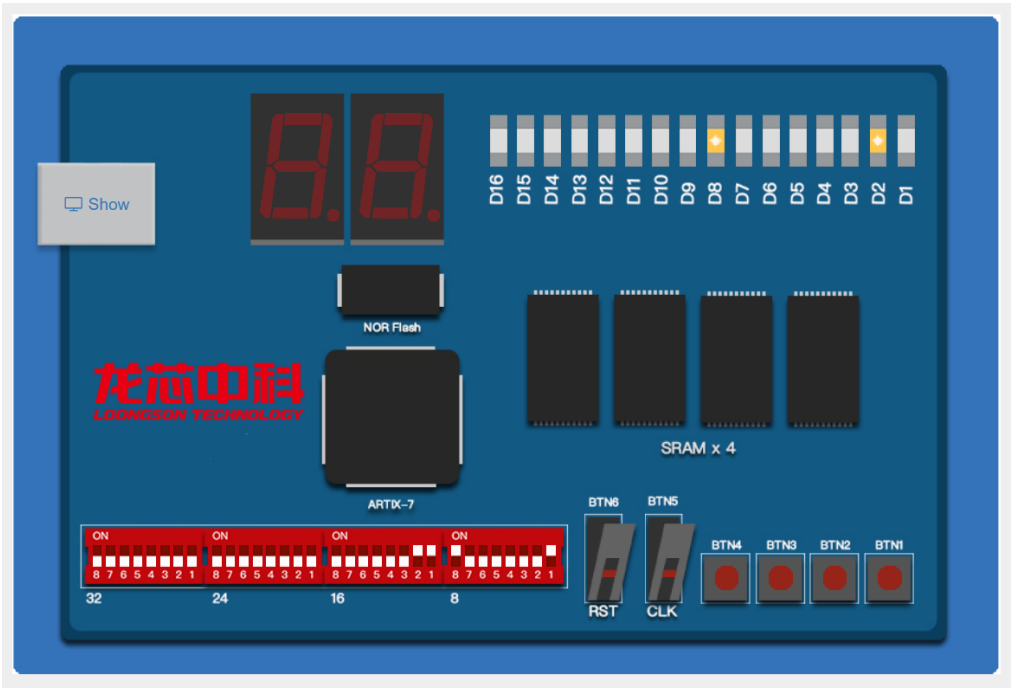


管脚配置

```
#LEDS

set_property -dict {PACKAGE_PIN B24 IOSTANDARD LVCMOS33} [get_ports {Result[0]}]

set_property -dict {PACKAGE_PIN E21 IOSTANDARD LVCMOS33} [get_ports {Result[1]}]

set_property -dict {PACKAGE_PIN A24 IOSTANDARD LVCMOS33} [get_ports {Result[2]}]

set_property -dict {PACKAGE_PIN D23 IOSTANDARD LVCMOS33} [get_ports {Result[3]}]

set_property -dict {PACKAGE_PIN C22 IOSTANDARD LVCMOS33} [get_ports {Result[4]}]

set_property -dict {PACKAGE_PIN C21 IOSTANDARD LVCMOS33} [get_ports {Result[5]}]

set_property -dict {PACKAGE_PIN E20 IOSTANDARD LVCMOS33} [get_ports {Result[6]}]
```

```
set_property -dict {PACKAGE_PIN B22 IOSTANDARD LVCMOS33} [get_ports {Result[7]}]

set_property -dict {PACKAGE_PIN C23 IOSTANDARD LVCMOS33} [get_ports {C}]

#DIP_SW

set_property -dict {PACKAGE_PIN T3 IOSTANDARD LVCMOS33} [get_ports {A[0]}]

set_property -dict {PACKAGE_PIN J3 IOSTANDARD LVCMOS33} [get_ports {A[1]}]

set_property -dict {PACKAGE_PIN M2 IOSTANDARD LVCMOS33} [get_ports {A[2]}]

set_property -dict {PACKAGE_PIN P1 IOSTANDARD LVCMOS33} [get_ports {A[3]}]

set_property -dict {PACKAGE_PIN P4 IOSTANDARD LVCMOS33} [get_ports {A[4]}]

set_property -dict {PACKAGE_PIN L5 IOSTANDARD LVCMOS33} [get_ports {A[5]}]

set_property -dict {PACKAGE_PIN L3 IOSTANDARD LVCMOS33} [get_ports {A[6]}]

set_property -dict {PACKAGE_PIN N6 IOSTANDARD LVCMOS33} [get_ports {A[7]}]

set_property -dict {PACKAGE_PIN M6 IOSTANDARD LVCMOS33} [get_ports {E}]

set_property -dict {PACKAGE_PIN N7 IOSTANDARD LVCMOS33} [get_ports {B[0]}]

set_property -dict {PACKAGE_PIN M7 IOSTANDARD LVCMOS33} [get_ports {B[1]}]

set_property -dict {PACKAGE_PIN L7 IOSTANDARD LVCMOS33} [get_ports {B[2]}]

set_property -dict {PACKAGE_PIN M5 IOSTANDARD LVCMOS33} [get_ports {B[3]}]

set_property -dict {PACKAGE_PIN K3 IOSTANDARD LVCMOS33} [get_ports {B[4]}]

set_property -dict {PACKAGE_PIN J1 IOSTANDARD LVCMOS33} [get_ports {B[5]}]

set_property -dict {PACKAGE_PIN L2 IOSTANDARD LVCMOS33} [get_ports {B[6]}]

set_property -dict {PACKAGE_PIN K2 IOSTANDARD LVCMOS33} [get_ports {B[7]}]

set_property -dict {PACKAGE_PIN K1 IOSTANDARD LVCMOS33} [get_ports {C0}]
```

测试


Show
D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1
NOR Flash
龙芯中科
LOONGSON TECHNOLOGY
SRAM x 4
ARTIX-7
ON
8 7 6 5 4 3 2 1
32 24 16 8
BTN6 BTN5 BTN4 BTN3 BTN2 BTN1
RST CLK

五、实验过程中出现的故障现象、原因分析及解决的办法

加法器最高位进位设置有误，导致溢出出现错误结果，设置最高位进位标志，处理溢出情况。