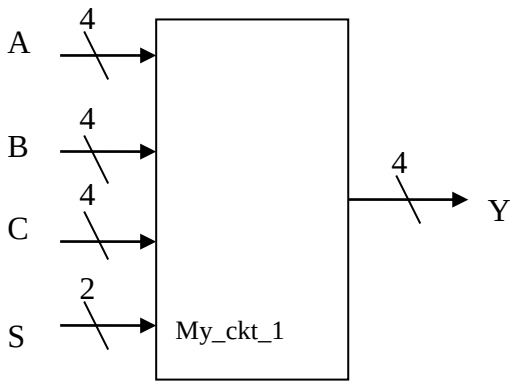
Homework 1
Due Day: 11/13

Consider a system consisting of 4 input ports and 1 output port as shown below.




In the system, the 4 input ports are denoted by A, B, C and S, respectively. Let A={A3,A2,A1,A0}, B={B3,B2,B1,B0}, C={C3,C2,C1,C0}, and S={S1,S0}. The output port is denoted by Y={Y3,Y2,Y1,Y0}. The input port S determines the mode of the operations. There are 4 modes in the system. The following table shows the operations of each mode.

| Mode | Operations |
|---|---|
| Mode 1 (S={S1,S0}={0,0}) | Yi=Ai OR Bi, i=3,2,1,0. |
| Mode 2 (S={S1,S0}={0,1}) | Y= max{A,B,C} |
| Mode 3 (S={S1,S0}={1,0}) | Y= A*B |
| Mode 4 (S={S1,S0}={1,1}) | Y=A+C |

For modes 2, 3 and 4, inputs A, B, and C are treated as unsigned integers.

Write a VHDL code to implement the system using Quartus II. Your project report should include the following items.

1. the Quartus II project file containing the VHDL code of the system,
2. the word files containing the simulation results and the corresponding discussions.

Hint: Please use data type UNSIGNED for signals A, B, C, S and Y.

Reference output:

(此結果僅為參考範例，同學的輸入輸出可能與下圖不同。)