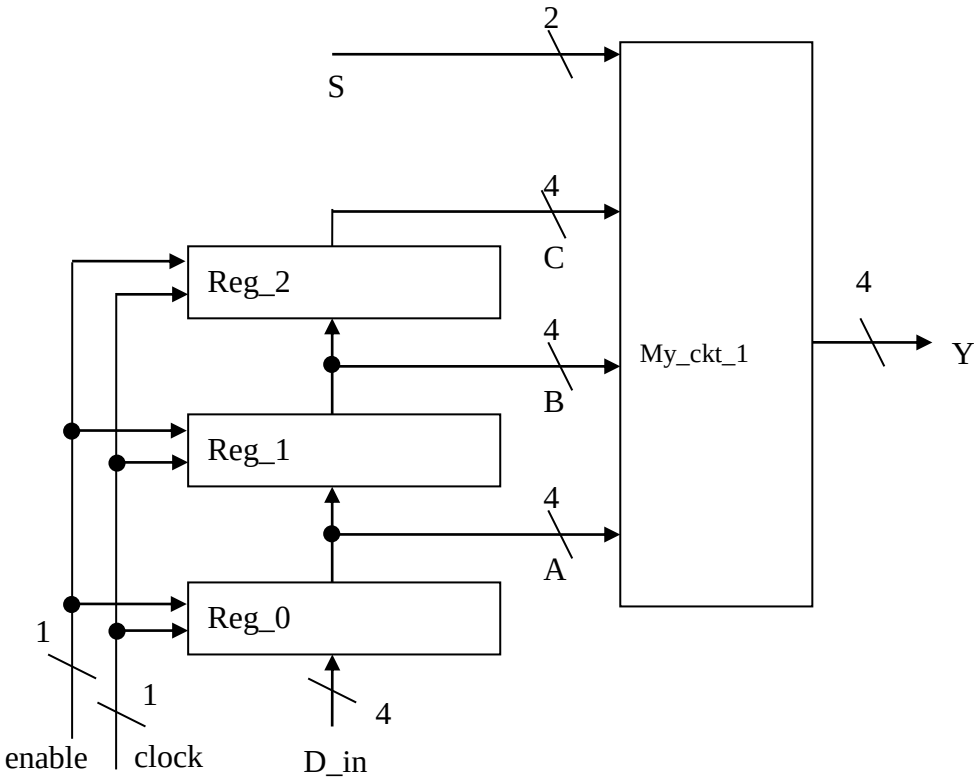
Homework 2
Due Day: 12/11

Consider a shift register based system shown below. It contains four input ports (S, clock, enable, and D_in) and one output port (Y). The shift register in the circuit consists of three stages.



The circuit with entity name My_ckt_1 is the circuit we have implemented in HW1. The functions of the My_ckt_1 can be summarized in the following table.

Mode	Operations
Mode 1 (S={S1,S0}={0,0})	Yi=Ai OR Bi, i=3,2,1,0.
Mode 2 (S={S1,S0}={0,1})	Y= max{A,B,C}

Mode 3 (S={S1,S0}={1,0})	Y= A*B
Mode 4 (S={S1,S0}={1,1})	Y=A+C

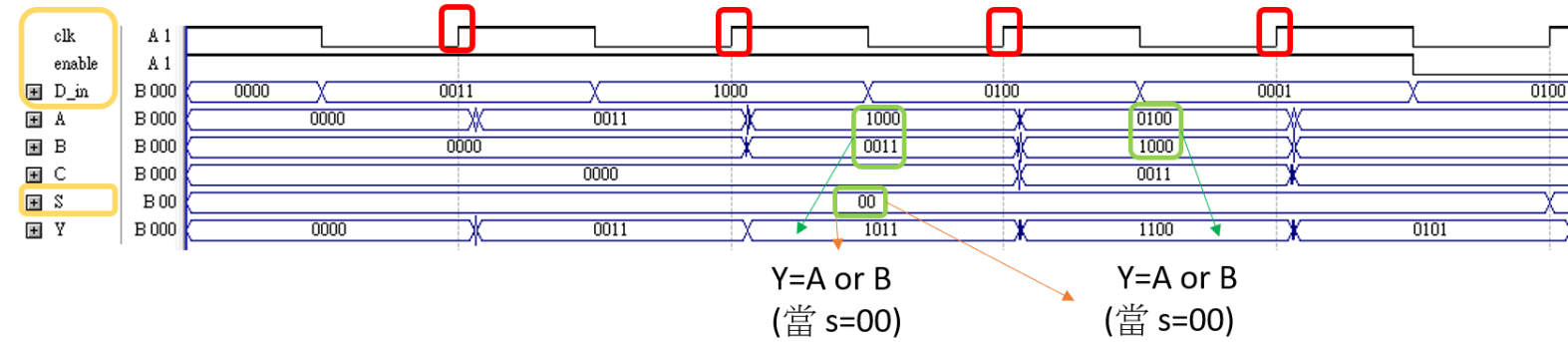
Write a VHDL code to implement the system using Quartus II. Your project report should include the following items.

1. the Quartus II project file containing the VHDL code of the system,
2. the word files containing the simulation results and the corresponding discussions.

Reference output:
(此結果僅為參考範例，同學的輸入輸出可能與下圖不同。)

自行設定的輸入值

當 rising edge 且 enable為 1 時，D_in才進行位移。



輸出有延遲雜訊為正常現象。

自行設定的輸入值