VLSI Homework #4
Due Day: 01/15/2021

The goal of this homework is to design a traffic light control circuit as shown below. As shown in Figure 1, the circuit consists of a controller and a counter.

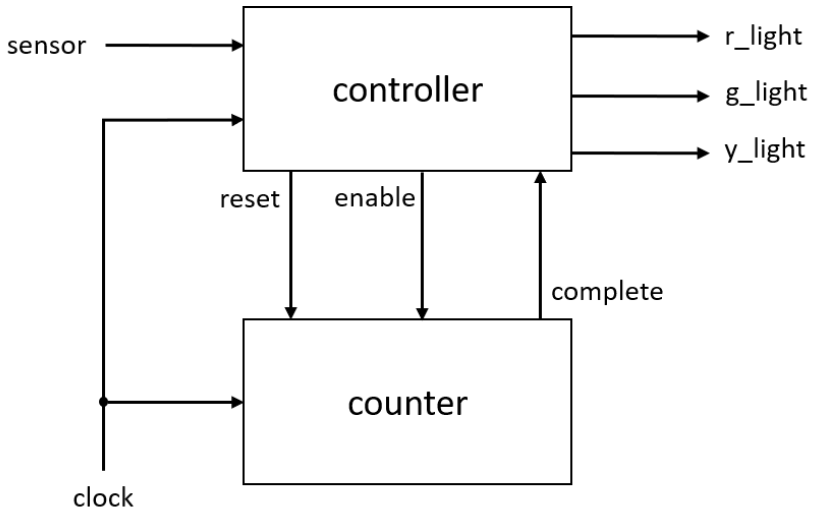

Figure 1. The architecture of the traffic light control circuit.

The ASM chart of the controller is shown in Figure 2. The controller has three states: red, green and yellow. When the controller in red state, it turns on r_light (r_light=1), and resets the counter (reset=1). The controller stays in the red state until sensor input becomes 1. After that, the controller enters the green state, which turns on g_light (g_light=1) and enables the counter (enable=1). After the counting operation is completed (complete=1), the controller then enters yellow state. In the yellow state, the controller turns on y_light (y_light=1), and then returns to red state.

The counter performs up counting operations. It will be reset as 0 when reset=1. When reset=0 and enable=1, the counter will increase its counting value by 1 on the rising edge of the clock. When counting value reaches the maximum value, the complete=1.

(a) Implement the traffic light controller by VHDL.
(b) (Optional) Implement the traffic light controller by Verilog.

Your project report should include the Quartus II project file containing the codes of the system.

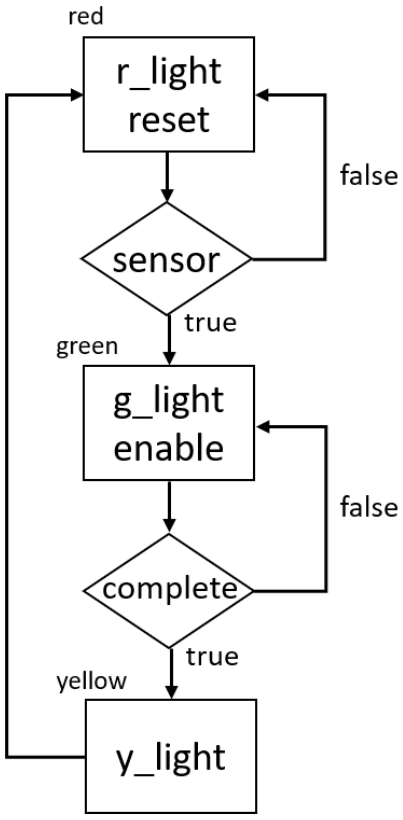

Figure 2. The ASM chart of the controller.

配分方式：

1. **設計中包含 controller 和 counter**（如題目要求和範例所示），VHDL 的設計配分上限為 100 分，optional 的 Verilog 設計最多加分 50 分，因此分數總上限為 **150 分**。

2. **設計中只有 controller，不包含 counter**（即綠燈只持續 1 個 clock 就變成黃燈）。VHDL 的設計配分上限為 80 分，optional 的 Verilog 設計最多加 40 分，因此分數總上限為 **120 分**。

	只寫 VHDL	寫 VHDL 加 Verilog
有 controller 和 counter	上限 100 分	上限 150 分
只有 controller 沒有 counter	上限 80 分	上限 120 分

Reference output:
(此結果僅為參考範例，同學的輸入輸出可能與下圖不同。)