Optimised Microprocessor Architecture Design for Machine Learning Applications

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The project presents a five-stage pipelined RISC-V CPU design with custom instructions—namely ReLU, vector addition, and matrix multiplication—to accelerate convolutional neural network (CNN) inference computations. Implemented in Verilog and verified via ModelSim simulation, the processor architecture consists of the classic pipeline stages—Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory (MEM), and Write Back (WB)—together with pipeline registers between stages. Techniques such as data forwarding and pipeline stalling are employed to address common hazards and ensure correct execution in the presence of instruction dependencies. Fixed-point arithmetic is used in place of floating-point for CNN acceleration, balancing resource limits and efficiency on FPGAs. To validate matrix multiplication accuracy and pipeline performance, I incorporated CNN-trained data: a larger file of more than 200 lines was generated by a TensorFlow-based CNN, from which only the first 64 lines (each 8 bits wide) were transformed into a `hex` file for final testing in the ALU-based design. Both single-cycle and pipelined implementations produce matching outputs, verifying correctness, while the pipelined CPU demonstrates significantly better performance in cycle count reduction. Although future work may explore hardware-level deployment (e.g., on a DE10-Nano FPGA), the current results already affirm the feasibility and scalability of this approach for CNN-focused computations under resource-conscious environments.

1 Introduction and Literature Review

1.1 Microprocessors and Motivation

The evolution of microprocessors can be traced back to the late 1960s, when rapid advancements in integrated circuit (IC) technology made it possible to integrate the core functions of a computer onto a single chip. In 1971, Intel introduced the world's first commercial microprocessor—the Intel 4004. Although the 4004 was merely a 4-bit processor, its development ushered in the microprocessor era, proving that a computer's essential functions could be consolidated into one compact IC. Following this breakthrough, Intel released the 8-bit 8008 and the 16-bit 8080 processors, both of

which propelled the computer industry forward and laid the groundwork for embedded systems and industrial automation [1].

As IC manufacturing technology improved, microprocessors underwent a significant qualitative leap. In 1978, Intel launched the 8086 processor, heralding the birth of the x86 architecture [2]. Renowned for its strong backward compatibility and versatile design, the x86 architecture rapidly became the dominant force in personal computing, evolving through various iterations such as the 80286, 80386, and the Pentium series. Beyond desktop computing, x86 also established its presence in servers and workstations. Meanwhile, in the 1980s, Acorn Computers in the United Kingdom introduced the ARM architecture. In contrast to x86, ARM embraced a Reduced Instruction Set Computing (RISC) philosophy emphasizing low power consumption and high efficiency, making it particularly well-suited for embedded devices. ARM's proliferation tracked the meteoric rise of mobile computing, propelling ARM cores into dominance for smartphones and other portable electronics. This rapid expansion fostered a paradigm shift in the microprocessor industry, elevating power and energy efficiency to a primary concern.

Beyond x86 and ARM, other RISC-based architectures—MIPS and PowerPC—also emerged, each with its own performance and power advantages [1]. MIPS processors, known for high performance and energy efficiency, found widespread use in embedded applications, while PowerPC was initially integral to Apple computers and numerous embedded systems. In many cases, these architectures supported high-performance servers on one hand and power-critical embedded systems on the other.

Entering the 21st century, microprocessors have tended toward multicore designs and system-on-chip (SoC) solutions [1]. Contemporary devices often integrate traditional CPU cores with specialized accelerators, such as Graphics Processing Units (GPUs), Digital Signal Processors (DSPs), and AI accelerators, to address specific performance bottlenecks through parallelism [1]. Techniques like pipelining, superscalar execution, and out-of-order processing further exploit concurrency to deliver higher instruction throughput.

From a personal perspective, the rapid evolution of microprocessors is not only a technological feat but also reflects humankind's unceasing pursuit of more efficient data handling and more seamless integration into everyday life. Whether in the high-performance CPUs powering modern servers or the energy-efficient ARM chips fueling smartphones, microprocessors continue to serve as the engine of digital transformation. With the explosive growth of the Internet of Things (IoT), big data, and artificial intelligence, microprocessors will likely evolve into ever more intelligent, efficient, and tightly integrated systems, lighting the path to an even more ubiquitously networked

and data-driven future [1].

Table 1: Comparison of Microprocessor Architectures

	x86	**ARM**	**RISC (e.g., MIPS, PowerPC)**
Origin	Developed by Intel (and AMD)	Developed by Acorn Computers / ARM Ltd.	Based on RISC principles
Design Philosophy	CISC (Complex Instruction Set Computing)	RISC with emphasis on power efficiency	Pure RISC design
Applications	Desktops, laptops, servers, workstations	Mobile devices, embedded systems, IoT	Embedded systems, specialized HPC
Evolution	Multicore and SoC designs	Dominant in mobile computing	Used in customizable, open-source solutions

A single-cycle microprocessor completes each instruction in a single clock cycle. That is, instruction fetch, decoding, execution, memory access, and result write-back occur within one clock cycle [3]. While appealing for its simplicity and straightforward control design, a single-cycle approach must elongate its clock period to accommodate the slowest instruction, thus limiting the maximum clock frequency. The result is an educationally friendly but performance-constrained architecture.

Although single-cycle processors logically move through these five steps (IF, ID, EX, MEM, WB), each instruction consumes the entire clock cycle in sequence rather than being overlapped in hardware. This design often requires more routing, multiplexers, and dedicated combinational logic than a multi-cycle or pipelined equivalent, because each instruction path must be handled within that single cycle.

In contrast, a pipelined microprocessor divides execution into multiple stages so that multiple instructions can be processed simultaneously. Borrowing the idea of an industrial assembly line, pipeline stages (IF, ID, EX, MEM, WB) are implemented with distinct hardware units, allowing subsequent instructions to be fetched as the first moves on to later stages [3]. This concurrent activity can significantly boost throughput and effectively decrease the average clock cycles per instruction, although it introduces complexities such as data hazards and control hazards. These hazards must be handled via data forwarding, pipeline stalling, and branch prediction, among other techniques.

In a five-stage pipelined processor, each instruction ideally advances one pipeline stage per clock cycle. Hence, after a short initial delay (the pipeline fill time), the

processor can complete one instruction per cycle. The real-world performance gains, however, are slightly lower than this ideal due to hazards. Even so, pipelining is a fundamental approach to achieve higher performance in modern CPU designs.

1.2 RISC-V Instruction Set Architecture(ISA)

RISC-V is a Reduced Instruction Set Computer (RISC) architecture originally developed at the University of California, Berkeley, and is distinguished by its open, modular, and extensible nature [4, 2]. Unlike proprietary architectures like x86 or ARM, RISC-V's specifications are publicly available, thus allowing both academic and industrial entities to tailor and extend the instruction set as needed [5].

In RISC-V, every basic instruction is encoded in a fixed 32-bit format. Taking the R-type instruction as an example, its format comprises a 7-bit opcode, a 5-bit destination register (`rd`), a 3-bit function field (`funct3`), a 5-bit first source register (`rs1`), a 5-bit second source register (`rs2`), and a 7-bit additional function field (`funct7`). The `funct7` field further distinguishes variants of an operation (for example, `add` vs. `sub`), while `funct3` pinpoints the exact operation type [2]. Other instruction formats include I-type, S-type, B-type, U-type, and J-type, each bringing different forms of immediate fields to support arithmetic with constants, data load/store, and branching operations. During program execution, the CPU fetches the 32-bit binary instruction from memory, decodes its opcode and function fields to generate the needed control signals for the ALU and other CPU components, and then proceeds through memory access and write-back to retire the instruction [1].

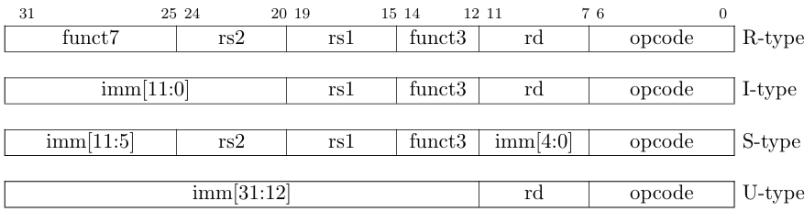


Figure 1: RISC-V base instruction formats [5]

A significant advantage of RISC-V is its simple but flexible foundation, which supports a base integer instruction set (e.g., RV32I or RV64I) that can be expanded with specialized extensions [6]. For example, in this project, custom instructions were implemented to handle matrix multiplication, vector addition, and ReLU activation for CNN inference tasks. Leveraging reserved opcode fields or reassigning specific bits in the instruction format, one can integrate new operations into the decode and execution

units, thus accelerating specialized workloads.

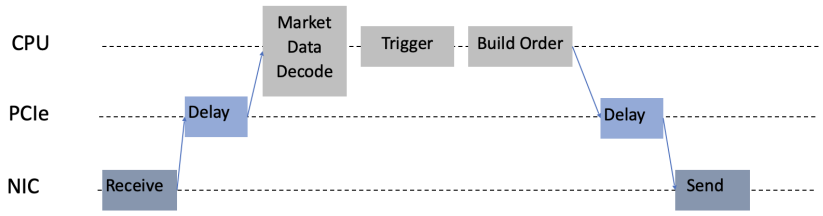
1.3 Literature Review

1.3.1 Applications

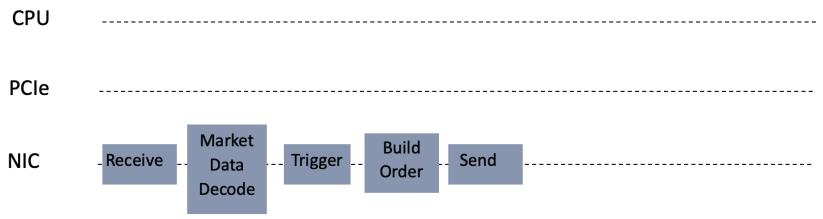
Field-Programmable Gate Arrays (FPGAs), the RISC-V ISA, and machine learning have intersected significantly over the past few decades, giving rise to reconfigurable, energy-efficient, and high-performance computing platforms for AI acceleration. FPGAs originated in the mid-1980s as a solution to the high non-recurring engineering costs of ASICs. Early FPGAs offered limited capabilities, but successive generations integrated sophisticated DSP blocks, large on-chip memories, and high-speed transceivers, transforming them into powerful reconfigurable platforms that now underpin a variety of commercial and research applications [7]. Since 2010, RISC-V has brought an open, modular ISA that can be customized without licensing fees. Its lightweight base instruction set, expanded as needed, allows for an elegant co-design of hardware and software, well matched to the parallel computing strengths of modern FPGAs. With the rise of machine learning—particularly deep learning using CNNs— the need for hardware that can handle large, complex datasets with high throughput and low latency has grown dramatically.

In finance, FPGAs are heavily employed in latency-sensitive tasks such as high-frequency trading, where every nanosecond is critical. By processing entire order flows directly on an FPGA-based NIC (Network Interface Card), data transfers through PCIe and CPU layers are minimized [8]. Figure 2a shows the conventional software-only pipeline, while Figure 2b depicts a more efficient FPGA-centric approach. By eliminating round trips to the CPU for market data and order construction, FPGA solutions reduce total latency and enable more deterministic behavior—key advantages in automated trading strategies.

In industrial control, FPGAs power real-time systems that demand deterministic responses and robust fault tolerance [9]. They are employed in sensor fusion, motor control, and signal filtering under harsh factory conditions. By embedding RISC-V cores alongside FPGA logic, manufacturers can combine high-level control tasks running on RISC-V with time-critical tasks implemented directly in hardware [10], reducing latency and boosting reliability. This hybrid approach is especially valuable in areas like robotics, where low-latency data analysis from LiDAR or stereo vision sensors enables



(a) Software only execution system



(b) FPGA NIC execution system

Figure 2: Comparison of software and FPGA [8]

instantaneous path planning and obstacle avoidance.

Similarly, aerospace and automotive industries rely on FPGA-based systems for onboard data processing. For instance, autonomous driving systems often merge inputs from cameras, radars, and LiDAR, requiring high-throughput hardware that can accomplish sensor fusion in real time. Integrating an open and extensible RISC-V core on the same FPGA platform provides a flexible control layer for advanced driver-assistance systems and safe automotive computation [11].

FPGA technology has also become a key enabler for bridging high-performance computing with real-time data acquisition in industrial and medical applications. Figure 3 shows a typical architecture where FPGA modules interface with industrial computers via CompactPCI buses. This approach allows multi-channel data acquisition, high-speed signal processing, and local acceleration for computationally expensive operations like CNN-based inspection [12]. In medical imaging, FPGAs enhance reconstruction algorithms for MRI, CT, and ultrasound by exploiting massive parallelism to reduce latency and boost throughput. Integration with a RISC-V control core offers a unified hardware/software environment to coordinate resources and manage communication among various subsystems, thereby improving overall diagnostic accuracy [13].

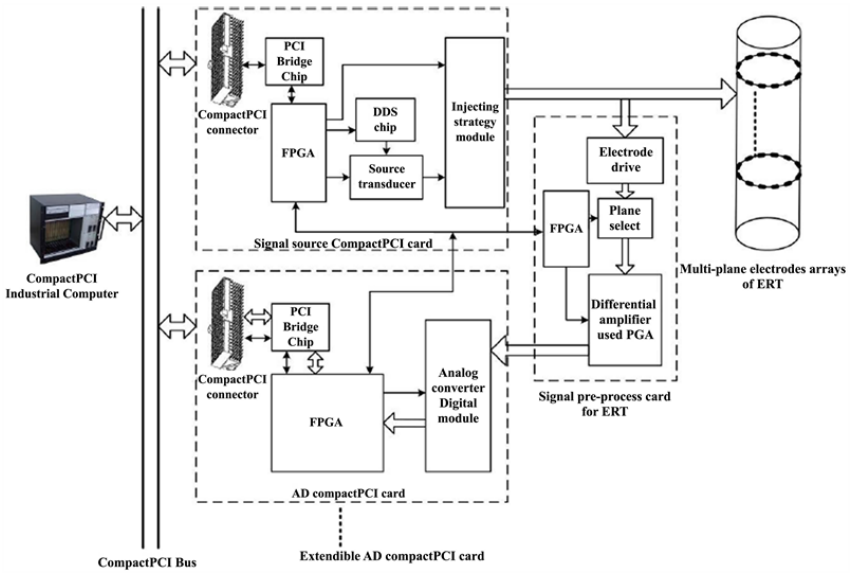


Figure 3: Architecture of the DAS based on CompactPCI Bus and FPGA [12]

1.3.2 Conclusion

From the initial emergence of microprocessors and their subsequent evolution into multicore, SoC, and domain-specific accelerators, it is evident that modern computing must efficiently balance performance, power, and flexibility. The open and extensible nature of RISC-V, paired with the reconfigurability of FPGAs, creates a powerful synergy—especially for computationally intensive tasks such as CNN inference. Recent industry applications, spanning finance, industrial control, robotics, and aerospace, underscore how FPGA-accelerated RISC-V solutions can simultaneously provide low latency, high throughput, and scalable hardware integration. Against this backdrop, our

project leverages a pipelined RISC-V CPU design enhanced with custom instructions tailored for CNN acceleration. By comparing single-cycle and pipelined implementations, I aim to demonstrate substantial performance gains in terms of reduced CPI and overall instruction throughput. The following sections detail our architectural choices, methodology, and experimental validations that reinforce the viability and adaptability of this FPGA-based RISC-V design.

1.4 Goals and Objectives

Goals

- **Develop a CNN-Oriented Five-Stage Pipelined RISC-V CPU:**
  Create a Verilog-based, five-stage pipeline (IF, ID, EX, MEM, WB) that can be seamlessly extended with custom instructions for Convolutional Neural Network (CNN) tasks. The overarching goal is to confirm that such a pipeline architecture can balance efficiency and correctness, even under data-intensive workloads.

- **Enhance Execution Through Custom Instructions:**
  Integrate specialized operations (e.g., matrix multiplication, vector addition, ReLU activation) into the RISC-V ISA. Demonstrate that incorporating these instructions can significantly reduce cycle counts for typical CNN inference tasks, while preserving baseline RISC-V compatibility.

- **Facilitate CNN-Driven Validation:**
  Employ real data from a trained CNN model—selecting a 64-line subset from a larger weight file—to test matrix-multiplication accuracy in both single-cycle and pipelined CPU variants. Show that the pipeline approach not only preserves correctness but also boosts performance in cycle count reduction.

- **Lay the Foundation for Future FPGA Deployment:**
  Although hardware implementation is deferred to future work, ensure that pipeline organization, fixed-point arithmetic, and hazard-handling strategies are readily transferable to an FPGA board (e.g., DE0-Nano). This establishes a blueprint for potential real-time neural-network acceleration in resource-constrained systems.

Objectives

- **Objective 1: Pipeline Construction and Hazard Mitigation**
  Partition the CPU into five well-defined pipeline stages and implement robust forwarding and stalling mechanisms. Verify—through functional simulation—that data and control hazards do not compromise correctness.

- **Objective 2: Implementation of CNN-Focused Instructions**
  Extend the base RISC-V ISA with instructions for matrix multiplication, vector addition, and ReLU operations. Formally define each instruction's opcode, operand usage, and modifications in the EX/MEM pipeline stages.

- **Objective 3: Comparative Testing with Single-Cycle Architecture**
  Construct a simpler single-cycle RISC-V processor as a performance baseline. Use identical CNN data inputs (converted into a 64-line `hex` file) to compare cycle counts, correctness, and simulated resource usage against the pipelined implementation.

- **Objective 4: Simulation and Verification of `hex` Data Processing**
  Incorporate the 64-line CNN-trained dataset into the test environment. Confirm both CPU versions produce matching outputs, and quantify the pipelined CPU's speedup versus the single-cycle reference when running the same CNN-focused instructions.

- **Objective 5: Establish a Pathway for Future Hardware Integration**
  Summarize design considerations for eventual FPGA-based deployment—e.g., clock frequency targets, memory interface design, and handling of fixed-point arithmetic for larger CNN workloads. Provide guidelines on how to extend this approach to additional custom instructions or more advanced CNN models.

2 Theoretical Background

This section presents three essential hardware modules in a RISC-V processor design: the Arithmetic Logic Unit (ALU), the Register File, and the Data Memory. I illustrate each module's conceptual schematic, a corresponding Verilog code snippet (shown as images), and the simulation waveforms that confirm correct functionality. In the following subsections, I highlight the main design principles rather than full code listings, focusing on how these components operate and interact.

2.1 Arithmetic Logic Unit (ALU)

2.1.1 ALU Structure and Code Overview

Figure 4 depicts a typical ALU schematic with two 32-bit inputs (`SrcA`, `SrcB`), a 3-bit control signal (`ALUControl`), and outputs `ALUResult` plus a `Zero` flag. When `ALUControl` indicates an arithmetic or logical operation (e.g., ADD, SUB, AND, OR, SLT), the ALU processes `SrcA` and `SrcB` accordingly.

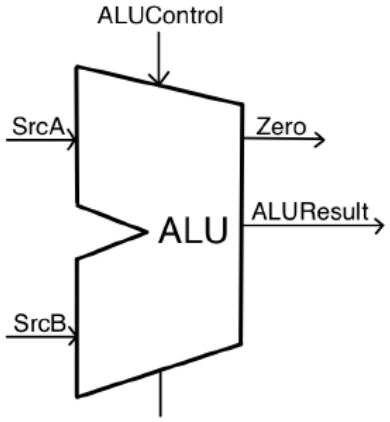


Figure 4: Schematic of the basic ALU

Figure 5 shows the corresponding Verilog code snippet for the ALU. Inside the `always @(*)` block, a `case` statement differentiates each operation: `3'b000` for addition (`SrcA + SrcB`), `3'b001` for subtraction, etc. Whenever `ALUResult` evaluates to zero, the `Zero` output is asserted high.

2.1.2 ALU Simulation and Results

I tested the ALU with a dedicated testbench that varies `ALUControl` and input operands. For example, when `ALUControl = 3'b000` and `SrcA = 10`, `SrcB = 5`, the ALU outputs

```
always @(*) begin

    case (ALUControl)
        3'b000: ALUResult = SrcA + SrcB;                          // ADD
        3'b001: ALUResult = SrcA - SrcB;                          // SUB
        3'b010: ALUResult = SrcA & SrcB;                          // AND
        3'b011: ALUResult = SrcA | SrcB;                          // OR
        3'b100: ALUResult = (SrcA < SrcB) ? 32'd1 : 32'd0;         // SLT
        default: ALUResult = 32'd0;
    endcase
end
```

Figure 5: Key Verilog code snippet for the ALU, illustrating the `always` block and `case` statement handling ADD, SUB, AND, OR, and SLT operations.

15. Similarly, subtraction (`3'b001`) with the same operands yields `5`. When `SrcA = 7` and `SrcB = 7`, the subtraction result is zero, driving `Zero` high. Figure 6 shows the ModelSim waveform for these scenarios, confirming that each control setting produces the expected result.

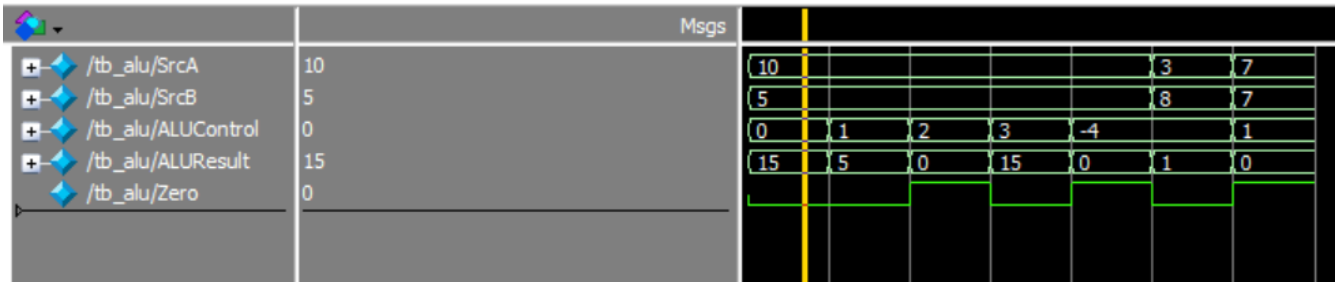


Figure 6: ALU simulation waveform. Each segment corresponds to a different `ALUControl` value. ADD (10+5=15), SUB (10-5=5), AND/OR with bitwise logic, and SLT comparison can be observed. When the result is zero, the `Zero` flag is asserted.

2.2 Register File

2.2.1 Register File Design and Code Overview

Figure 7 illustrates a multi-ported register file with two 32-bit read ports (`rs1`, `rs2`) and one 32-bit write port (`rd`). In RISC-V, `x0` is always zero, so any writes to register zero are discarded.

The main logic is shown in Figure 8, where an `always @(posedge clk or posedge rst)` block handles synchronous writes. On reset, all registers initialize to zero. During normal operation, the address `rd` is written with `writeData` on a rising clock edge, provided `RegWrite` is asserted and `rd` is not zero.

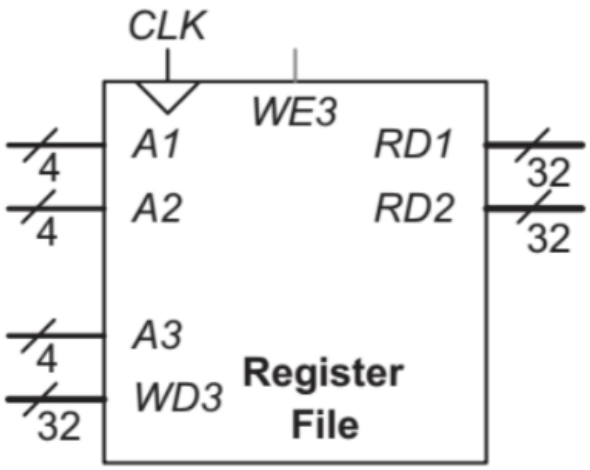


Figure 7: Register file architecture with two simultaneous read ports and a single write port.

```
always @(posedge clk or posedge rst) begin

    if (rst) begin
        for (i = 0; i < 32; i = i + 1) begin
            register_file_array[i] <= 32'b0;
        end
    end else begin
        if (RegWrite) begin

            if (rd != 5'd0) begin
                register_file_array[rd] <= writeData;
            end
        end
    end
end
```

Figure 8: Highlighted Verilog code for the register file. The `always` block resets all 32 registers to zero or writes new data to register `rd` if `RegWrite` is enabled.

2.2.2 Register File Simulation and Results

I verified basic read/write operations by instantiating the register file in a testbench. When `RegWrite` = 1 and `rd`=1, for instance, the value `0xAAAA_5555` is captured on the next clock edge. Reading from `rs1`=1 then returns that same data. Attempts to write to `rd`=0 confirm `x0` remains zero. Figure 9 displays the resulting waveform.

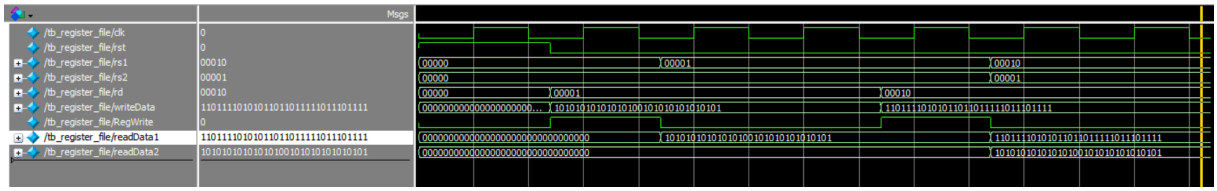


Figure 9: Register file waveform showing successful writes to nonzero registers and continuous reads on `rs1`, `rs2`. Register zero (`x0`) is never modified, adhering to RISC-V conventions.

2.3 Data Memory

2.3.1 Memory Interface and Operation

In a RISC-V CPU, data memory stores operands and intermediate results. Figure 10 depicts a typical interface with a 32-bit `Address`, 32-bit `Write data`, and a 32-bit `Read data` output. Two control signals, `MemWrite` and `MemRead`, indicate whether a store (SW) or load (LW) is taking place. The design can be synchronous or asynchronous, depending on FPGA resources and architectural preferences.

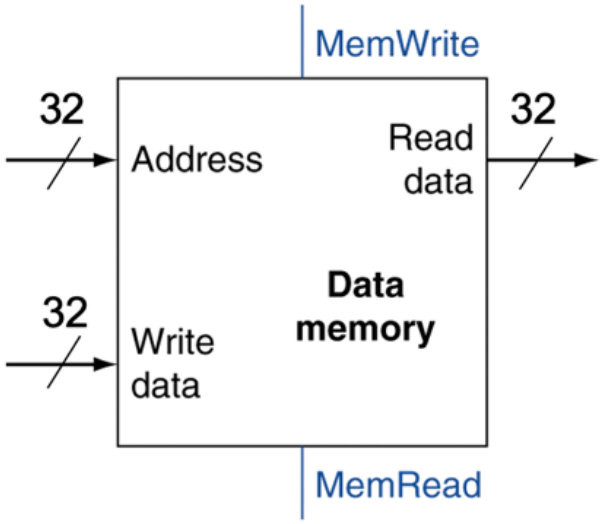


Figure 10: Data memory module with a 32-bit address, 32-bit write/read data lines, and control signals `MemWrite` and `MemRead`.

A typical load sequence might set `MemRead` high, place a valid address on `Address`, and then capture the memory's output in the next pipeline stage. For stores, `MemWrite` goes high while `Write data` and `Address` remain stable until the operation completes. In the following pipeline implementation, these signals coordinate with the ALU result (e.g., `SrcA + immediate`) to compute addresses for memory access.

Summary

In these sections above, I examined the design and verification of three core components in a RISC-V CPU:

- The **ALU**, which processes arithmetic and logic operations based on a 3-bit control signal.
- The **Register File**, featuring two read ports and one write port, ensuring `x0` remains constant at zero.
- The **Data Memory** interface, enabling load/store instructions via straightforward control signals (`MemWrite`, `MemRead`).

Each module was tested with ModelSim waveforms and produced expected results such as `10+5=15` in the ALU and correct read/write behavior in the register file. These building blocks form the foundation of the five-stage RISC-V pipeline discussed in subsequent sections.

2.4 Single-Cycle vs. Pipelined Architectures

Modern RISC-V or similar CPU designs can be realized in either a single-cycle implementation or a pipelined implementation, each with distinct performance and complexity trade-offs. In a *single-cycle* CPU, every instruction (from fetching the instruction in memory to writing back the result) completes in exactly one clock cycle. By contrast, in a *pipelined* CPU, the instruction processing stages overlap, akin to an assembly line.

- **Single-Cycle Design:** In a single-cycle CPU, each instruction runs through all five stages (Instruction Fetch, Decode, Execute, Memory, Write Back) in a single clock period. Because the processor's clock period must be long enough to support the slowest instruction [3], many simpler instructions waste time. Figure 11 ("Complete single-cycle processor") provides a high-level schematic, where the control logic orchestrates ALU operations, register file reads/writes, and memory accesses in one extended cycle per instruction. Although simpler to reason about, the design is often slower for complex instructions, yielding a clock cycle time that scales poorly with more complicated instructions like `LW` (load word).
- **Pipelined Design:** In a pipelined CPU, the classic five stages are divided into separate hardware units, and multiple instructions advance through these pipeline stages in parallel. Figure 12 ("Pipelined Datapath") shows the canonical five-stage pipeline structure, where each stage is separated by pipeline registers. While

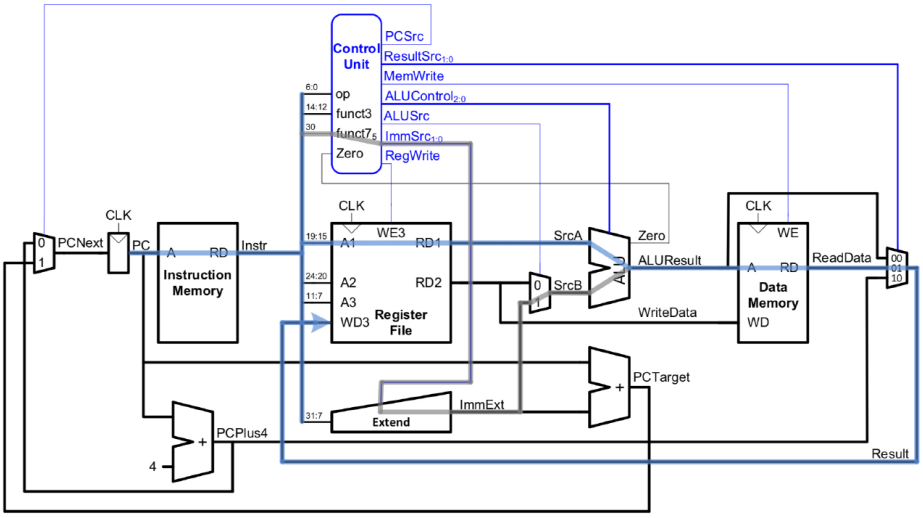


Figure 11: Complete single-cycle processor. All stages (IF, ID, EX, MEM, WB) happen in a single extended clock cycle. [3]

one instruction occupies the Execute (EX) stage, the next instruction can simultaneously occupy the Decode (ID) stage, etc. This arrangement can significantly improve the overall throughput (one instruction completing each cycle, after the pipeline is full). However, pipeline overhead arises from the need to handle hazards and to insert pipeline registers.

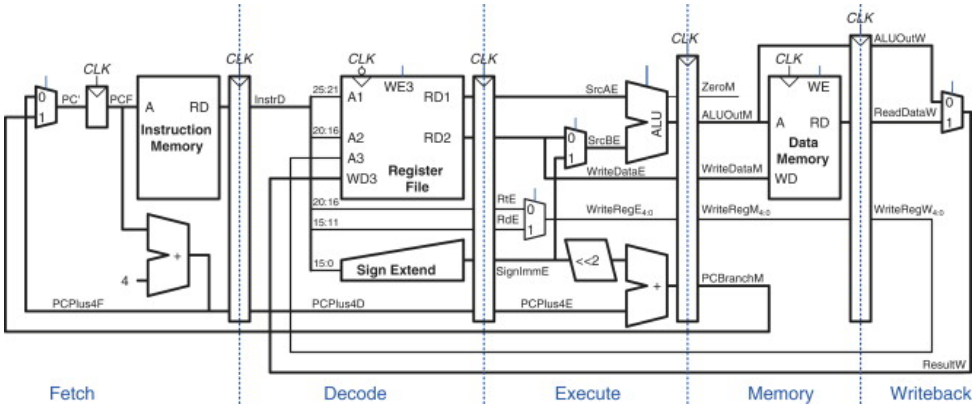


Figure 12: Pipelined datapath with five stages and pipeline registers (gray) between them. Instructions proceed concurrently through IF, ID, EX, MEM, and WB. [3]

Figure 13 offers a timing diagram comparison:

- *(a) Single-cycle timing* shows that the CPU finishes one entire instruction within one lengthy cycle, and the next instruction waits for the subsequent cycle.
- *(b) Pipelined timing* reveals how instructions overlap in time, each occupying different stages of the pipeline concurrently. After a short pipeline fill period,

the processor can complete nearly one instruction per clock cycle, substantially increasing the instruction throughput (instructions per second).

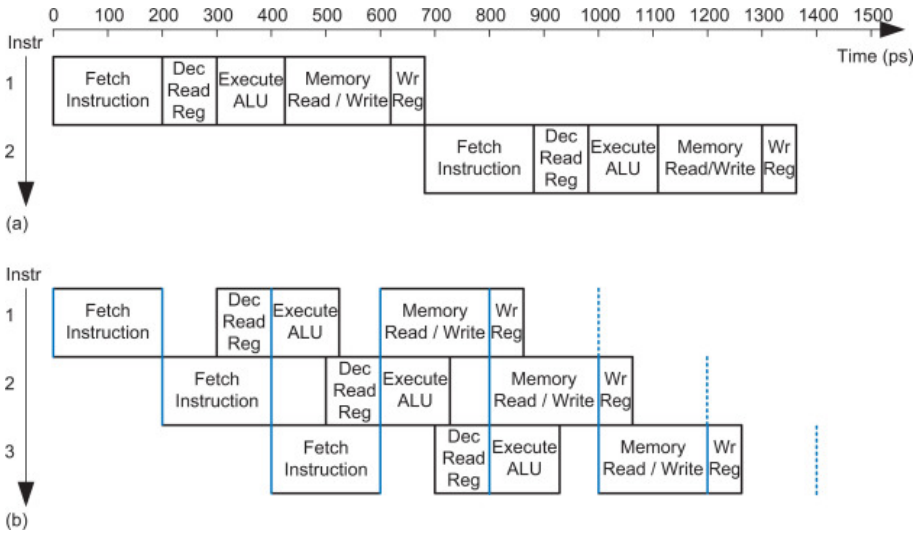


Figure 13: (a) Single-cycle timing vs. (b) pipelined timing. Note how the pipelined design overlaps different instructions in each stage, improving overall throughput. [3, 14]

The performance advantage of pipelining is often summarized by the *ideal CPI* (cycles per instruction) approaching 1. The actual CPI is usually slightly higher due to stalls, flushes, and hazard resolution. Nonetheless, pipelining remains foundational to modern CPU performance.

2.5 Control Signals and Their Role

Both single-cycle and pipelined processors rely on a dedicated control unit to generate various *control signals*, which steer data flow through the datapath. For instance:

- `RegWrite`: Enables writing the register file on the rising edge of the clock.
- `MemWrite`: Enables writing to data memory.
- `ALUSrc`: Selects whether the second ALU operand is a register file output or an immediate (extended) value.
- `MemtoReg`: Routes the result from data memory (for a load) versus the ALU output back into the register file.
- `PCSrc`: Decides whether the next PC comes from `PC+4` or from a branch target (for branches and jumps).
- `ALUControl`: Encodes the type of ALU operation (e.g. ADD, SUB, AND, OR, etc.).

Single-Cycle Control: In a single-cycle design (e.g., Figure 11), the control logic is typically a purely *combinational* block that examines the `opcode` and `funct` fields of the current instruction. It then asserts the correct mix of signals (`RegWrite`, `MemWrite`, etc.) so that the datapath executes that instruction in the same (and only) cycle.

Since all stages happen at once, each control signal must be valid throughout the entire extended cycle. A single-cycle control unit can be constructed by a decoder plus sub-decoders for ALU operations, resulting in a truth-table-based or HDL-based logic that directly sets each control line.

Pipelined Control: In a pipelined design (e.g., Figure 12), the control signals must be carried along with the instruction data from one stage to the next, because each stage may need different subsets of the signals. Typically, the ID (decode) stage generates all the signals, and pipeline registers pass them to EX, MEM, and WB stages. The `MemWrite` control, for example, is only needed in the MEM stage, so it flows through pipeline registers from ID until it arrives at MEM [3, 14].

Handling branches and other instructions that change flow is more complex, because the control logic must detect the branch *early enough* and choose whether to fetch new instructions or flush pipeline stages that fetched unwanted instructions. Hence, the pipeline control must be mindful of the pipeline timing and is typically more elaborate than in the single-cycle case.

2.6 Hazard Handling

When instructions overlap in a pipelined CPU, various conflicts called *hazards* arise. Figure 14 ("Abstract pipeline diagram illustrating hazards") shows an example, highlighting possible collisions between pipeline stages. I categorize hazards as follows:

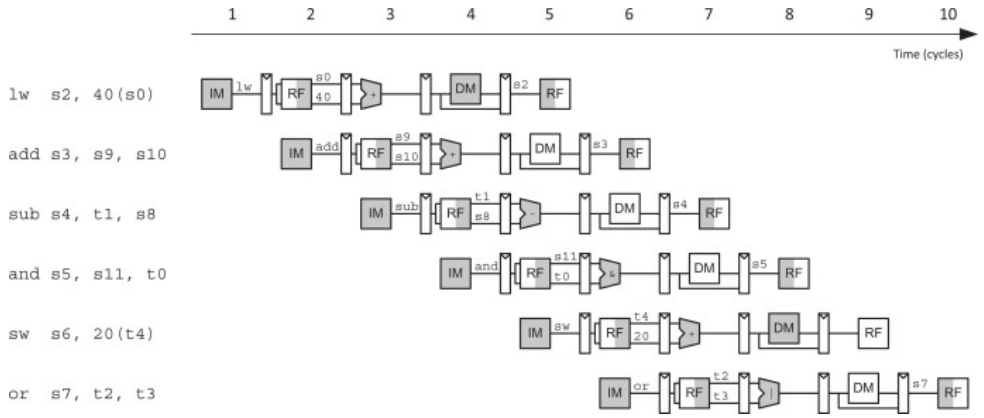


Figure 14: Abstract pipeline diagram illustrating hazards. Overlapping instructions can conflict on registers (data hazards), addresses (control hazards), or hardware resources (structural hazards).

Data Hazards

A data hazard occurs when one instruction depends on a value that has not yet been written back by a preceding instruction. For instance, if `I1` writes to register `x5` in the WB stage at the end of cycle t, but `I2` tries to read `x5` in the ID stage *during* cycle t, `I2` will read an old, incorrect value. Common solutions include:

- **Forwarding** (or bypassing): The pipeline routes the result directly from the EX or MEM stage of `I1` to the input of the ALU for `I2`'s EX stage, thereby bypassing the register file's older contents.
- **Stalling**: The pipeline inserts a no-operation (NOP) instruction or *bubble* so that the instruction needing the operand waits an extra cycle or two [3, 14]. This approach negatively impacts throughput, so modern designs use forwarding wherever possible and only resort to stalls when absolutely needed (e.g. load-use hazards).

Control Hazards

A control hazard (or branch hazard) arises when the CPU does not yet know whether a branch is taken, but it has already fetched subsequent instructions [3, 14]. If the branch is taken, some incorrectly fetched instructions must be flushed from the pipeline. Approaches include:

- **Stall until branch resolution**: The simplest method, but stalls degrade performance.
- **Early branch resolution**: The CPU moves branch determination to an earlier pipeline stage (e.g., ID), reducing or removing the hazard penalty.
- **Branch prediction**: The CPU predicts whether the branch is likely taken or not, continuing to fetch along that path. If the prediction is wrong, it flushes the mis-fetched instructions.

Structural Hazards

Although less common in a fully *Harvard* pipeline (where instruction and data memories are separate), a structural hazard can occur if two stages need the same hardware resource simultaneously [3, 14]. For example, if the memory stage (MEM) and the instruction fetch stage (IF) share a single memory module, a structural hazard arises any time an instruction tries to perform a data access in the same cycle that another

instruction needs to fetch an instruction [15]. Workarounds may involve duplicating resources or scheduling memory accesses to avoid conflicts.

In summary, hazard handling is an integral part of pipeline design. The hazard unit detects hazards by comparing register fields among instructions in different stages. When it identifies a data or control hazard, the pipeline either forwards data values, stalls, or flushes instructions. Although this extra logic adds complexity compared to a single-cycle design, pipelining drastically improves instruction throughput in most real workloads.

3 Methodology

This section describes our methodology in three major steps: (1) introducing the MNIST dataset and the core deep-learning techniques used (including regularization methods and activation functions), (2) training and quantizing a Convolutional Neural Network (CNN) to generate integer-weight data, and (3) leveraging those integer parameters (in a `hex` file) to validate matrix multiplication on a single-cycle processor and a five-stage pipelined processor. Although this subsection focuses on the data-generation process, subsequent parts will discuss how each CPU design is implemented and tested.

3.1 MNIST and Machine-Learning Techniques

3.1.1 MNIST Dataset

MNIST is a well-established benchmark dataset for digit recognition, containing 60,000 training images and 10,000 test images of handwritten digits 0–9 [16]. Each image is 28×28 pixels in grayscale, making it a convenient starting point for demonstrating convolutional architectures and various network optimizations. Despite its relatively simple nature, MNIST remains a standard reference for validating fundamental design concepts in deep learning systems.

3.1.2 Regularization and Activation Functions

To improve generalization and prevent overfitting, various regularization mechanisms are common in CNNs:

- **Batch Normalization (BN):** Introduced by Ioffe and Szegedy [17], BN normalizes intermediate feature map activations, often accelerating training and stabilizing gradients.

- **Dropout:** Randomly disabling a fraction of neurons during training effectively combats overfitting, encouraging more robust feature extraction [17].

I also use the Rectified Linear Unit (ReLU) activation, $\mathrm{ReLU}(x) = \max(0, x)$, which is simple and prevents vanishing gradients in deeper architectures.

3.1.3 Model Architecture and Training

Building upon these ideas, I trained a CNN on MNIST using two convolutional blocks (each with ReLU, batch normalization, and max-pooling), followed by dropout. After flattening, a 128-neuron fully connected layer (with ReLU, batch normalization, dropout) precedes a final softmax output layer for digit classification. I employ `Adam` as the optimizer and `sparse_categorical_crossentropy` as the loss function, typically running for 10 epochs at a batch size of 128. In practice, this setup quickly converges to $\approx 98\%$ validation accuracy on MNIST.

```
model = Sequential([

    Conv2D(32, (3, 3), activation='relu', input_shape=(28, 28, 1), padding='same'),
    BatchNormalization(),
    MaxPooling2D(pool_size=(2, 2)),
    Dropout(0.25),



    Conv2D(64, (3, 3), activation='relu', padding='same'),
    BatchNormalization(),
    MaxPooling2D(pool_size=(2, 2)),
    Dropout(0.25),


    Flatten(),
    Dense(128, activation='relu'),
    BatchNormalization(),
    Dropout(0.5),
    Dense(10, activation='softmax')
])
```

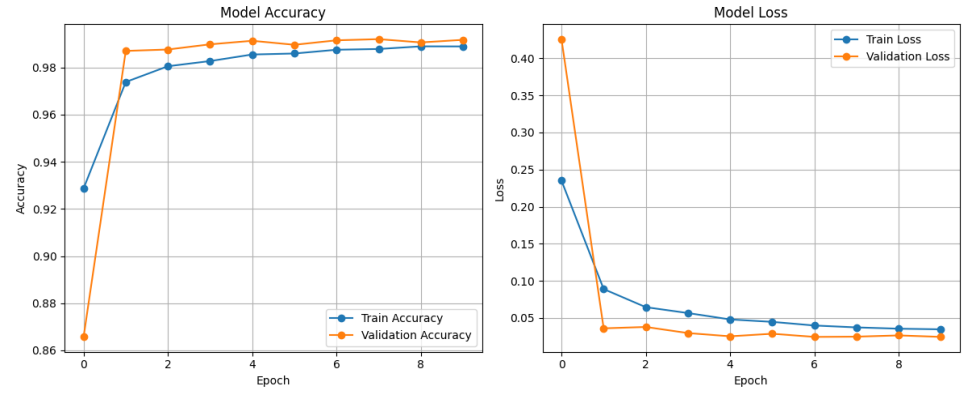
Figure 15: Core snippet of the Keras CNN code, demonstrating convolutional layers with batch normalization, dropout, and a final fully connected block.

Figure 16 displays sample convergence curves (accuracy/loss) across epochs, as well as example MNIST digits. The fundamental model-building code is partially shown in Figure 15, reflecting the essential layers and hyperparameters used.

3.1.4 Post-Training Quantization and Hex Data Generation

To align with embedded application constraints, I convert the trained floating-point model to 8-bit integer precision via TensorFlow Lite (`tf.lite.TFLiteConverter`) optimizations [17]. In particular:

1. **Quantization:** Scales and zero-points are computed for each layer's weights and activations, reducing them to 8-bit.




```
Epoch 1/10
469/469 ━━━━━━━━━━━━━━━━━━━━ 10s 19ms/step - accuracy: 0.8568 - loss: 0.4780 - val_accuracy: 0.8657 - val_loss: 0.4258
Epoch 2/10
469/469 ━━━━━━━━━━━━━━━━━━━━ 10s 21ms/step - accuracy: 0.9723 - loss: 0.0946 - val_accuracy: 0.9870 - val_loss: 0.0359
Epoch 3/10
469/469 ━━━━━━━━━━━━━━━━━━━━ 10s 21ms/step - accuracy: 0.9801 - loss: 0.0655 - val_accuracy: 0.9876 - val_loss: 0.0378
Epoch 4/10
469/469 ━━━━━━━━━━━━━━━━━━━━ 9s 19ms/step - accuracy: 0.9833 - loss: 0.0543 - val_accuracy: 0.9898 - val_loss: 0.0296
Epoch 5/10
469/469 ━━━━━━━━━━━━━━━━━━━━ 9s 20ms/step - accuracy: 0.9856 - loss: 0.0490 - val_accuracy: 0.9913 - val_loss: 0.0252
Epoch 6/10
469/469 ━━━━━━━━━━━━━━━━━━━━ 9s 20ms/step - accuracy: 0.9865 - loss: 0.0428 - val_accuracy: 0.9896 - val_loss: 0.0287
Epoch 7/10
469/469 ━━━━━━━━━━━━━━━━━━━━ 9s 20ms/step - accuracy: 0.9874 - loss: 0.0397 - val_accuracy: 0.9915 - val_loss: 0.0244
Epoch 8/10
469/469 ━━━━━━━━━━━━━━━━━━━━ 9s 20ms/step - accuracy: 0.9871 - loss: 0.0384 - val_accuracy: 0.9920 - val_loss: 0.0247
Epoch 9/10
469/469 ━━━━━━━━━━━━━━━━━━━━ 9s 20ms/step - accuracy: 0.9895 - loss: 0.0337 - val_accuracy: 0.9906 - val_loss: 0.0264
Epoch 10/10
469/469 ━━━━━━━━━━━━━━━━━━━━ 9s 20ms/step - accuracy: 0.9892 - loss: 0.0329 - val_accuracy: 0.9917 - val_loss: 0.0244
Test loss: 0.0244
Test accuracy: 0.9917
```

Figure 16: Top: Illustration off training/validation accuracy and loss over 10 epochs for MNIST.
Bottom: Sample grayscale MNIST images for digits 0–9.

2. **Export to `.tflite`:** The final quantized model is saved, enabling on-device inference on microcontrollers [18].

3. **Dump integer arrays to `hex` file:** I parse each integer parameter (weights, biases) and write them line-by-line in hexadecimal (`cnn_weights.hex`). This dataset accurately reflects the numeric distributions typical of CNN inference.

Figure 17 outlines the post-quantization layer structure, including the shapes of convolutional filters and dense layer parameters. I select only the first 64 lines of the `hex` file to represent 8×8 matrices used in the subsequent matrix multiplication tests.

Advantages of Using Real Quantized Data

- **Realistic Numeric Ranges:** CNN parameters exhibit typical distributions that test integer math logic in a manner more robust than trivial or random data.

- **Practical Verification:** By comparing CPU-computed matrix products to the TFLite or Python reference, I guarantee correctness in a scenario closely resembling embedded deep learning.

Model: "sequential"

Layer (type)	Output Shape	Param #
conv2d (Conv2D)	(None, 28, 28, 32)	320
batch_normalization (BatchNormalization)	(None, 28, 28, 32)	128
max_pooling2d (MaxPooling2D)	(None, 14, 14, 32)	0
dropout (Dropout)	(None, 14, 14, 32)	0
conv2d_1 (Conv2D)	(None, 14, 14, 64)	18,496
batch_normalization_1 (BatchNormalization)	(None, 14, 14, 64)	256
max_pooling2d_1 (MaxPooling2D)	(None, 7, 7, 64)	0
dropout_1 (Dropout)	(None, 7, 7, 64)	0
flatten (Flatten)	(None, 3136)	0
dense (Dense)	(None, 128)	401,536
batch_normalization_2 (BatchNormalization)	(None, 128)	512
dropout_2 (Dropout)	(None, 128)	0
dense_1 (Dense)	(None, 10)	1,290

Total params: 422,538 (1.61 MB)
Trainable params: 422,090 (1.61 MB)
Non-trainable params: 448 (1.75 KB)

Figure 17: Layer-wise summary after quantization, including convolutional and fully connected parameters.

- **Uniform 8-bit Format:** The `hex` data replicate embedded-friendly integer formats, which is key for validating both pipeline logic and memory access patterns under realistic loads.

Both single-cycle and pipelined designs load the same quantized `hex` data for matrix multiplication. Using the top 64 lines to form eight 8×8 integer matrices, I demonstrate how the designs handle typical embedded inference parameters. Finally, by comparing their hardware results against a Python/TFLite reference, I confirm functional correctness and set the stage for performance discussion.

3.2 Single-Cycle Microprocessor

Having established the motivation for using quantized CNN parameters, we now present our *single-cycle* CPU implementation. In this approach, each instruction (including any custom operations such as matrix multiplication or ReLU) completes fully within one clock cycle. The design proves helpful for correctness verification, albeit with a stringent timing requirement to accommodate the most complex instruction path in a single cycle.

3.2.1 Overall Top-Level Structure

Figure 18 shows the updated CPU schematic, combining:

1. **Instruction Memory**: A small array for storing RISC-V instructions, indexed by `PC[9:2]`.

2. **Control Unit**: Decodes fields from the instruction (`opcode`, `funct3`, `funct7`) to generate `alu_ctrl`, `alu_src`, `reg_write`, `mem_write`, `pc_src`, *etc.*

3. **Register File**: 32 general-purpose registers, with two read ports and one write port, addressed by `instr[19:15]` (`rs1`), `instr[24:20]` (`rs2`), and `instr[11:7]` (`rd`).

4. **ALU Module**: Performs arithmetic/logic instructions and custom instructions.

5. **Data Memory**: For load/store instructions, addressed by the ALU output.

Because the design completes each instruction in one cycle, the program counter (`PC`) must update every clock edge: it typically increments by 4, or if a branch is taken (`pc_src` set), it jumps by an immediate offset. For memory instructions, the same cycle fetches the instruction, reads registers, computes an address, possibly reads/writes data memory, and writes back to a register (if needed).

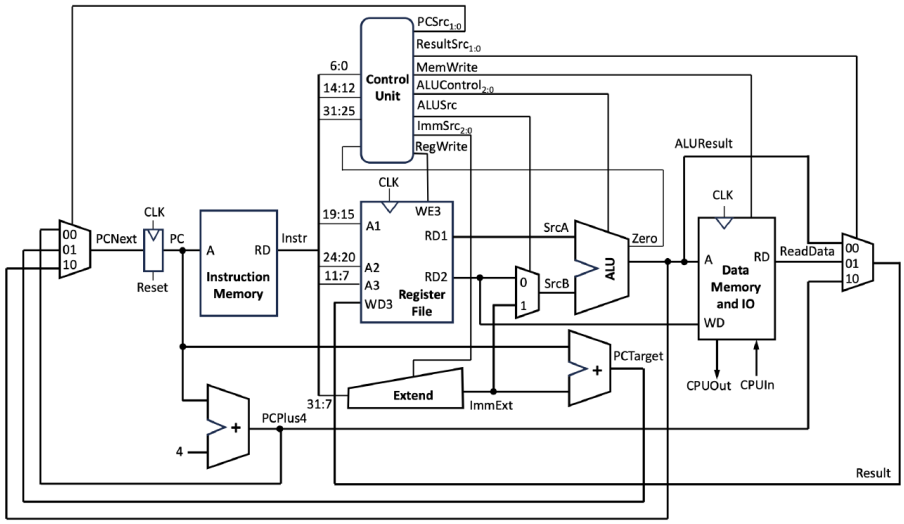


Figure 18: Top-level single-cycle CPU design. All stages—Fetch, Decode, Execute, Memory Access, Write-Back—occur within a single clock period.

3.2.2 ALU with Extended Custom Operations

The updated `ALU` code snippet is illustrated in Figure 19. A control signal `custom_en` selects between standard R-type operations and special instructions. In the standard path (`custom_en`=0), the ALU handles:

- `3'b000`: Add (`a + b`)
- `3'b001`: Sub (`a - b`)
- `3'b010`: And (`a & b`)
- `3'b011`: Or (`a | b`)
- `3'b100`: Equality check (`a == b`)
- `3'b101`: Inequality check (`a != b`)

When `custom_en`=1, two new opcodes are available for custom instructions:

- `3'b110 (MaxMul)`: A simplified matrix multiplication or scalar multiplication, returning `a * b`.
- `3'b111 (ReLU)`: Returns `(a > 0) ? a : 0`.

This design demonstrates the extensibility of the ALU to domain-specific tasks (like matrix multiplication or activation functions) with minimal overhead in a single-cycle environment.

```
always @(*) begin
    if(custom_en) begin
        case(op)
            3'b110: result  <= a * b;
            3'b111: result  <= (a > 0) ? a : 0; // ReLU
            default: result <= 0;
        endcase
    end else begin
        case(op)
            3'b000: result  <= a + b;
            3'b001: result  <= a - b;
            3'b010: result  <= a & b;
            3'b011: result  <= a | b;
            3'b100: result  <= (a == b);
            3'b101: result  <= (a != b);
            default: result <= 0;
        endcase
    end
end
endmodule
```

Figure 19: Core ALU snippet: standard arithmetic/logic plus custom ops (MaxMul, ReLU) gated by `custom_en`.

3.2.3 Control Unit Logic

Our `ctrl` module, shown in Figure 20, provides the necessary signals for instruction execution within a single cycle:

- **Standard R-type** (`7'b0110011`): Sets `reg_write=1`, chooses `alu_ctrl` according to `funct3` (`ADD`, `SUB`, `AND`, `OR`), with `funct7[5]` distinguishing Add/Sub.

- **Load** (`7'b0000011`) and **Store** (`7'b0100011`): Asserts `mem_read` or `mem_write`, sets `alu_src=2'b10` to add the immediate for addressing, and if load, sets `mem_to_reg=1`.
- **Branch** (`7'b1100011`): Asserts `pc_src`, picks `alu_ctrl` = `BEQ` (`3'b100`) or `BNE` (`3'b101`).
- **Custom** (`7'b0001011`): Activates `custom_en=1`, sets `reg_write=1`, and uses `funct3` to select *MaxMul* (`3'b110`) or *ReLU* (`3'b111`).

```
    always @(*) begin

        reg_write  = 0;
        mem_to_reg = 0;
        mem_write  = 0;
        mem_read   = 0;
        alu_src    = 2'b00;
        pc_src     = 0;
        alu_ctrl   = 3'b000;
        custom_en  = 0;

        case(opcode)
            7'b0110011: begin // R-type
                reg_write = 1;
                case(funct3)
                    3'b000: alu_ctrl = (funct7[5] ? 3'b001 : 3'b000); // ADD/SUB
                    3'b111: alu_ctrl = 3'b010; // AND
                    3'b110: alu_ctrl = 3'b011; // OR
                endcase
            end
            7'b0000011: begin // Load
                reg_write = 1;
                mem_to_reg = 1;
                mem_read = 1;
                alu_src = 2'b10;
                alu_ctrl = 3'b000;
            end
            7'b0100011: begin // Store
                mem_write = 1;
                alu_src = 2'b10;
                alu_ctrl = 3'b000;
            end
            7'b1100011: begin // Branch
                pc_src = 1;
                case(funct3)
                    3'b000: alu_ctrl = 3'b100; // BEQ
                    3'b001: alu_ctrl = 3'b101; // BNE
                endcase
            end
            7'b0001011: begin // 自定义指令
                custom_en = 1;
                reg_write = 1;
                case(funct3)
                    3'b000: alu_ctrl = 3'b110; // MaxMul
                    3'b001: alu_ctrl = 3'b111; // ReLU
                endcase
            end
        endcase
    end
endmodule
```

Figure 20: Control unit excerpt mapping `opcode`+`funct3`+`funct7` to single-cycle signals: `alu_ctrl`, `pc_src`, `mem_write`, `custom_en`, and others.

Because we are not pipelining, there is no need for pipeline registers or stall logic. The control signals are purely combinational, inferred once per instruction fetch.

3.2.4 Data Path Operation in One Cycle

Within `riscv_single_block`, each clock cycle proceeds as follows:

1. **PC and Instruction Fetch**: The `pc` increments by 4 unless `pc_src=1`, in which case it adds a sign-extended branch immediate. The new `pc` addresses `instr_mem` to obtain the 32-bit instruction.

2. **Register Reads and ALU Inputs**: The CPU reads `rs1_data`, `rs2_data` from the register file. If needed, an immediate is sign-extended (`imm_ext`) and selected by `alu_src`.

3. **ALU Execution**: The `alu` receives `a=rs1_data` and `b`, determined by `alu_src` (either `rs2_data`, `4`, or `imm_ext`). It then returns `alu_result`, which could be a normal arithmetic/logic result or a custom MaxMul/ReLU operation.

4. **Memory Access (if load/store)**: If `mem_write=1`, the CPU writes `rs2_data` into `data_mem[alu_result[9:2]]`; if `mem_read=1`, `mem_data` is read from that same address.

5. **Write Back**: If `reg_write=1` and `rd` $\neq 0$, the CPU updates the register file at index `instr[11:7]` with either `alu_result` or `mem_data`, depending on `mem_to_reg`.

All of these actions—fetch, decode, read registers, compute address, data memory read/write, and register write—occur in a single cycle. The main limitation is the clock must be slow enough to accommodate the worst-case instruction delay path, including the custom matrix multiplication.

3.2.5 Observations and Use for Matrix Multiply Verification

- **MaxMul Instruction**: The ALU multiplies `a * b` in one cycle. This is a straightforward scalar multiply. In principle, repeated usage can replicate 8×8 matrix multiplication if the program orchestrates multiple `MaxMul` instructions and accumulations.

- **ReLU Instruction**: The ALU conditionally zeroes negative values. This mimics common neural network activation in embedded inference.

- **Testing Real CNN Weights**: Once the `cnn_weights.hex` data are loaded into memory or register file, we can run a short RISC-V assembly loop that calls `MaxMul` for each partial product. The single-cycle CPU's register file accumulates the results in an outer loop, verifying correctness.

Although this design is not deeply optimized (due to the single-cycle constraint), it is conceptually simpler and serves as a robust baseline. In the next section (§**??**), we contrast it with a **five-stage pipelined processor**, distributing the same operations across multiple pipeline stages and adopting advanced hazard handling.

4 Results, Analysis and Discussion

5 Conclusion and Future Work

6 References

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7 Appendices

To add appendices, use the `\appendix` command, followed by `\section` commands for each appendix. Appendices start on a new page. To start every appendix on a new page use `\newpage` in the LaTeX code.

Appendices

A Some supplemental material

Note that this page does not appear in the page count in the declaration.

B The second appendix

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