		User: drf@ppa-pc86131	Date:	12/19/13		Total Time R	ange: 0 - 3	3999176000		Page 1	of 3
#	Desig.	Signal	Value			Time: 0 - 3	33999176000	x 1ps (C1	:24086397100		
				0	500000000	1000000	0000 150	0000000	20000000000000000000000000000000000000	250000000	I .
sg		U_ASICSIM_1									
001	V1	OFFSET_NULL	1								
002	V1	ANA_RDBACK	0								
003	V1	ANALOG_STATE(2 downto 0	X"0"	0	1 / 3	6			0		
004	V1	PWR_UP_ACQ	0								
005	V1	RESET_LOAD	0								
006	V1	RESET_L	1								
007	V1	REG_WR_ENA	0								
800	V1	LEAKAGE_NULL	1								
009	V1	RESET	0								
010	V1	RDBACK	1								
011	V1	REG_CLOCK	0								
012	V1	DATA_OUT	1								
013	V1	THRESH_OFF	1								
014	V1	PRECHARGE_BUS	0								
015	V1	DESEL_ALL_CELLS	0								
016	V1	TRIG_INH	1								
017	V1	COMMAND	0								
018	V1	SYSCLK	1								
019	V1	RAMP_PERIOD	0								
020	V1	PWR_UP_ACQ_DIG	0								
021	V1	REG_SEL0	1								
022	V1	REG_SEL1	1								
023	V1	REG_DATA	0								
009: 013: 017:	/KPIXSMA /LLTE /SMAL	KPIXSIM(0)/U_ASICSIM/OFFSET_NULL, 3/KPIXSIM(0)/U_ASICSIM/RESET_LOAD, ALLTB/KPIXSIM(0)/U_ASICSIM/RESET, B/KPIXSIM(0)/U_ASICSIM/THRESH_OFF, LITB/KPIXSIM(0)/U_ASICSIM/COMMAND, JB/KPIXSIM(0)/U_ASICSIM/REG_SEL0,	010: /KPIXSMALLTB/KPIXSIM(0)/U_A 014: /B/KPIXSIM(0)/U_ASICSIM 018: /KPIXSMALLTB/KPIXSIM(0)/U_	ASICSIM/RDBACK M/PRECHARGE_BU _ASICSIM/SYSCI	K, 011: /ALLTB/KPIX US, 015: /KPIXSIM((LK, 019: /LTB/KPIXX	SIM(0)/U_ASICSIM)/U_ASICSIM/DESE IM(0)/U_ASICSIM/	1/REG_CLOCK, 01 CL_ALL_CELLS, 0 RAMP_PERIOD, 0	2: /MALLTB/	KPIXSIM(0)/U_ASI(/KPTXSTM(0)/U_AS	CSIM/DATA_OUT,	

		τ	User: drf@ppa-pc86131	Date:	12/19/13	Total Time Range:	0 - 33999176000		Page 2 of 3	;
#	De	esig.	Signal	Value		Time: 0 - 339991	76000 x 1ps (C			
					0 500000000	II.	15000000000	200000000000000	25000000000000000000000000000000000000	30000000
024	4	V1	READ_STATE(2 downto 0)	X"2"	0					
025	5	V1	TEMP_EN	1						
026	5	V1	SEL_CELL	0						
027	7	V1	DATA_RDBACK	1						
028	8	V1	CAL_STROBE	0						
029	9	V1	<pre>TEMP_ID(7 downto 0)</pre>	X"55"	0c 0c		55			
sg	;	τ	J_ASICSIM							
030	0	V1	OFFSET_NULL	1						
031	1	V1	ANA_RDBACK	0						
032	2	V1	ANALOG_STATE(2 downto 0	X"0"	0 1 3	6		0		
033	3	V1	PWR_UP_ACQ	0						
034	4	V1	RESET_LOAD	0						
035	5	V1	RESET_L	1						
036	5	V1	REG_WR_ENA	0						
037	7	V1	LEAKAGE_NULL	1						
038	8	V1	RESET	0						
039	9	V1	RDBACK	1						
040	0	V1	REG_CLOCK	0						
041	1	V1	DATA_OUT	1						
042	2	V1	THRESH_OFF	1						
043	3	V1	PRECHARGE_BUS	0						
044	4	V1	DESEL_ALL_CELLS	0						
045	5	V1	TRIG_INH	1						
046	5	V1	COMMAND	0						
032: 036: 040:	/. /. /.)/U_ LLTB ALLT	ASICSIM/ANALOG_STATE(2 downto 0), /KPIXSIM(0)/U_ASICSIM/REG_WR_ENA, B/KPIXSIM(0)/U_ASICSIM/REG_CLOCK,	033: /LLTB/KPIXSIM(0)/U_ASIC 037: /TB/KPIXSIM(0)/U_ASICSI 041: /MALLTB/KPIXSIM(0)/U_AS	SICSIM/TEMP_EN, 026: /MALLTB/K ID(7 downto 0), 030: /LTB/KPIX SIM/PWR_UP_ACQ, 034: /LLTB/KPI M/LEAKAGE_NULL, 038: /KPIXSMALLTB ICSIM/DATA_OUT, 042: /LLTB/KPI ICSIM/TRIG_INH, 046: /SMALLTB/	XSIM(0)/U_ASICSIM/RESET_1 /KPIXSIM(0)/U_ASICSIM/RE XSIM(0)/U_ASICSIM/THRESH	LOAD, 035: /SMALLT SET, 039: /KPIXSMALLT _OFF, 043: /B/KPIX	FB/KPIXSIM(0)/U_ASI FB/KPIXSIM(0)/U_ASI	CSIM/RESET_L, CSIM/RDBACK,	

		User: drf@ppa-pc86131	Date	12/19/13 Tota	l Time Range:	0 - 3399917600)	Page 3 of 3	
#	Desig.	Signal	Value	Tin	ne: 0 - 339991	76000 x 1ps (C	1:24086397100RE		
				0 500000000	10000000000	15000000000	C1:24086397100REF 200000000000	M1:24086397100(0) 25000000000	30000000
047	V1	SYSCLK	1						
048	V1	RAMP_PERIOD	0						
049	V1	PWR_UP_ACQ_DIG	0						
050	V1	REG_SEL0	1						
051	V1	REG_SEL1	1						
052	V1	REG_DATA	0		, , ,				
053	V1	READ_STATE(2 downto 0)	X"2"	0					
054	V1	TEMP_EN	1						
055	V1	SEL_CELL	0						
056	V1	DATA_RDBACK	1						
057	V1	CAL_STROBE	0						
058	V1	<pre>TEMP_ID(7 downto 0)</pre>	X"55"	0c 0c		55)
sg		KPIXSMALLTB							
059	V1	FPGARSTL	1						
060	V1	KPIXSERTXOUT(3 downto 0	X"0"	0		0			
061	V1	KPIXCLKOUTP	1						
062	V1	KPIXRSTOUT	0						
063	V1	GTPREFCLKN	0						
064	V1	GTPREFCLKP	1						
065	V1	<pre>KPIXSERRXIN(3 downto 0)</pre>	X"1"	0 0					
066	V1	TRIGIN	(0,0,0,0)			(0,0,0,0)			
047: 051:	/KPIXSMA /MALL	LLTB/KPIXSIM(0)/U_ASICSIM/SYSCLK, TB/KPIXSIM(0)/U_ASICSIM/REG_SEL1,	048: /LTB/KPIXSIM(0)/U_AS: 052: /MALLTB/KPIXSIM(0)/U_	SIM/RAMP_PERIOD, 049: //KPIXSIM(0)/U_ SICSIM/REG_DATA, 053: /(0)/U_ASICSIM/I	ASICSIM/PWR_UP_ACQ READ_STATE(2 downto	_DIG, 050: /MALLT	B/KPIXSIM(0)/U_ASICS TB/KPIXSIM(0)/U_ASIC	SIM/REG_SELO, CSIM/TEMP_EN,	

^{049: /}kPIXSMALLTB/RPIXSIM(0)/U_ASICSIM/SYSCLK, 046: /...TBY.RPIXSIM(0)/U_ASICSIM/REG_SELD, 051: /...RALLTB/RPIXSIM(0)/U_ASICSIM/REG_SELD, 051: /...RALLTB/RPIXSIM(0)/U_ASICSIM/REG_DATA, 053: /...(0)/U_ASICSIM/REG_DATA, 053: /...(0)/U_ASICSIM/REG_DATA, 053: /...(0)/U_ASICSIM/REG_DATA, 053: /...(0)/U_ASICSIM/REG_SELD, 054: /...SMALLTB/RPIXSIM(0)/U_ASICSIM/REG_SELD, 055: /...MALLTB/RPIXSIM(0)/U_ASICSIM/REG_SELD, 056: /...SMALLTB/RPIXSIM(0)/U_ASICSIM/REG_SELD, 056: /...SMALTB/RPIXSIM(0)/U_ASICSIM/REG_SELD, 056: /...SMALTB/RPIXSIM(0)/U_ASICSIM/REG_SELD, 056: /...SMALTB/RPIXSIM(0)/U_ASICSIM/REG_SELD, 056: /...SMALTB/RPIXSIM(0)/U_ASICSIM/REG_SELD, 056: /...SMALTB/RPIXSIM(0)/U_ASICSIM/REG_SELD, 056: /.