

Weekly Report

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Week 5

Summary:

This week, I paid less attention to the capstone project, because of the midterm. Thus, I just solve the problems of last week. I sent the email to sponsor, Ataur and asked my problems of last term. He answered my questions clearly. To sum up, Ataur asked me keep reporting the 1st one detailed report.

Data:

I put one counter in my code and make it meet the requirement of Ataur.

```
from tkinter import *
import re

def detail_report_window(report):
    root = Tk()
    root.title('Detail Timing Report')
    root.geometry('800x600')
    atext=Text(root,width='600', height='600',bg='yellow')
    atext.insert(INSERT, report)
    atext.pack()

def match_detail(path1,path2,path_group):
    QOR_report=open(path1).read()
    Detailed_QOR_report=open(path2).read()
    for str in QOR_report.split('\n\n'):
        if re.search(path_group ,str, re.M|re.I):
            fact=re.search(r'Critical Path Slack:(.*)',str,re.M|re.I)
            slack=fact.group(1)
            i=0
            for str in Detailed_QOR_report.split('\n\n\n'):
                if re.search(r'Path Group: '+path_group,str,re.M|re.I):
                    if re.search(r'slack.*'+slack,str,re.M|re.I):
                        if i<1:
                            detail = re.search(r'Startpoint:.*slack.*\d', str, re.M|re.I|re.S|re.DOTALL)
                            detail_report_window(detail.group())
                            i+=1

Detailed_QOR_report_path="C:/Users/Ting Wang/Desktop/tool/QORs_Detailed_Timing_Report.txt"
QOR_report_path="C:/Users/Ting Wang/Desktop/tool/QOR_Report_File.txt"
Path_Group=input("Path_Group: ")
match_detail(QOR_report_path, Detailed_QOR_report_path, Path_Group)
```

When I typed in “inputs”, the previous result:

Detail Timing Report											
Start	Start	Start	Start	Start	Start	Start	Start	Start	Start	Start	Startpoint: wdata[2] (input port clocked by wclk)
En	En	En	En	En	En	En	En	En	En	En	Endpoint: fifomem/mem_reg[2][2] (rising edge-triggered flip-flop clocked by wclk)
Pa	Pat	Pat	Pa	Pa	Pa	Pa	Pa	Pa	Pa	Pa	Path Group: INPUTS
Pa	Pat	Pat	Pa	Pa	Pa	Pa	Pa	Pa	Pa	Pa	Path Type: max
De	Des	Des	De	De	De	De	De	De	De	De	Des/Clust/Port
---	---	---	---	---	---	---	---	---	---	---	Wire Load Model
---	---	---	---	---	---	---	---	---	---	---	Library
fi	fif	fifo	fi	fi	fi	fi	fi	fi	fi	fi	fifol 8000 saed32rvt_fflp16vl25c
fi	fif	fifo	fi	fi	fi	fi	fi	fi	fi	fi	fifomem_DATASIZE4_ADDRSIZE2 ForQA saed32rvt_fflp16vl25c
Po	Poi	Poi	Po	Po	Po	Po	Po	Po	Po	Po	Point
---	---	---	---	---	---	---	---	---	---	---	Cap
---	---	---	---	---	---	---	---	---	---	---	Trans
---	---	---	---	---	---	---	---	---	---	---	Incr
---	---	---	---	---	---	---	---	---	---	---	Path
cl	cloc	cloc	cl	cl	cl	cl	cl	cl	cl	cl	clock wclk (rise edge) 0.000 0.000
cl	cloc	cloc	cl	cl	cl	cl	cl	cl	cl	cl	clock network delay (ideal) 0.000 0.000
in	inp	inp	ir	ir	ir	ir	ir	ir	ir	ir	input external delay 0.100 0.100 r
wd	wda	wdat	wd	wd	wd	wd	wd	wd	wd	wd	wdata[2] (in) 1.879 0.000 0.000 0.100 r
fi	fif	fifo	fi	fi	fi	fi	fi	fi	fi	fi	fifomem/wdata[2] (fifomem_DATASIZE4_ADDRSIZE2) 0.000 0.100 r
fi	fif	fifo	fi	fi	fi	fi	fi	fi	fi	fi	fifomem/U16/A2 (AO22X1) 0.000 0.196 0.296 r
fi	fif	fifo	fi	fi	fi	fi	fi	fi	fi	fi	fifomem/U16/Y (AO22X1) 0.734 0.025 0.031 0.326 r
fi	fif	fifo	fi	fi	fi	fi	fi	fi	fi	fi	fifomem/mem_reg[2][2]/D (DFFX1) 0.025 0.011 0.338 r
da	dat	data	da	da	da	da	da	da	da	da	data arrival time 0.338
cl	cloc	cloc	cl	cl	cl	cl	cl	cl	cl	cl	clock wclk (rise edge) 1.000 1.000
cl	cloc	cloc	cl	cl	cl	cl	cl	cl	cl	cl	clock network delay (ideal) 0.000 1.000
fi	fif	fifo	fi	fi	fi	fi	fi	fi	fi	fi	fifomem/mem_reg[2][2]/CLK (DFFX1) 0.000 1.000 r
li	lib	lib	li	li	li	li	li	li	li	li	library setup time -0.019 0.981
da	dat	data	da	da	da	da	da	da	da	da	data required time 0.981
---	---	---	---	---	---	---	---	---	---	---	---
da	dat	data	da	da	da	da	da	da	da	da	data required time 0.981
da	dat	data	da	da	da	da	da	da	da	da	data arrival time -0.338
---	---	---	---	---	---	---	---	---	---	---	---
sl	sla	slac	sl	sl	sl	sl	sl	sl	sl	sl	slack (MET) 0.643

There are more than one detailed reports here.

Now, after I changed my code, there is only one detailed report left.

Detail Timing Report

Startpoint: wdata[0] (input port clocked by wclk)					
Endpoint: fifomem/mem_reg[0][0]					
(rising edge-triggered flip-flop clocked by wclk)					
Path Group: INPUTS					
Path Type: max					

Des/Clust/Port	Wire Load Model	Library			

fifol	8000	saed32rvt_fflpl6vl25c			
fifomem_DATASIZE4_ADDR_SIZE2	ForQA	saed32rvt_fflpl6vl25c			

Point	Cap	Trans	Incr	Path	

clock wclk (rise edge)			0.000	0.000	
clock network delay (ideal)			0.000	0.000	
input external delay			0.100	0.100 r	
wdata[0] (in)	1.879	0.000	0.000	0.100 r	
fifomem/wdata[0] (fifomem_DATASIZE4_ADDR_SIZE2)			0.000	0.100 r	
fifomem/U24/A2 (AO22X1)		0.000	0.196	0.296 r	
fifomem/U24/Y (AO22X1)	0.734	0.025	0.031	0.326 r	
fifomem/mem_reg[0][0]/D (DFFX1)		0.025	0.011	0.338 r	
data arrival time				0.338	

clock wclk (rise edge)			1.000	1.000	
clock network delay (ideal)			0.000	1.000	
fifomem/mem_reg[0][0]/CLK (DFFX1)			0.000	1.000 r	
library setup time			-0.019	0.981	
data required time				0.981	

data required time				0.981	
data arrival time				-0.338	

slack (MET)				0.643	

Next Week:

I may mainly focus on my midterm and maybe spend less time on capstone.