

Weekly Report

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Week13

Summary:

Finish the task 19 now. Adding the notebook option in right click popupmenu. User can open a report by adding a new tab or replace the current tab. The code did working on Linux, but need to do some modified.

Issue:

No issues this week.

Data:

Open several report

Search

☒ Startpoint

☒ Endpoint

☒ Path Group

☒ Timing Slack

Keyword

Startpoint

Endpoint

Path Group

Timing Slack (>value or else)

Search

Clear

DC Analysis

Startpoint	Endpoint	Path Group	Timing Slack
wptr_full/wbin_reg[0]	wptr_full/wptr_reg[1]	wclk	0.247
wptr_full/wbin_reg[0]	wptr_full/wptr_reg[0]	wclk	0.434
wptr_full/wbin_reg[0]	wptr_full/wfull_reg	wclk	0.156
wptr_full/wbin_reg[0]	wptr_full/wbin_reg[2]	wclk	0.362
wptr_full/wbin_reg[0]	wptr_full/wbin_reg[1]	wclk	0.547
wptr_full/wfull_reg	wfull	OUTPUTS	0.724
rptr_empty/empty_reg	rptr_empty/rptr_reg[2]	rcclk	0.815
rptr_empty/empty_reg	rptr_empty/rptr_reg[1]	rcclk	0.013
rptr_empty/empty_reg	rptr_empty/rptr_reg[1]	rcclk	-0.040

Report1 ✕ Report2 ✕ Report3 ✕

Startpoint: wptr_full/wbin_reg[0] (rising edge-triggered flip-flop clocked by wclk)
Endpoint: wptr_full/wbin_reg[1] (rising edge-triggered flip-flop clocked by wclk)
Path Group: wclk
Path Type: max

Des/Clust/Port Wire Load Model Library

fifo1 8000 saed32rvt_ff1p16v125c
wptr_full_ADDRSIZE2
ForQA saed32rvt_ff1p16v125c

Point	Cap	Trans	Incr	Path
clock wclk (rise edge)			0.000	0.000
clock network delay (ideal)			0.000	0.000
wptr_full/wbin_reg[0]/CLK (DFFARX1)		0.000	0.000	0.000r
wptr_full/wbin_reg[0]/QN (DFFARX1)	0.940	0.024	0.045	0.045r
wptr_full/U11/A (INVX1)		0.024	0.014	0.059r
wptr_full/U11/Y (INVX1)	1.946	0.021	0.013	0.073f
wptr_full/U6/A1 (AND2X1)		0.021	0.067	0.139f
wptr_full/U6/Y (AND2X1)	1.764	0.017	0.024	0.164f
wptr_full/U4/A1 (XOR2X1)		0.017	0.061	0.224f
wptr_full/U4/Y (XOR2X1)	2.977wptr_	0.021wptr_	0.021wptr_	0.021wptr_

data required time 0.981
data arrival time -0.434

slack (MET) 0.547

When all the tab close,

DC Analysis			
Startpoint	Endpoint	Path Group	Timing Slack
wptr_full/wbin_reg[0]	wptr_full/wptr_reg[1]	wclk	0.247
wptr_full/wbin_reg[0]	wptr_full/wptr_reg[0]	wclk	0.434
wptr_full/wbin_reg[0]	wptr_full/wfull_reg	wclk	0.156
wptr_full/wbin_reg[0]	wptr_full/wbin_reg[2]	wclk	0.362
wptr_full/wbin_reg[0]	wptr_full/wbin_reg[1]	wclk	0.547
wptr_full/wbin_reg[0]	wptr_full/wbin_reg[0]	wclk	0.724
wptr_full/wfull_reg	wfull	OUTPUTS	0.815
rptr_empty/rempty_reg	rptr_empty/rptr_reg[2]	rcclk	0.013
rptr_empty/rempty_reg	rptr_empty/rptr_reg[1]	rcclk	-0.040
rptr_empty/rempty_reg	rptr_empty/rptr_reg[0]	rcclk	0.055
rptr_empty/rempty_reg	rptr_empty/rempty_reg	rcclk	-0.066
rptr_empty/rempty_reg	rptr_empty/rbin_reg[2]	rcclk	0.013
rptr_empty/rempty_reg	rptr_empty/rbin_reg[1]	rcclk	0.002
rptr_empty/rbin_reg[0]	rptr_empty/rbin_reg[0]	rcclk	0.208
rptr_empty/rempty_reg	rempty	OUTPUTS	0.292
wptr_full/wfull_reg	fifomem/mem_reg[3][3]	wclk	0.035
wdata[3]	fifomem/mem_reg[3][3]	INPUTS	0.645
wptr_full/wfull_reg	fifomem/mem_reg[3][2]	wclk	0.035
wdata[2]	fifomem/mem_reg[3][2]	INPUTS	0.645
wptr_full/wfull_reg	fifomem/mem_reg[3][1]	wclk	0.035
wdata[1]	fifomem/mem_reg[3][1]	INPUTS	0.645
wdata[0]	fifomem/mem_reg[3][0]	INPUTS	0.645
wptr_full/wfull_reg	fifomem/mem_reg[3][0]	wclk	0.035
wdata[3]	fifomem/mem_reg[2][3]	INPUTS	0.643
wptr_full/wfull_reg	fifomem/mem_reg[2][3]	wclk	0.039
wptr_full/wfull_reg	fifomem/mem_reg[2][2]	wclk	0.039
wdata[2]	fifomem/mem_reg[2][2]	INPUTS	0.643
wdata[1]	fifomem/mem_reg[2][1]	INPUTS	0.643
wptr_full/wfull_reg	fifomem/mem_reg[2][1]	wclk	0.039
wptr_full/wfull_reg	fifomem/mem_reg[2][0]	wclk	0.039
wdata[0]	fifomem/mem_reg[2][0]	INPUTS	0.643
wptr_full/wfull_reg	fifomem/mem_reg[1][3]	wclk	0.039
wdata[3]	fifomem/mem_reg[1][3]	INPUTS	0.643
wdata[2]	fifomem/mem_reg[1][2]	INPUTS	0.643
wptr_full/wfull_reg	fifomem/mem_reg[1][2]	wclk	0.039
wdata[1]	fifomem/mem_reg[1][1]	INPUTS	0.643
wptr_full/wfull_reg	fifomem/mem_reg[1][1]	wclk	0.039
wdata[0]	fifomem/mem_reg[1][0]	INPUTS	0.643
wptr_full/wfull_reg	fifomem/mem_reg[0][3]	wclk	0.039
wdata[3]	fifomem/mem_reg[0][3]	INPUTS	0.643
wdata[2]	fifomem/mem_reg[0][2]	INPUTS	0.643
wptr_full/wfull_reg	fifomem/mem_reg[0][2]	wclk	0.039
wdata[1]	fifomem/mem_reg[0][1]	INPUTS	0.643
wptr_full/wfull_reg	fifomem/mem_reg[0][1]	wclk	0.039
wdata[0]	fifomem/mem_reg[0][0]	INPUTS	0.643
wptr_full/wfull_reg	fifomem/mem_reg[0][0]	wclk	0.039