Weekly Report

Linyi Hong Mar, 25 2018 Week11

Summary:

Now I am doing working on the MCMM_rpt assignment. I am almost finish the right-hand side and Xiaoqiao is working on the left-hand search part. We will combine them together to get a better performance. But I am not fully understand the request for interaction between different GUI report.

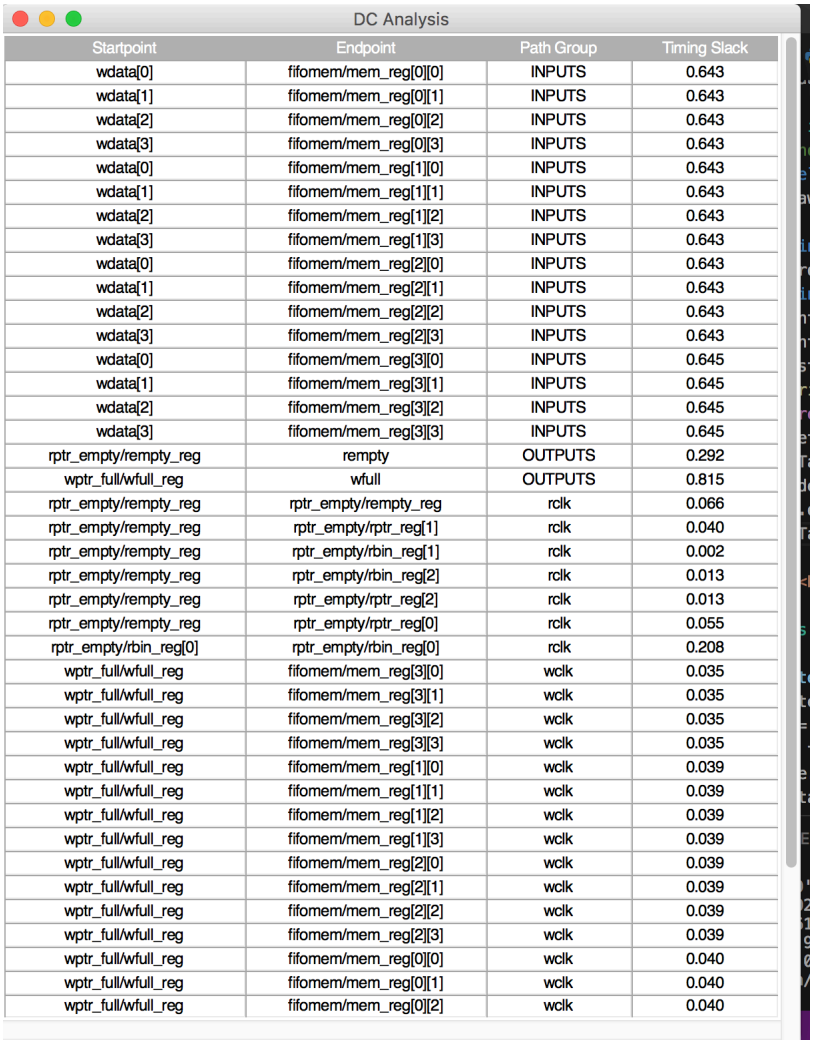
Issue:

For the Detail report, what kind of information are need to be sorted? I try to convert the part that I think it need to be compare, but I am not sure. Since I found there are some unchanged information or non-numerical information such as the startpoint, the library and so on, so I just simply put a textbox there. But I will update it later if getting more specific requirement.

For the interaction between different GUI interface, can you state the behavior more detail? I am sure that I understand it correctly or not.

Data:

Beginning



Startpoint	Endpoint	Path Group	Timing Slack
wdata[0]	fifomem/mem_reg[0][0]	INPUTS	0.643
wdata[1]	fifomem/mem_reg[0][1]	INPUTS	0.643
wdata[2]	fifomem/mem_reg[0][2]	INPUTS	0.643
wdata[3]	fifomem/mem_reg[0][3]	INPUTS	0.643
wdata[0]	fifomem/mem_reg[1][0]	INPUTS	0.643
wdata[1]	fifomem/mem_reg[1][1]	INPUTS	0.643
wdata[2]	fifomem/mem_reg[1][2]	INPUTS	0.643
wdata[3]	fifomem/mem_reg[1][3]	INPUTS	0.643
wdata[0]	fifomem/mem_reg[2][0]	INPUTS	0.643
wdata[1]	fifomem/mem_reg[2][1]	INPUTS	0.643
wdata[2]	fifomem/mem_reg[2][2]	INPUTS	0.643
wdata[3]	fifomem/mem_reg[2][3]	INPUTS	0.643
wdata[0]	fifomem/mem_reg[3][0]	INPUTS	0.645
wdata[1]	fifomem/mem_reg[3][1]	INPUTS	0.645
wdata[2]	fifomem/mem_reg[3][2]	INPUTS	0.645
wdata[3]	fifomem/mem_reg[3][3]	INPUTS	0.645
rptr_empty/rempty_reg	rempty	OUTPUTS	0.292
wptr_full/wfull_reg	wfull	OUTPUTS	0.815
rptr_empty/rempty_reg	rptr_empty/rempty_reg	rclk	0.066
rptr_empty/rempty_reg	rptr_empty/rptr_reg[1]	rclk	0.040
rptr_empty/rempty_reg	rptr_empty/rbin_reg[1]	rclk	0.002
rptr_empty/rempty_reg	rptr_empty/rbin_reg[2]	rclk	0.013
rptr_empty/rempty_reg	rptr_empty/rptr_reg[2]	rclk	0.013
rptr_empty/rempty_reg	rptr_empty/rptr_reg[0]	rclk	0.055
rptr_empty/rbin_reg[0]	rptr_empty/rbin_reg[0]	rclk	0.208
wptr_full/wfull_reg	fifomem/mem_reg[3][0]	wclk	0.035
wptr_full/wfull_reg	fifomem/mem_reg[3][1]	wclk	0.035
wptr_full/wfull_reg	fifomem/mem_reg[3][2]	wclk	0.035
wptr_full/wfull_reg	fifomem/mem_reg[3][3]	wclk	0.035
wptr_full/wfull_reg	fifomem/mem_reg[1][0]	wclk	0.039
wptr_full/wfull_reg	fifomem/mem_reg[1][1]	wclk	0.039
wptr_full/wfull_reg	fifomem/mem_reg[1][2]	wclk	0.039
wptr_full/wfull_reg	fifomem/mem_reg[1][3]	wclk	0.039
wptr_full/wfull_reg	fifomem/mem_reg[2][0]	wclk	0.039
wptr_full/wfull_reg	fifomem/mem_reg[2][1]	wclk	0.039
wptr_full/wfull_reg	fifomem/mem_reg[2][2]	wclk	0.039
wptr_full/wfull_reg	fifomem/mem_reg[2][3]	wclk	0.039
wptr_full/wfull_reg	fifomem/mem_reg[0][0]	wclk	0.040
wptr_full/wfull_reg	fifomem/mem_reg[0][1]	wclk	0.040
wptr_full/wfull_reg	fifomem/mem_reg[0][2]	wclk	0.040

After choosing one report

The top table is listing all the Startpoint, endpoint, Path Group and Timing Slack.
The bottom frame is showing the detail

DC Analysis

Startpoint	Endpoint	Path Group	Timing Slack
wdata[0]	fifomem/mem_reg[0][0]	INPUTS	0.643
wdata[1]	fifomem/mem_reg[0][1]	INPUTS	0.643
wdata[2]	fifomem/mem_reg[0][2]	INPUTS	0.643
wdata[3]	fifomem/mem_reg[0][3]	INPUTS	0.643
wdata[0]	fifomem/mem_reg[1][0]	INPUTS	0.643
wdata[1]	fifomem/mem_reg[1][1]	INPUTS	0.643
wdata[2]	fifomem/mem_reg[1][2]	INPUTS	0.643
wdata[3]	fifomem/mem_reg[1][3]	INPUTS	0.643
wdata[0]	fifomem/mem_reg[2][0]	INPUTS	0.643
wdata[1]	fifomem/mem_reg[2][1]	INPUTS	0.643
wdata[2]	fifomem/mem_reg[2][2]	INPUTS	0.643
wdata[3]	fifomem/mem_reg[2][3]	INPUTS	0.643

Startpoint: wdata[0] (input port clocked by wclk)
Endpoint: fifomem/mem_reg[0][0] (rising edge-triggered flip-flop clocked by wclk)
Path Group: INPUTS
Path Type: max

Des/Clust/Port Wire Load Model Library
---
fifo1 8000 saed32rvt_ff1p16v125c
fifomem_DATASIZE4_ADDRSIZE2
ForQA saed32rvt_ff1p16v125c

Point	Cap	Trans	Incr	Path
clock wclk (rise edge)			0.000	0.000
clock network delay (ideal)			0.000	0.000
input external delay			0.100	0.100r
wdata[0] (in)	1.879	0.000	0.000	0.100r
fifomem/wdata[0] (fifomem_DATASIZE4_ADDRSIZE2)			0.000	0.100r
fifomem/U24/A2 (AO22X1)		0.000	0.196	0.296r
fifomem/U24/Y (AO22X1)	0.734	0.025	0.031	0.326r
fifomem/mem_reg[0][0]/D (DFFX1)		0.025	0.011	0.338r
data arrival time				0.338
clock wclk (rise edge)			1.000	1.000
clock network delay (ideal)			0.000	1.000
fifomem/mem_reg[0][0]/CLK (DFFX1)			0.000	1.000r

data required time 0.981
data arrival time -0.338
---
slack (MET) 0.643

The detail table is only showing the red block content.

```
Startpoint: wdata[0] (input port clocked by wclk)
Endpoint: fifomem/mem_reg[0][0]
          (rising edge-triggered flip-flop clocked by wclk)
Path Group: INPUTS
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
fifo1              8000                  saed32rvt_ff1p16v125c
fifomem_DATASIZE4_ADDRSIZE2
                   ForQA                 saed32rvt_ff1p16v125c

Point                                          Cap     Trans      Incr       Path
-----------------------------------------------------------------------------------
clock wclk (rise edge)                                            0.000      0.000
clock network delay (ideal)                                       0.000      0.000
input external delay                                              0.100      0.100 r
wdata[0] (in)                                  1.879     0.000    0.000      0.100 r
fifomem/wdata[0] (fifomem_DATASIZE4_ADDRSIZE2)                    0.000      0.100 r
fifomem/U24/A2 (AO22X1)                                0.000      0.196      0.296 r
fifomem/U24/Y (AO22X1)                         0.734   0.025      0.031      0.326 r
fifomem/mem_reg[0][0]/D (DFFX1)                        0.025      0.011      0.338 r
data arrival time                                                            0.338

clock wclk (rise edge)                                            1.000      1.000
clock network delay (ideal)                                       0.000      1.000
fifomem/mem_reg[0][0]/CLK (DFFX1)                                 0.000      1.000 r
library setup time                                               -0.019      0.981
data required time                                                           0.981
-----------------------------------------------------------------------------------
data required time                                                           0.981
data arrival time                                                           -0.338
-----------------------------------------------------------------------------------
slack (MET)                                                                  0.643
```

For the top table, the value can be sort by Startpoint, Endpoint, Path group and Timing slack.

For the bottom table, the value can be sort by Point, Cap, Trans, Incr and Path.