Lab 2

Four to Sixteen Decoder

Group G

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ECE 3300L.01

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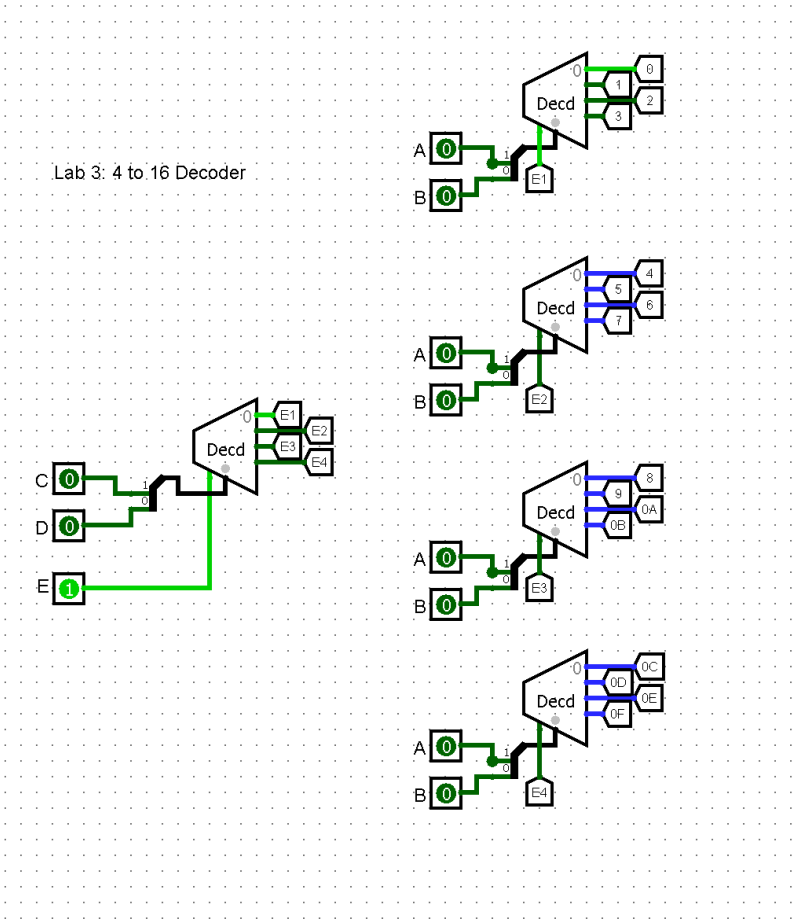
Problem

Create a 4 to 16 decoder using the gate level implementation and demonstrate on an FPGA board.

Code Detail

The Verilog code uses 5, 2 to 4 decoders built from logic gates to implement a 4 to 16 decoder that turns on a certain LED when triggered on the FPGA - binary. The two lower bits of the input are internally wired to 4 decoders, while the fifth decoder uses the higher two bits to control which 4 decoders are active based on the fifth decoder's output. The four decoders output is then represented as the output of the decoder via sixteen LEDs.

Schematic



(Input D is MSB, A is LSB)

Results

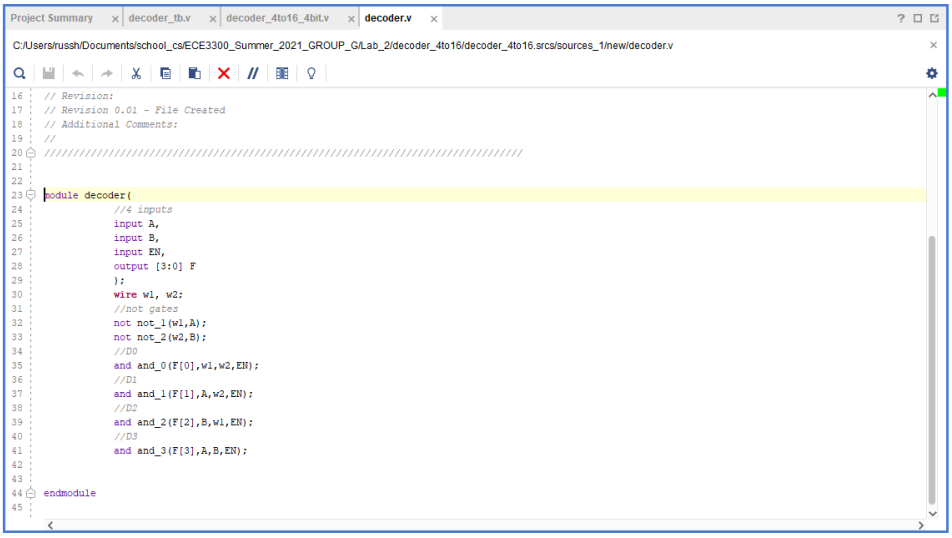


Figure 1: Verilog Code for 2 to 4 Decoder

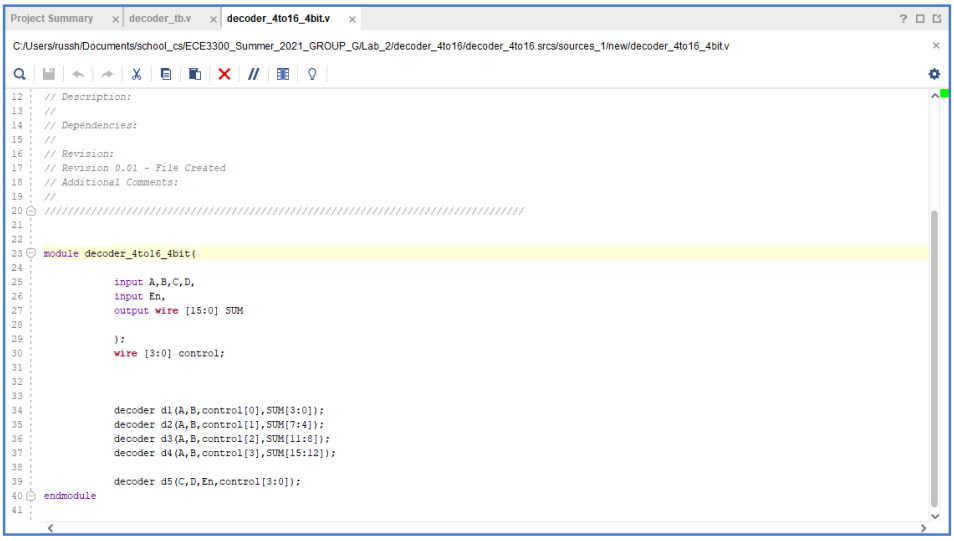


Figure 2: Verilog Code for 4 to 16 Decoder

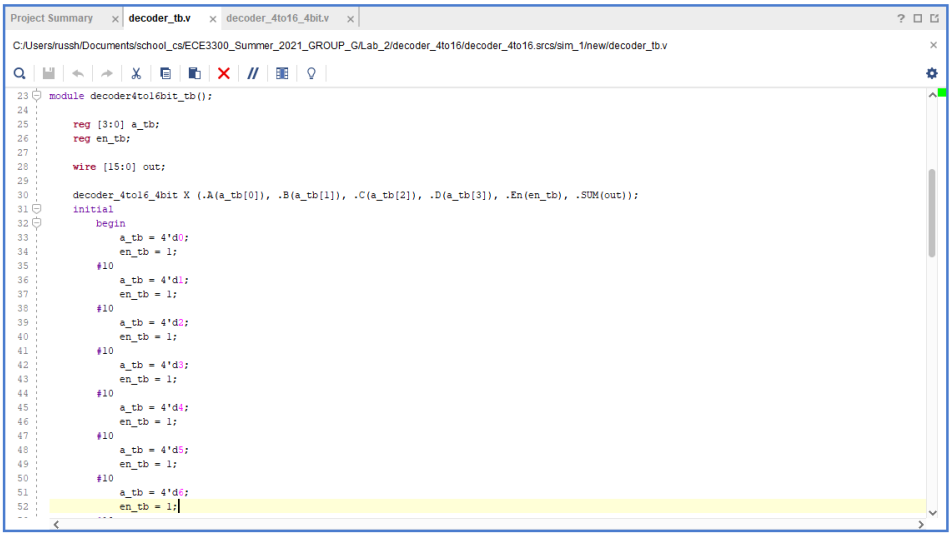


Figure 3: Testbench for the First Portion of Code

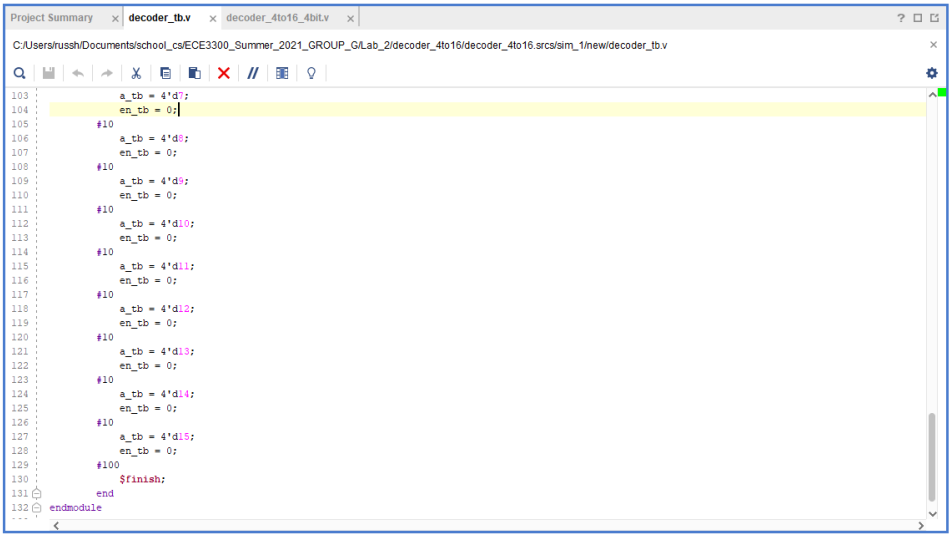


Figure 4: Testbench End-portion of Code

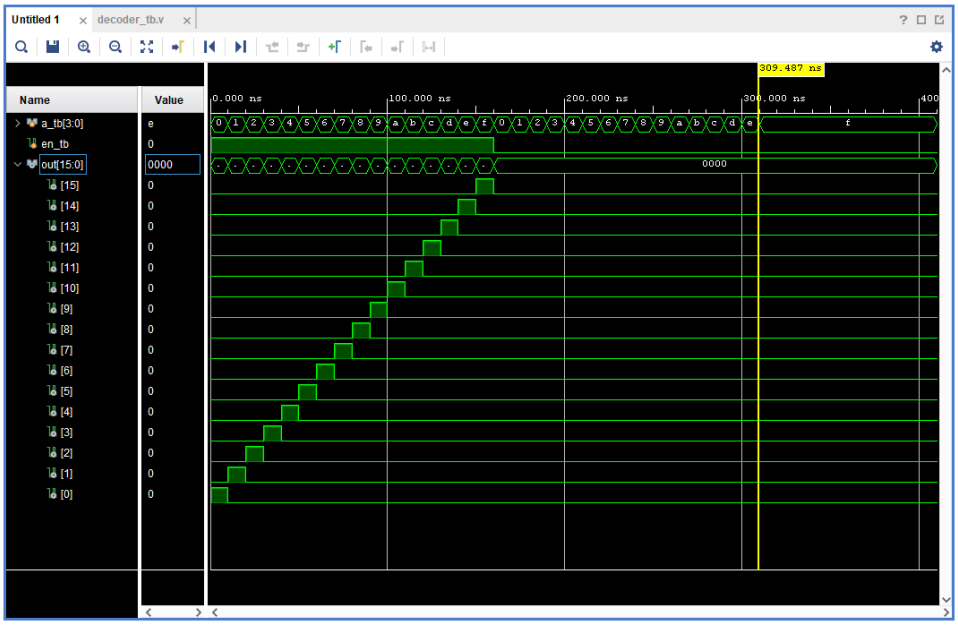


Figure 5: Behavioral simulation

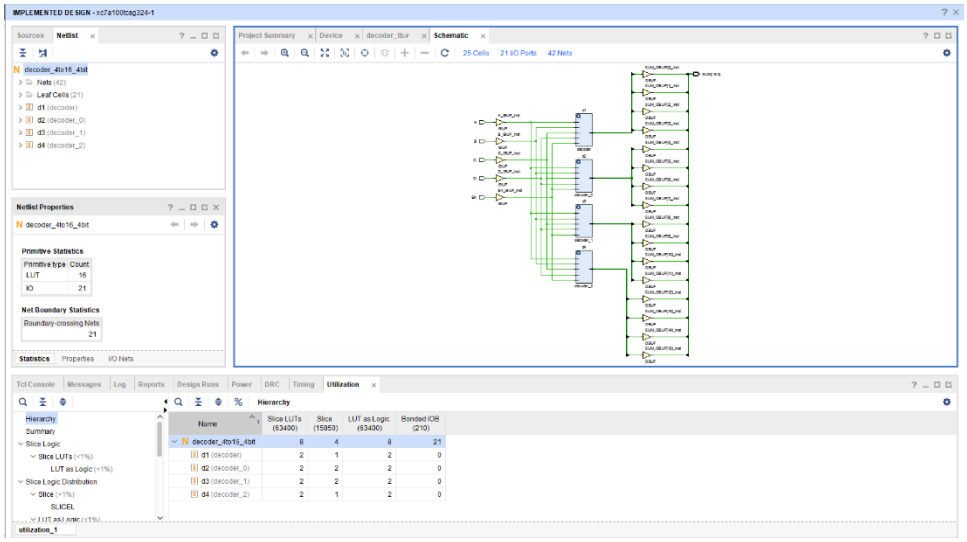


Figure 6: Utilization of Resources

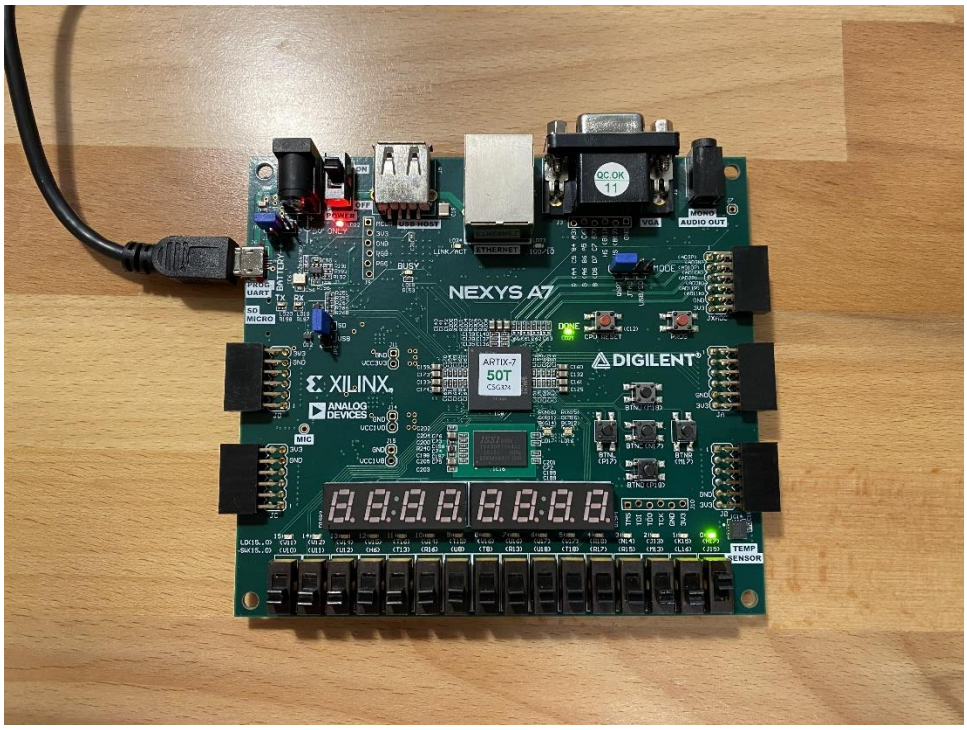


Figure 7: Enable Pin is High and the LED at 0 is ON

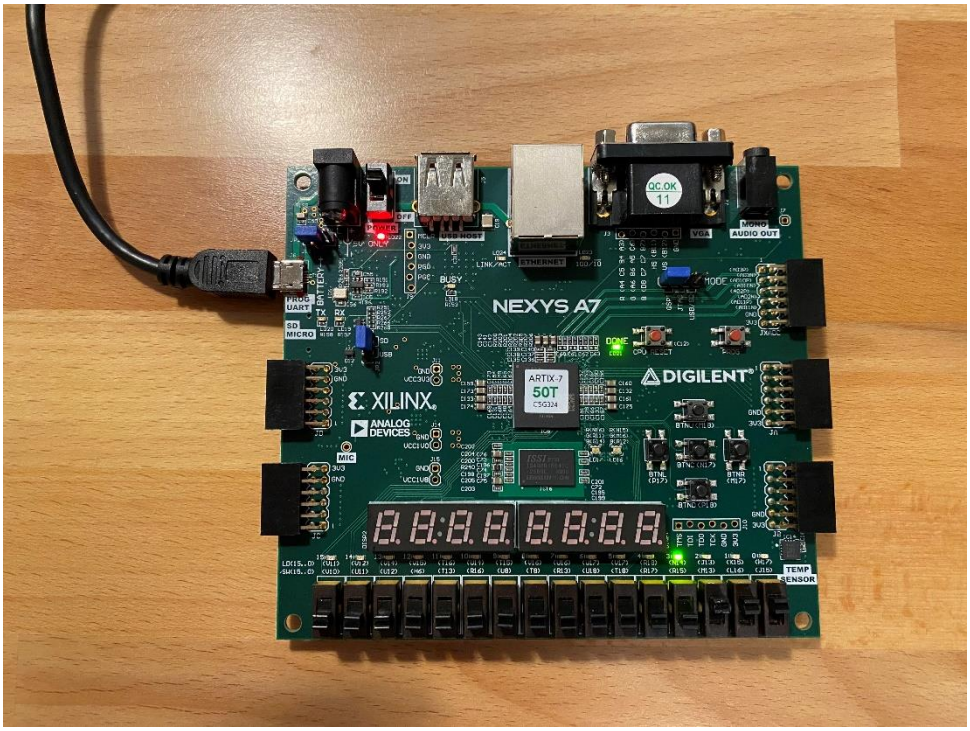


Figure 8: Enable Pin is High and the LED at 3 is ON

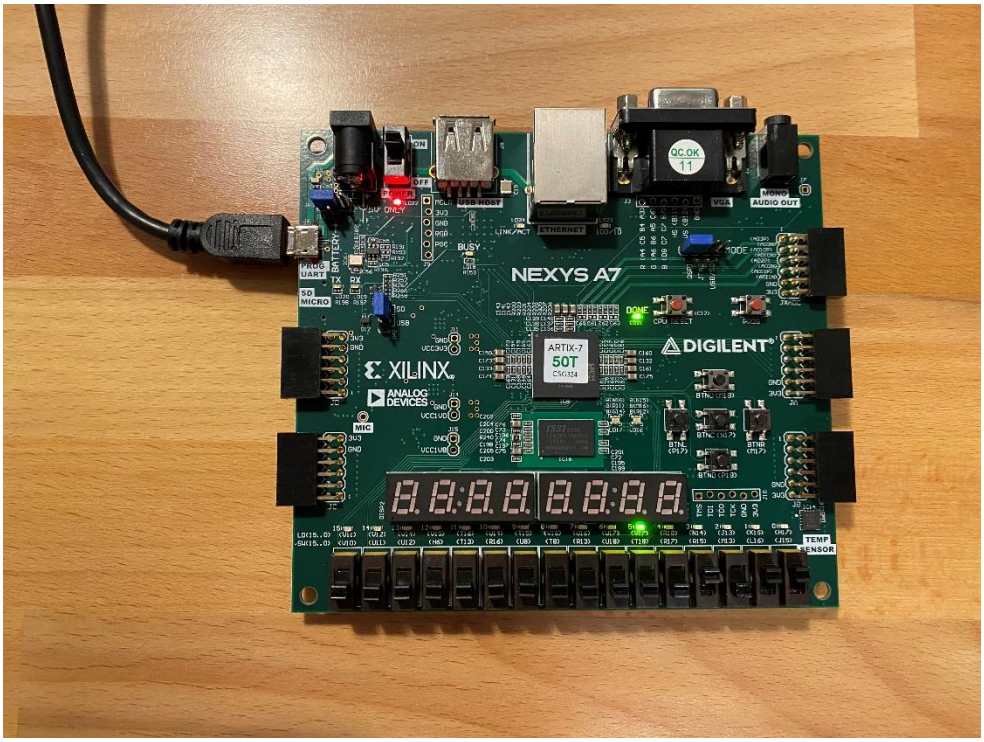


Figure 9: Enable Pin is High and the LED at 5 is ON

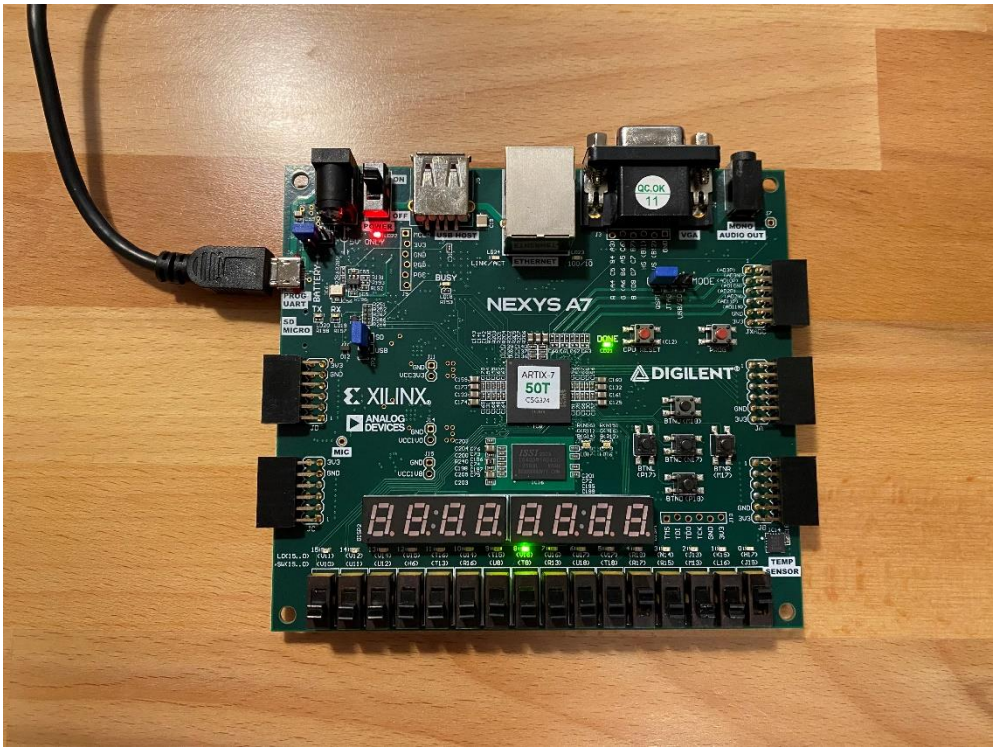


Figure 10: Enable Pin is High and the LED at 8 is ON

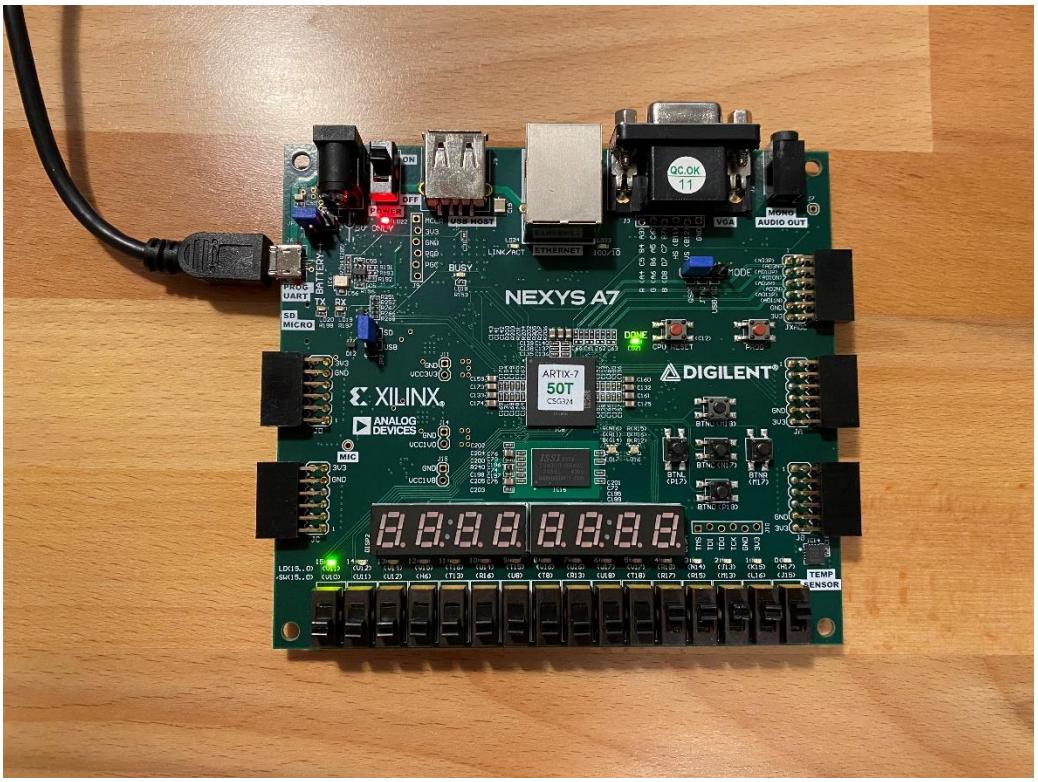


Figure 11: Enable Pin is High and the LED at 15 is ON

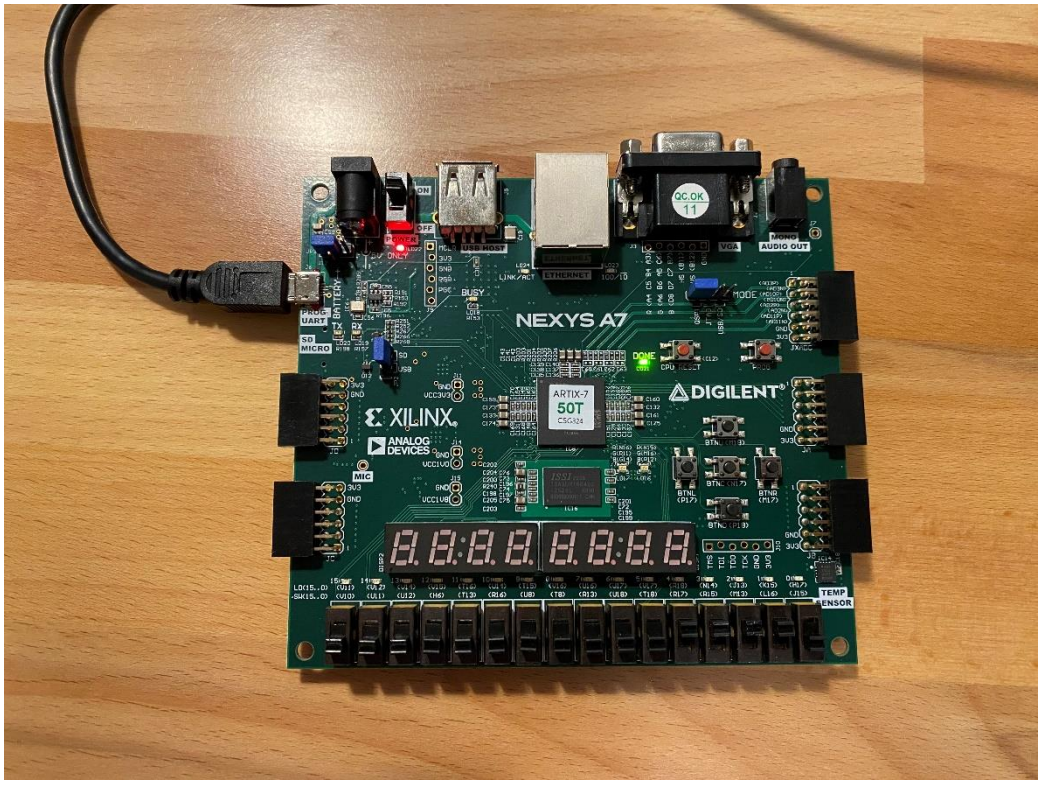


Figure 12: Enable Pin is Low and all LEDs are OFF

Discussion

The simulation displays the expected output for the decoder. When the enable is high, the correct decoder output is displayed based on the input. The implementation on the FPGA board also behaves as expected. The switches cause the correct LEDs to light without any issue. Each possible combination of switches is accounted for in the simulation and there aren't any edge cases we can find.

Conclusion

The implementation that we used works well, without any bugs that we could find. The implementation may be improved by using other types of modeling, such as dataflow modeling or behavioral modeling. The complexity of the current implementation may also be reduced by using other methods of modeling the desired behavior.

Work Distribution

Russell: Lab Report, Video and Photos regarding the FPGA, Source Code and Testbench.

Philbert: Lab Report, Video and Photos regarding the FPGA, Source Code and Testbench.

Paul: Lab Report, Video and Photos regarding the FPGA, Source Code and Testbench.