Lab 1
Four Bit Two-to-One Multiplexer

Group G
Chang, Philbert (013179257)
Hua, Russell (013184015)
Thai, Paul (014760252)

ECE 3300L.01
Professor Aly

06/17/2021

Problem

Create a two-to-one multiplexer that takes 2 four-bit inputs and uses 1 select pin to output one of the four-bit inputs.

Code Detail

The main goal is to choose what input is shown based on what the select is set to. We decided to create structural modeling and behavioral modeling implementations to see if there are any differences.

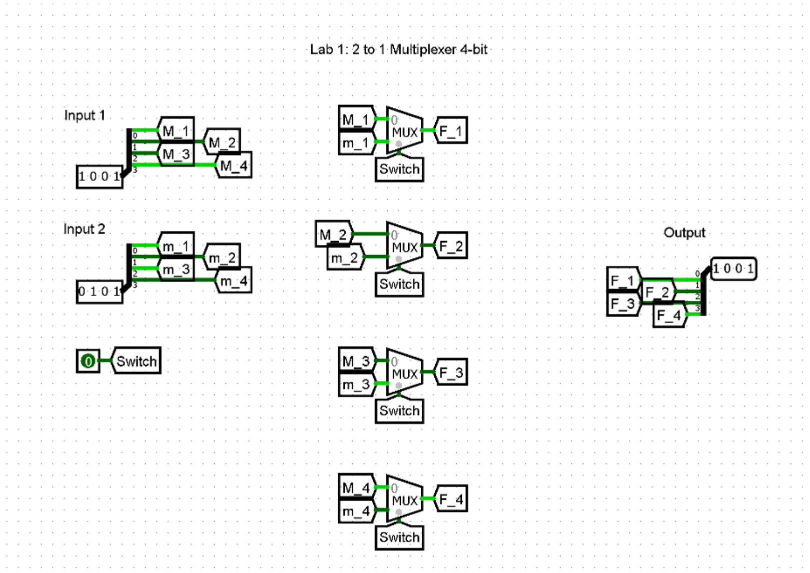
<u>Behavioral Modeling:</u>

This method uses a switch case statement to assign the input to the output. If the case s (for select) is 0, then assign the output to the first input: a. If s is 1, then assign the output to the second input: b. Inputs A and B use 4 bits as is output C. The resulting code is only a few lines and is quite simple.

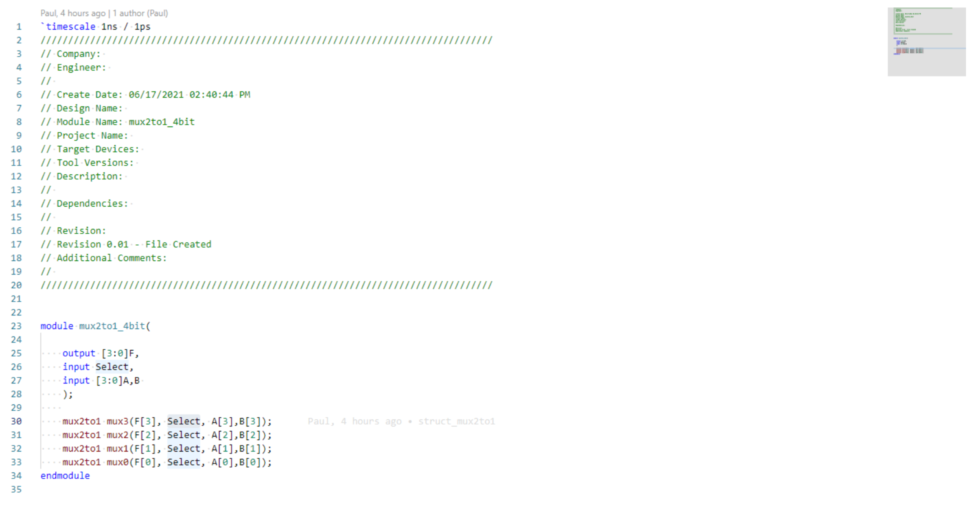
<u>Structural Modeling:</u>

In this method, we used a schematic of a basic one-bit 2-to-1 mux developed using logic gates. We start by writing the verilog code for the one-bit 2-to-1 mux in the module named “mux2to1”. After completing that module, we created a new module named “mux2to1_4bit”, which can be seen in Figure 1 in the results. We create a four-bit input and output by instantiating an array of size 4, then assigning each location in the array to 4 different one-bit 2-to-1 muxes.

Schematic



Results



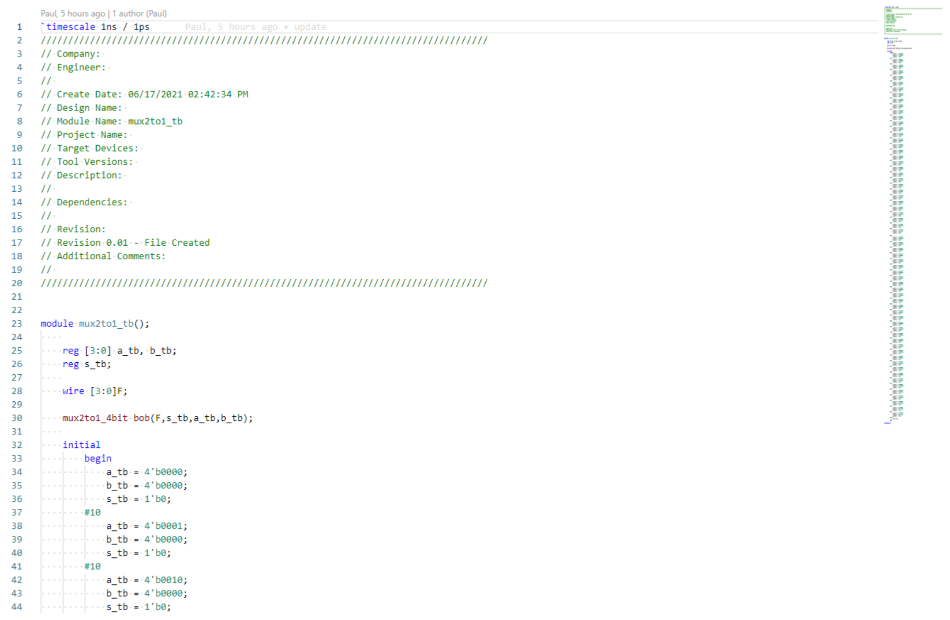
```
Paul, 4 hours ago | 1 author (Paul)
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company: 
// Engineer: 
// 
// Create Date: 06/17/2021 02:40:44 PM
// Design Name: 
// Module Name: mux2to1_4bit
// Project Name: 
// Target Devices: 
// Tool Versions: 
// Description: 
// 
// Dependencies: 
// 
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
// 
//////////////////////////////////////////////////////////////////////////////////


module mux2to1_4bit(

    output [3:0]F,
    input Select,
    input [3:0]A,B 
    );
    
    mux2to1 mux3(F[3], Select, A[3],B[3]);      Paul, 4 hours ago • struct_mux2to1
    mux2to1 mux2(F[2], Select, A[2],B[2]);
    mux2to1 mux1(F[1], Select, A[1],B[1]);
    mux2to1 mux0(F[0], Select, A[0],B[0]);
endmodule

```

Figure 1: Code of Structural Modeling

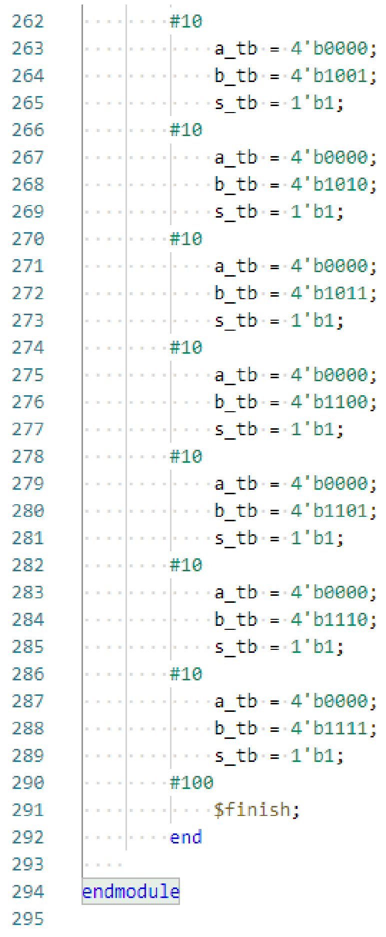


```
Paul, 5 hours ago | 1 author (Paul)
`timescale 1ns / 1ps      Paul, 5 hours ago • update
//////////////////////////////////////////////////////////////////////////////////
// Company: 
// Engineer: 
// 
// Create Date: 06/17/2021 02:42:34 PM
// Design Name: 
// Module Name: mux2to1_tb
// Project Name: 
// Target Devices: 
// Tool Versions: 
// Description: 
// 
// Dependencies: 
// 
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
// 
//////////////////////////////////////////////////////////////////////////////////


module mux2to1_tb();
    
    reg [3:0] a_tb, b_tb;
    reg s_tb;
    
    wire [3:0]F;

    mux2to1_4bit bob(F,s_tb,a_tb,b_tb);
    
    initial
        begin
            a_tb = 4'b0000;
            b_tb = 4'b0000;
            s_tb = 1'b0;
        #10
            a_tb = 4'b0001;
            b_tb = 4'b0000;
            s_tb = 1'b0;
        #10
            a_tb = 4'b0010;
            b_tb = 4'b0000;
            s_tb = 1'b0;
```

Figure 2: Testbench for Structural Modeling [P1]



```
        #10
            a_tb = 4'b0000;
            b_tb = 4'b1001;
            s_tb = 1'b1;
        #10
            a_tb = 4'b0000;
            b_tb = 4'b1010;
            s_tb = 1'b1;
        #10
            a_tb = 4'b0000;
            b_tb = 4'b1011;
            s_tb = 1'b1;
        #10
            a_tb = 4'b0000;
            b_tb = 4'b1100;
            s_tb = 1'b1;
        #10
            a_tb = 4'b0000;
            b_tb = 4'b1101;
            s_tb = 1'b1;
        #10
            a_tb = 4'b0000;
            b_tb = 4'b1110;
            s_tb = 1'b1;
        #10
            a_tb = 4'b0000;
            b_tb = 4'b1111;
            s_tb = 1'b1;
        #100
            $finish;
        end
    
endmodule
```

Figure 3: Testbench for Structural Modeling [P2]

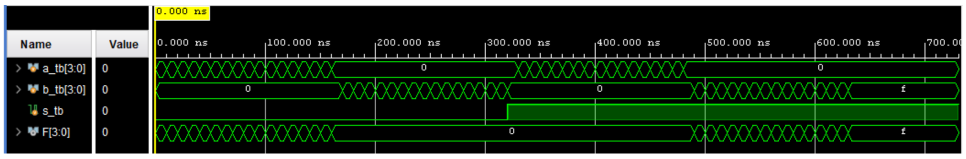
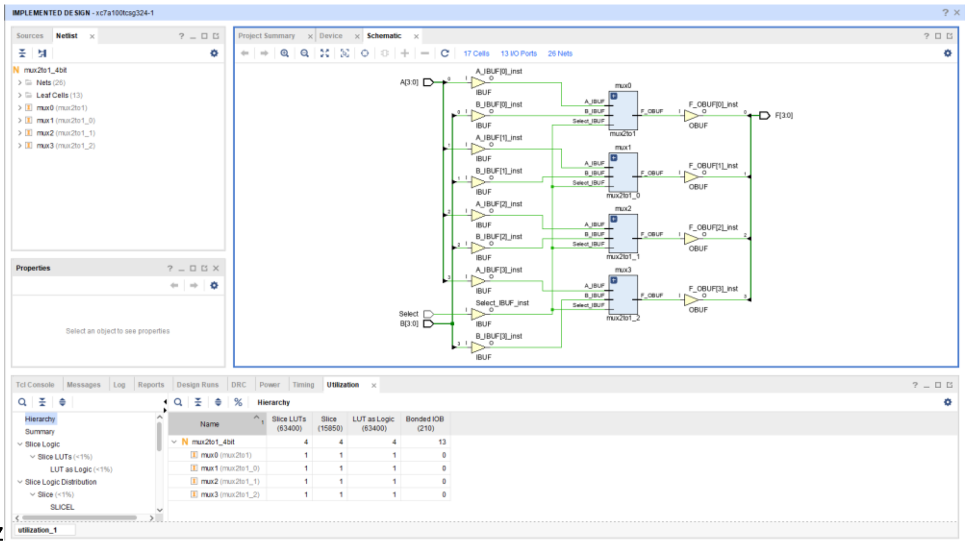


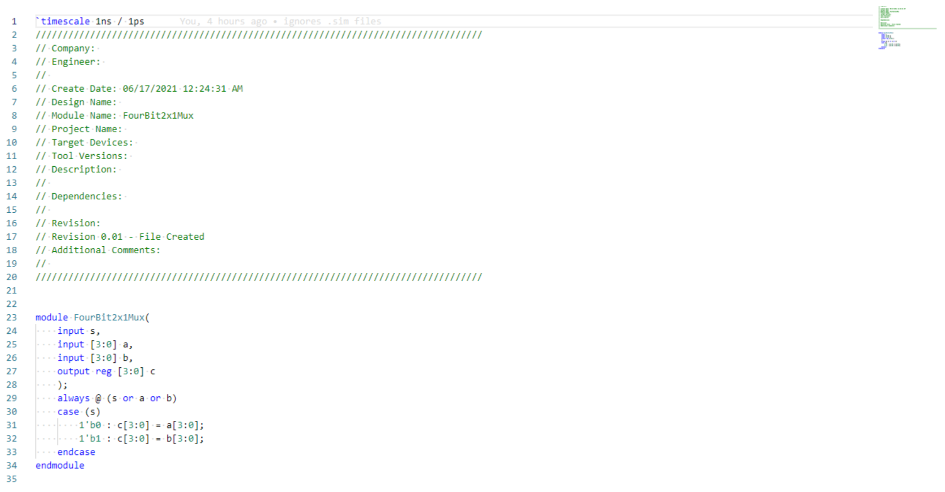
Figure 4: Simulation of Structural Modeling Code



Name	Slice LUTs (63400)	Slice (15850)	LUT as Logic (63400)	Bonded IOB (210)
mux2to1_4bit	4	4	4	13
mux0 (mux2to1)	1	1	1	0
mux1 (mux2to1_0)	1	1	1	0
mux2 (mux2to1_1)	1	1	1	0
mux3 (mux2to1_2)	1	1	1	0

Z

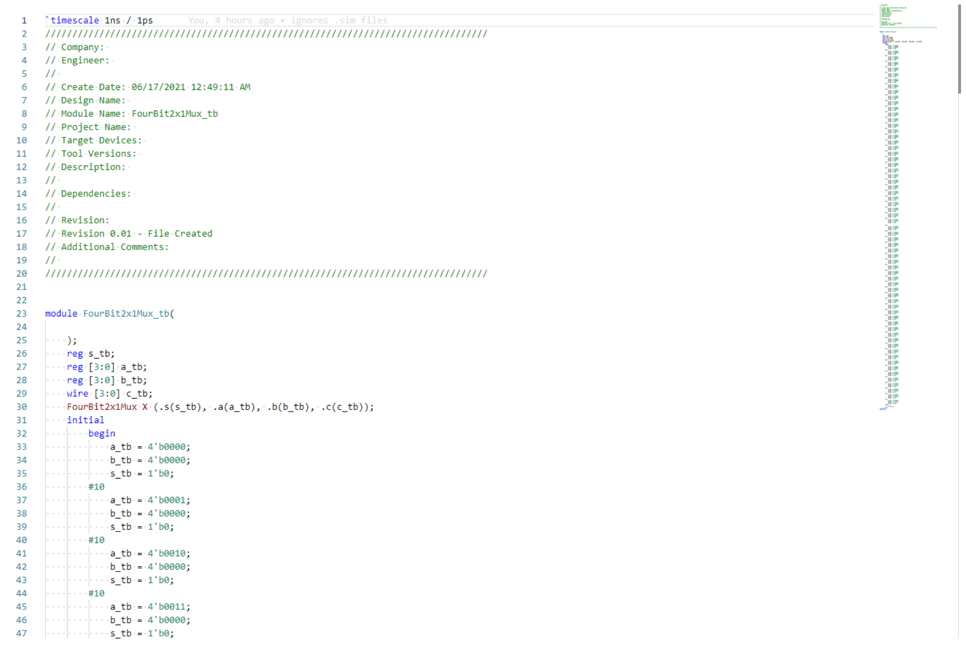
Figure 5: Resource Utilization of Structural Code



```
`timescale 1ns / 1ps      You, 4 hours ago • Ignores .sim files
//////////////////////////////////////////////////////////////////////////////////
// Company: 
// Engineer: 
// 
// Create Date: 06/17/2021 12:24:31 AM
// Design Name: 
// Module Name: FourBit2x1Mux
// Project Name: 
// Target Devices: 
// Tool Versions: 
// Description: 
// 
// Dependencies: 
// 
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
// 
//////////////////////////////////////////////////////////////////////////////////


module FourBit2x1Mux(
    input s,
    input [3:0] a,
    input [3:0] b,
    output reg [3:0] c
    );
    always @ (s or a or b)
    case (s)
        1'b0 : c[3:0] = a[3:0];
        1'b1 : c[3:0] = b[3:0];
    endcase
endmodule
```

Figure 6: Code of Behavioral Modeling

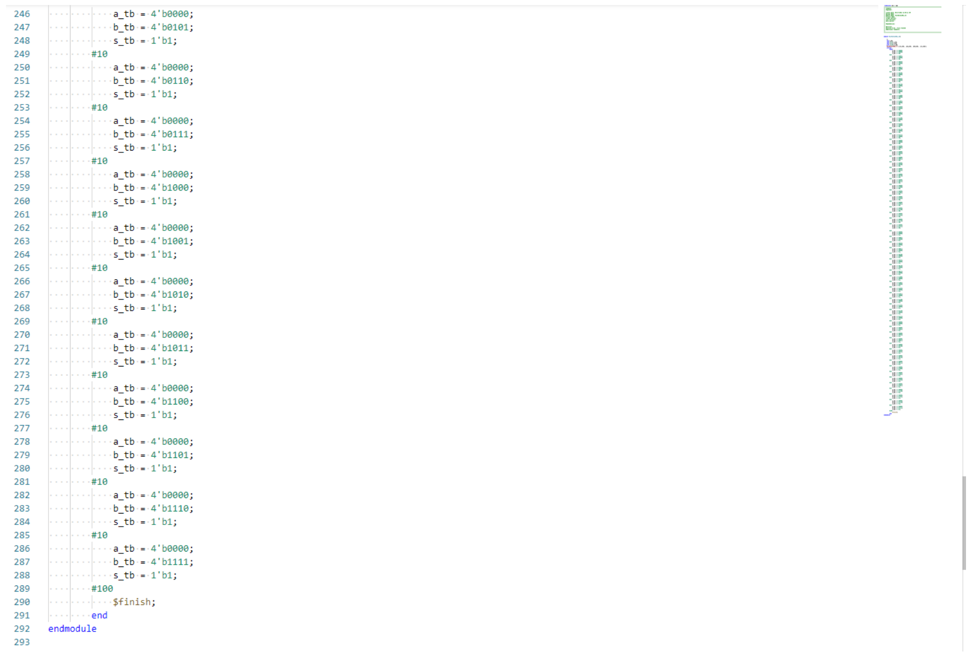


```
`timescale 1ns / 1ps      You, 4 hours ago • ignores .sim files
//////////////////////////////////////////////////////////////////////////////////
// Company: 
// Engineer: 
// 
// Create Date: 06/17/2021 12:49:11 AM
// Design Name: 
// Module Name: FourBit2x1Mux_tb
// Project Name: 
// Target Devices: 
// Tool Versions: 
// Description: 
// 
// Dependencies: 
// 
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
// 
//////////////////////////////////////////////////////////////////////////////////


module FourBit2x1Mux_tb(

    );
    reg s_tb;
    reg [3:0] a_tb;
    reg [3:0] b_tb;
    wire [3:0] c_tb;
    FourBit2x1Mux X (.s(s_tb), .a(a_tb), .b(b_tb), .c(c_tb));
    initial
        begin
            a_tb = 4'b0000;
            b_tb = 4'b0000;
            s_tb = 1'b0;
        #10
            a_tb = 4'b0001;
            b_tb = 4'b0000;
            s_tb = 1'b0;
        #10
            a_tb = 4'b0010;
            b_tb = 4'b0000;
            s_tb = 1'b0;
        #10
            a_tb = 4'b0011;
            b_tb = 4'b0000;
            s_tb = 1'b0;
```

Figure 7: Testbench for Behavioral Modeling [P1]



```
            a_tb = 4'b0000;
            b_tb = 4'b0101;
            s_tb = 1'b1;
        #10
            a_tb = 4'b0000;
            b_tb = 4'b0110;
            s_tb = 1'b1;
        #10
            a_tb = 4'b0000;
            b_tb = 4'b0111;
            s_tb = 1'b1;
        #10
            a_tb = 4'b0000;
            b_tb = 4'b1000;
            s_tb = 1'b1;
        #10
            a_tb = 4'b0000;
            b_tb = 4'b1001;
            s_tb = 1'b1;
        #10
            a_tb = 4'b0000;
            b_tb = 4'b1010;
            s_tb = 1'b1;
        #10
            a_tb = 4'b0000;
            b_tb = 4'b1011;
            s_tb = 1'b1;
        #10
            a_tb = 4'b0000;
            b_tb = 4'b1100;
            s_tb = 1'b1;
        #10
            a_tb = 4'b0000;
            b_tb = 4'b1101;
            s_tb = 1'b1;
        #10
            a_tb = 4'b0000;
            b_tb = 4'b1110;
            s_tb = 1'b1;
        #10
            a_tb = 4'b0000;
            b_tb = 4'b1111;
            s_tb = 1'b1;
        #100
            $finish;
        end
endmodule

```

Figure 8: Testbench for Behavioral Modeling [P2]

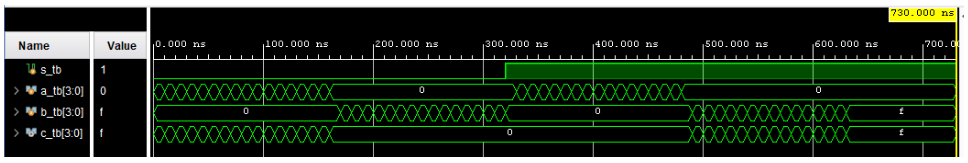
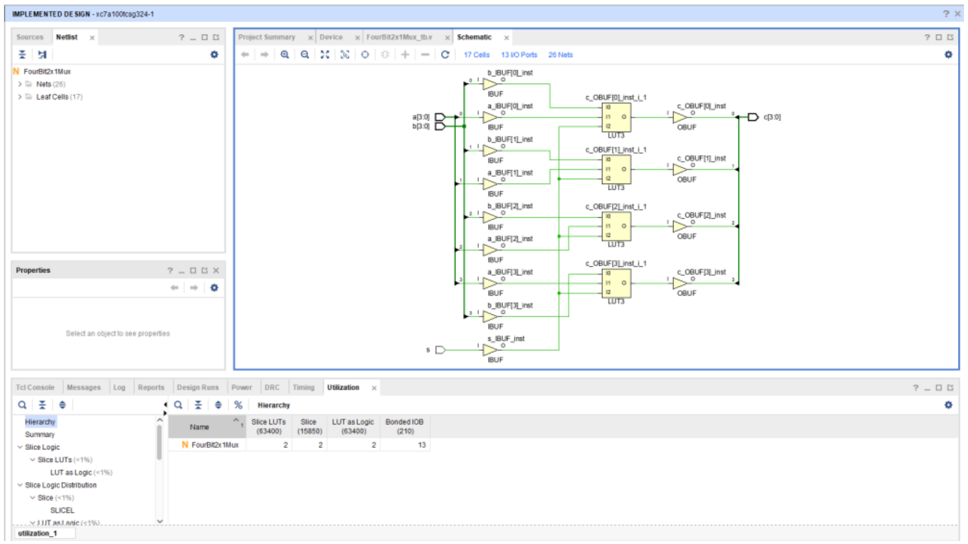


Figure 9: Simulation of Behavioral Model



Name	Slice LUTs (63400)	Slice (15850)	LUT as Logic (63400)	Bonded IOB (210)
FourBit2x1Mux	2	2	2	13

Figure 10: Resource Utilization for Behavioral Modeling

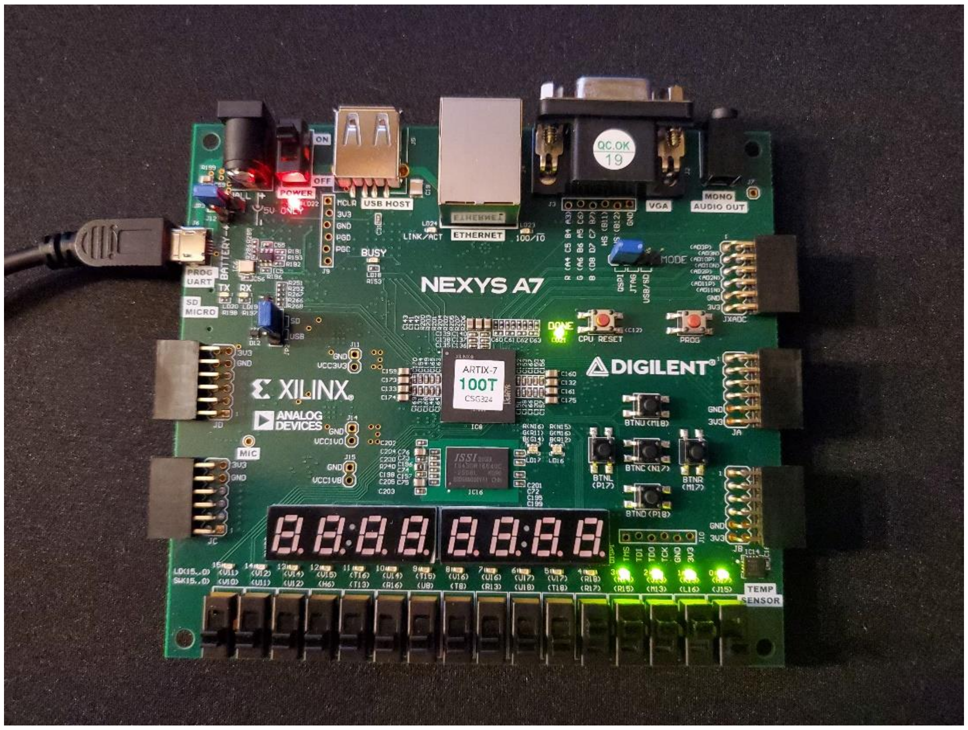


Figure 11: FPGA Board with Select to 0 and Switches 1-4 on

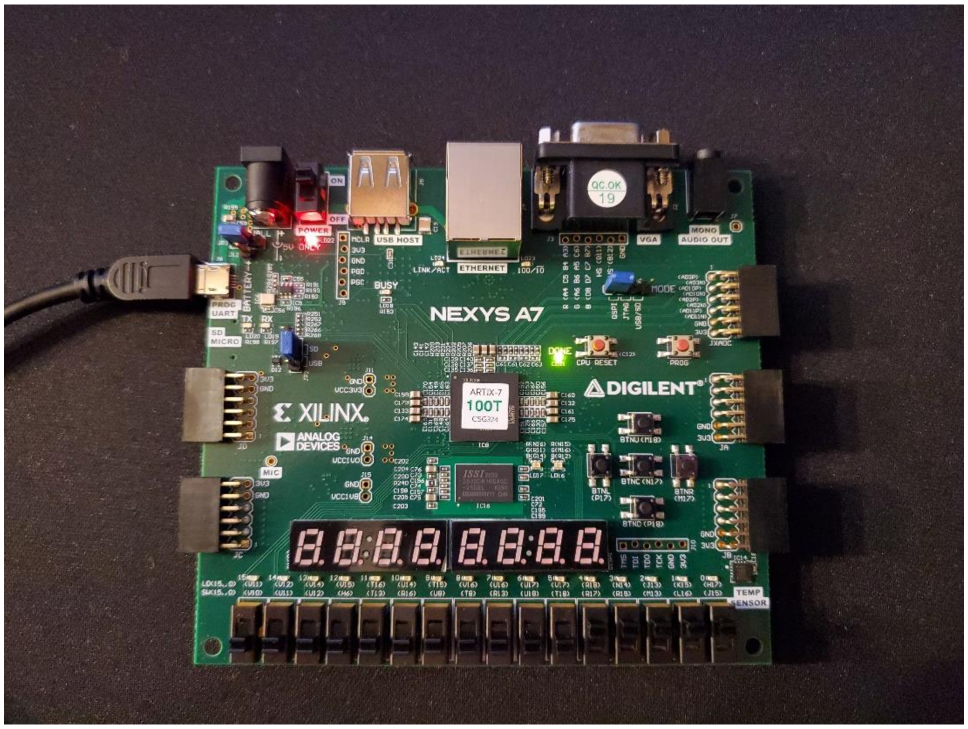


Figure 12: FPGA Board with Select to 1 and Switches 1-4 on

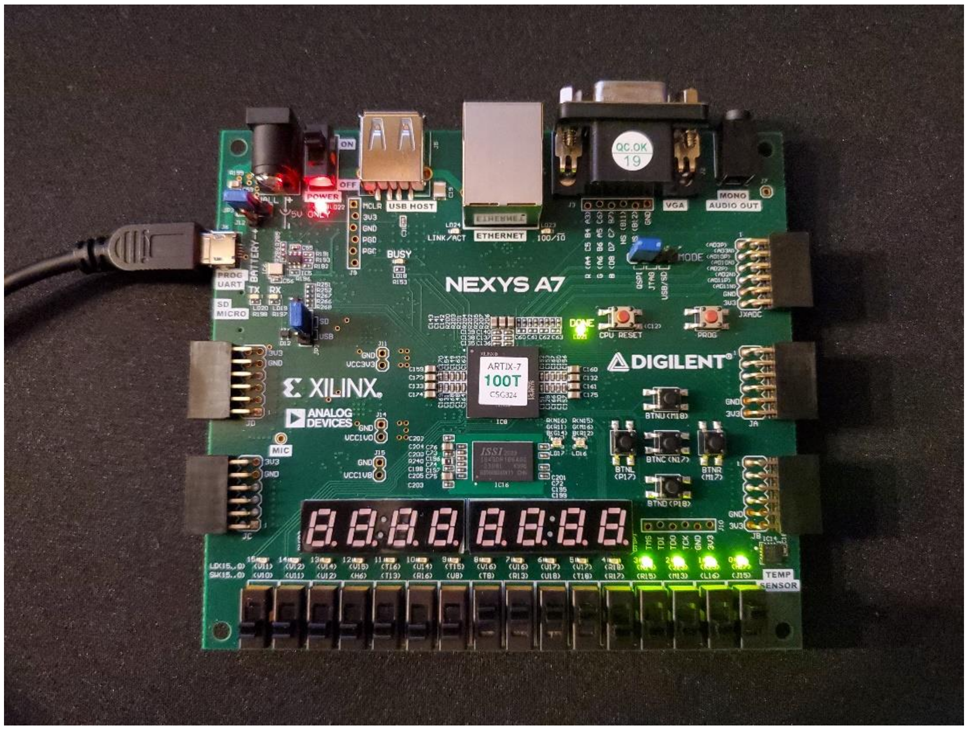


Figure 13: FPGA Board with Select to 1 and Switches 5-8 on

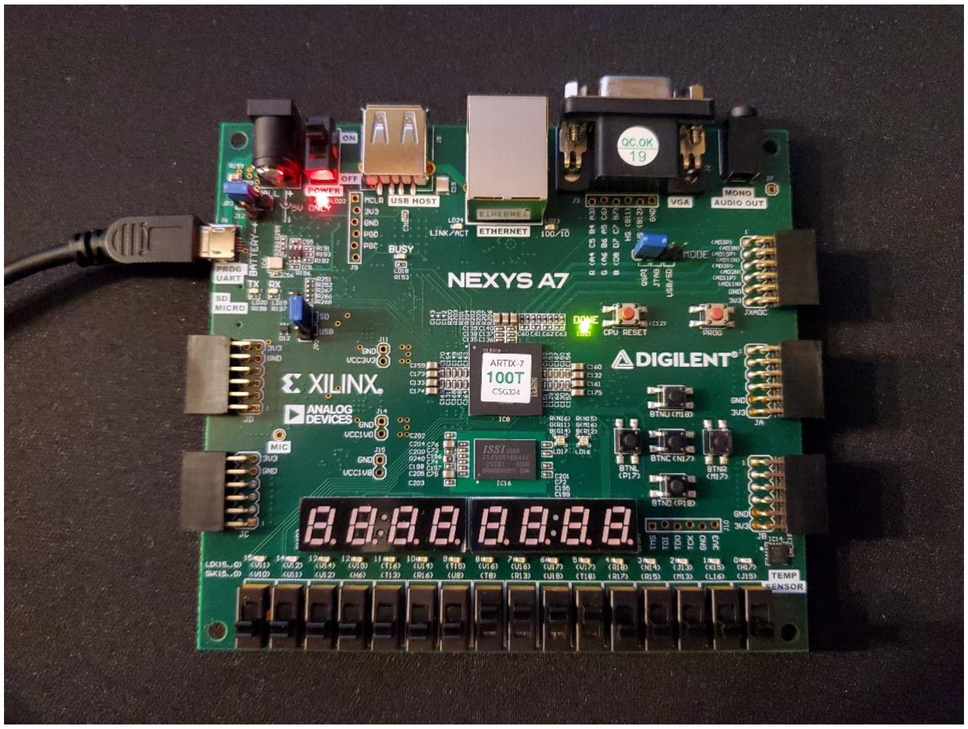


Figure 14: FPGA Board with Select to 0 and Switches 5-8 on

Discussion

Based on the simulation the 2x1 Mux works as expected. The structural and behavioral model works the same, but the behavioral model uses less LUTs: 2 compared with 4. On the physical board, the switches and LEDs behave as expected, with the first switch acting as the select and the next 8 switches being the first and second inputs – four for each.

One downside to behavioral modeling is that there isn't a clear relationship between circuit elements and the code. There isn't a clear structure that would translate to a switch case statement, however through synthesis, one is generated with Vivado.

Conclusion

The 2x1 Mux created in Vivado and programmed to an FPGA works as expected. The code isn't very complex, especially with the behavioral modeling, which used a switch case for what should be displayed as the output. One other implementation that wasn't considered was the data flow modeling, because implementing select input functionality is not straightforward. It seems that depending on the type of modeling used, there may be more efficient designs and it would be interesting to find or optimize better designs for this multiplexor.

Work Distribution

Russell: Testbenches and behavioral modeling code

Philbert: Structural modeling code and code detail

Paul: Structural modeling code and code detail

Everyone Pulled Their Weight on the Lab Report: Team Effort!