



1. Description

1.1. Project

Project Name	VitalSense_Main
Board Name	NUCLEO-L496ZG-P
Generated with:	STM32CubeMX 6.9.1
Date	06/20/2024

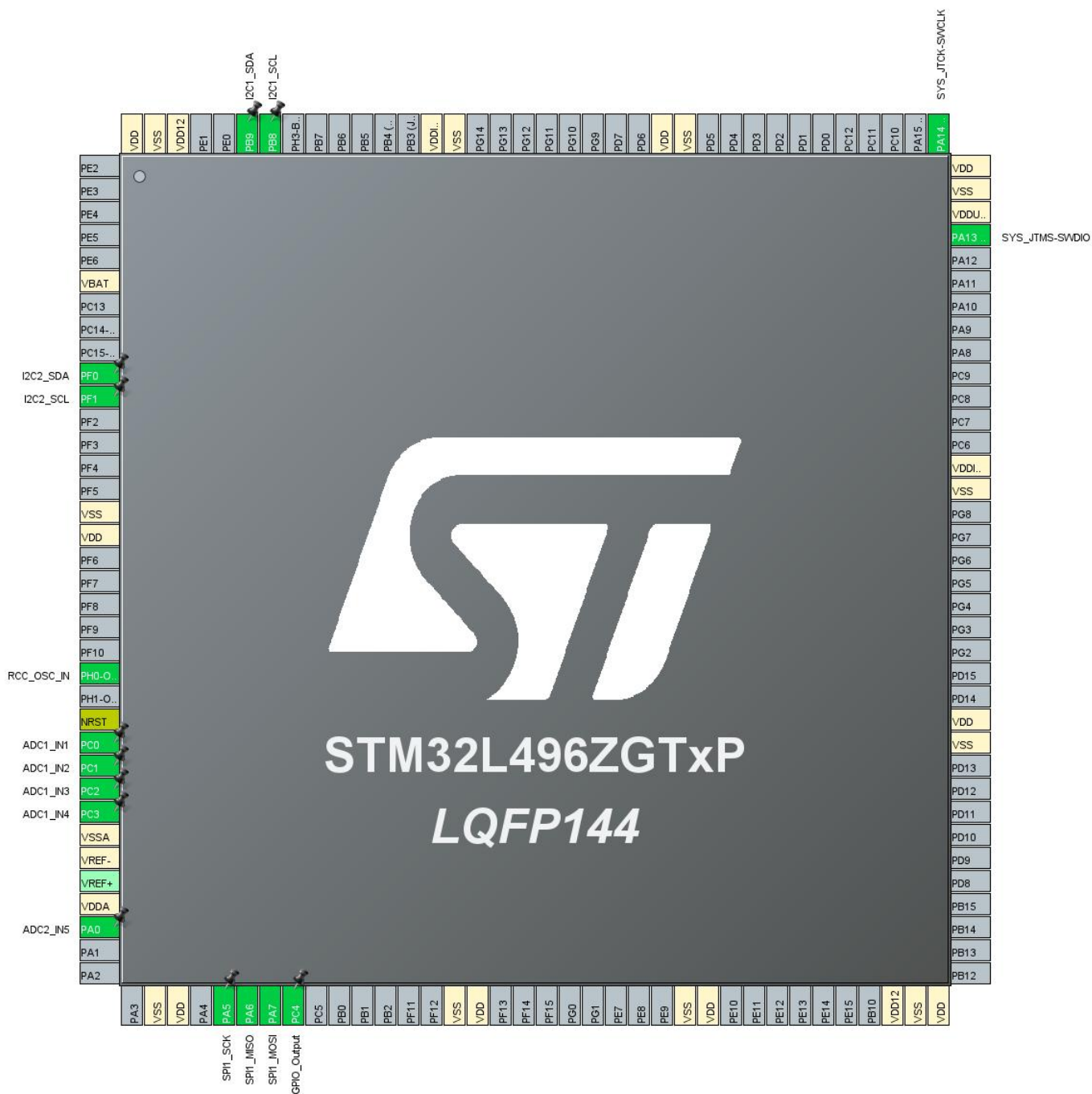
1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L496ZGTxP
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M4
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2. Pinout Configuration



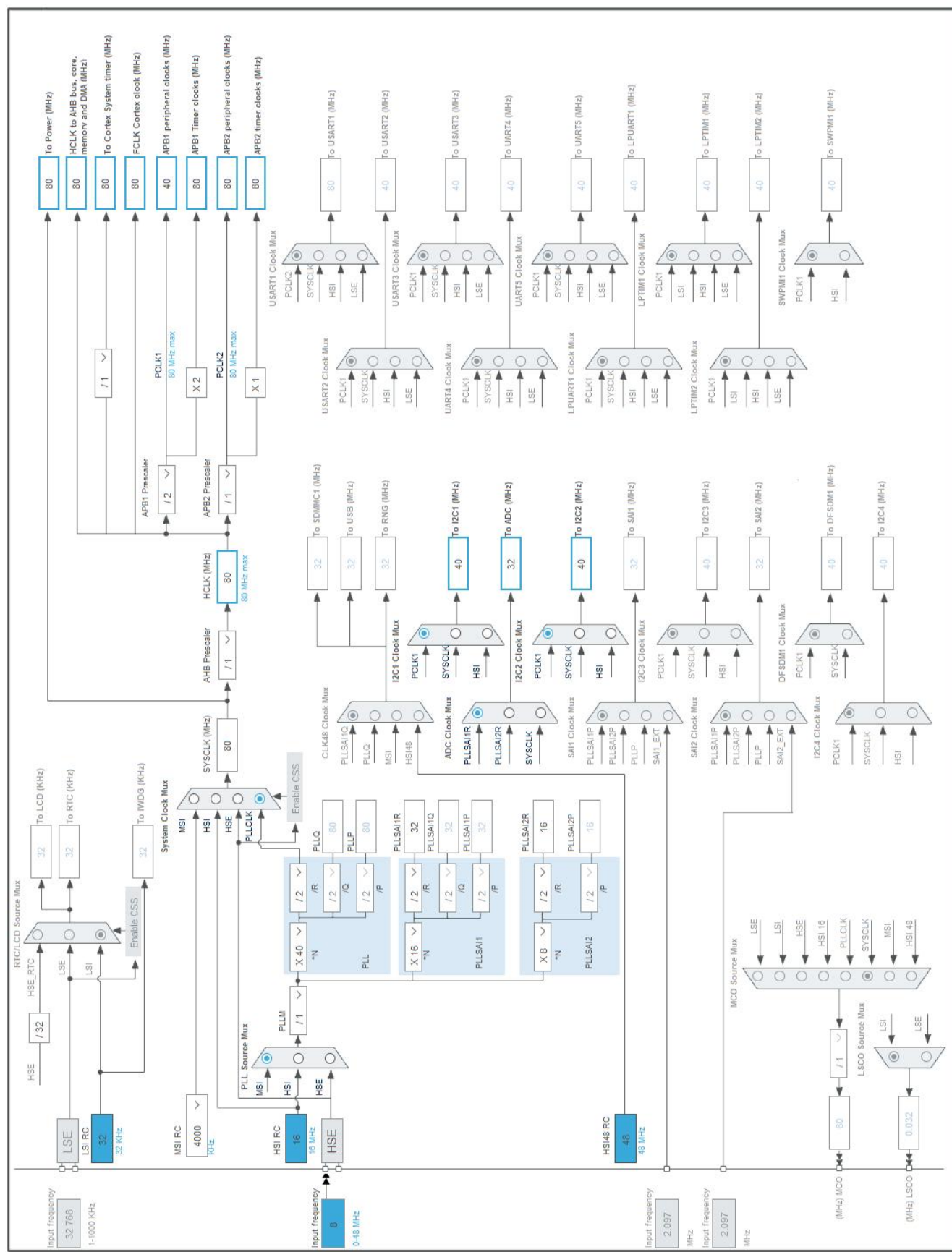
3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
10	PF0	I/O	I2C2_SDA	
11	PF1	I/O	I2C2_SCL	
16	VSS	Power		
17	VDD	Power		
23	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
25	NRST	Reset		
26	PC0	I/O	ADC1_IN1	
27	PC1	I/O	ADC1_IN2	
28	PC2	I/O	ADC1_IN3	
29	PC3	I/O	ADC1_IN4	
30	VSSA	Power		
31	VREF-	Power		
33	VDDA	Power		
34	PA0	I/O	ADC2_IN5	
38	VSS	Power		
39	VDD	Power		
41	PA5	I/O	SPI1_SCK	
42	PA6	I/O	SPI1_MISO	
43	PA7	I/O	SPI1_MOSI	
44	PC4 *	I/O	GPIO_Output	
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
70	VDD12	Power		
71	VSS	Power		
72	VDD	Power		
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDDIO2	Power		
105	PA13 (JTMS/SWDIO)	I/O	SYS_JTMS-SWDIO	
106	VDDUSB	Power		
107	VSS	Power		
108	VDD	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
109	PA14 (JTCK/SWCLK)	I/O	SYS_JTCK-SWCLK	
120	VSS	Power		
121	VDD	Power		
130	VSS	Power		
131	VDDIO2	Power		
138	PB8	I/O	I2C1_SCL	
139	PB9	I/O	I2C1_SDA	
142	VDD12	Power		
143	VSS	Power		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	VitalSense_Main
Project Folder	D:\EmbeddedSystems\Workspace_Polysomnography\VitalSense_Main
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L4 V1.18.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_I2C2_Init	I2C2
4	MX_I2C1_Init	I2C1
5	MX_SPI1_Init	SPI1
6	MX_FATFS_Init	FATFS
7	MX_ADC2_Init	ADC2
8	MX_ADC1_Init	ADC1

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L496ZGTxP
Datasheet	DS11585_Rev2

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

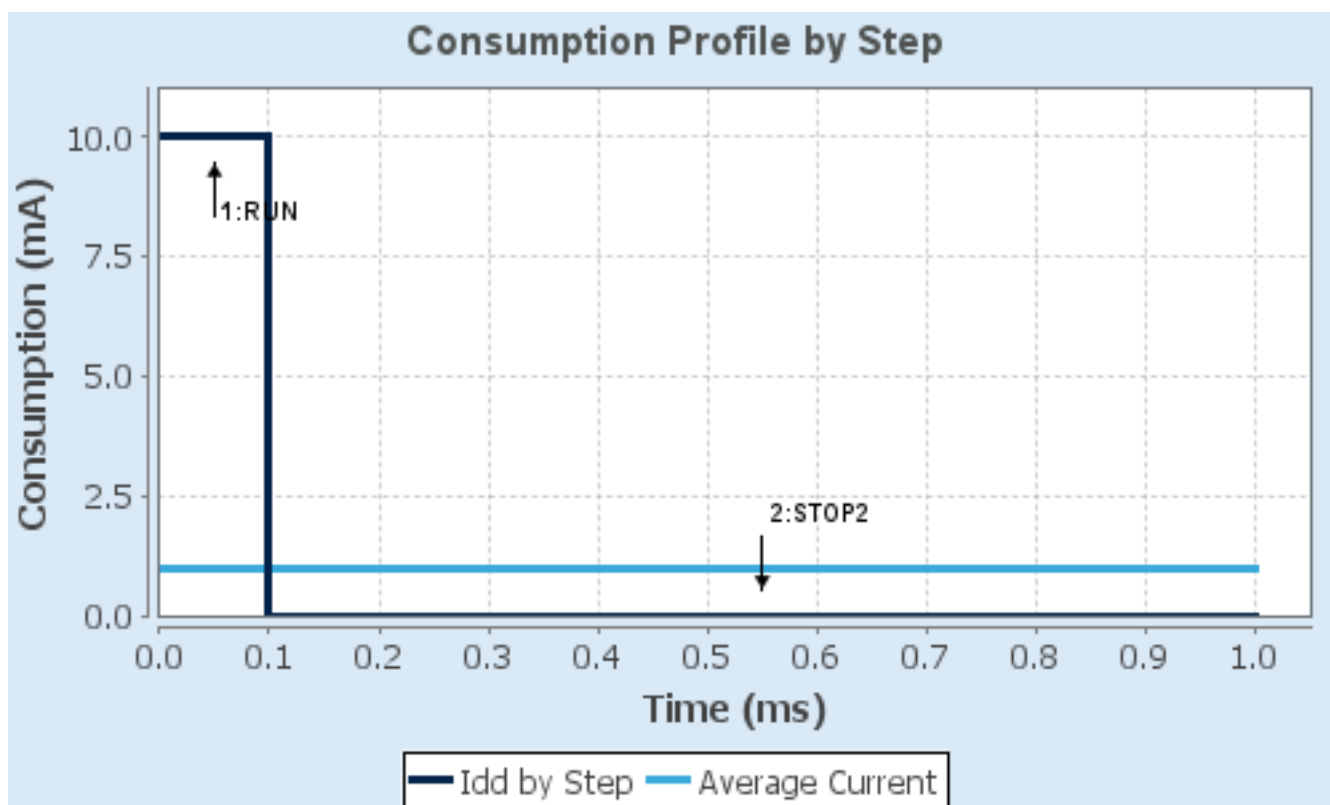
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	FLASH	n/a
CPU Frequency	80 MHz	0 Hz
Clock Configuration	HSE BYP PLL Flash-ON	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	10 mA	2.69 μ A
Duration	0.1 ms	0.9 ms
DMIPS	100.0	0.0
Ta Max	104.04	105
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	1 mA
Battery Life	4 months, 19 days, 3 hours	Average DMIPS	100.0 DMIPS

1.6. Chart



2. Peripherals and Middlewares Configuration

2.1. ADC1

IN1: IN1 Single-ended

IN2: IN2 Single-ended

IN3: IN3 Single-ended

IN4: IN4 Single-ended

2.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Scan Conversion Mode Enabled

Continuous Conversion Mode **Enabled ***

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Low Power Auto Wait Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable

Enable Regular Oversampling Disable

Number Of Conversion **4 ***

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel Channel 1

Sampling Time **12.5 Cycles ***

Offset Number No offset

Rank **2 ***

Channel Channel 1

Sampling Time **12.5 Cycles ***

Offset Number No offset

Rank **3 ***

Channel Channel 1

Sampling Time **12.5 Cycles ***

Offset Number No offset

Rank	4 *
Channel	Channel 1
Sampling Time	12.5 Cycles *
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable
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Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false
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Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false
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Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false
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2.2. ADC2

IN5: IN5 Single-ended

2.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode
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ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Enabled *
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 5
Sampling Time	12.5 Cycles *

Enable Injected Conversions Disable

Enable Analog WatchDog1 Mode	false
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Enable Analog WatchDog2 Mode	false
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Enable Analog WatchDog3 Mode	false
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2.3.1. Parameter Settings:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x00909BEB *

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

2.4.1. Parameter Settings:

Custom Timing	Disabled
I2C Speed Mode	Fast Mode *

I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x00301347 *

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

2.5. RCC

High Speed Clock (HSE): BYPASS Clock Source

2.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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2.6. SPI1

Mode: Full-Duplex Master

2.6.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits *
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	8 *
Baud Rate	10.0 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

2.7. SYS

Debug: Serial Wire

Timebase Source: SysTick

2.8. FATFS

mode: User-defined

2.8.1. Set Defines:

Version:

FATFS version	R0.12c
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Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	Enabled with static working buffer on the BSS *
MAX_LFN (Max Long Filename)	255

LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	4096 *
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
FS_REENTRANT (Re-Entrancy)	Disabled
FS_TIMEOUT (Timeout ticks)	1000
FS_LOCK (Number of files opened simultaneously)	2

* User modified value

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PC1	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PC2	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	
	PC3	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PA0	ADC2_IN5	Analog mode	No pull-up and no pull-down	n/a	
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
	PB9	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
I2C2	PF0	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
	PF1	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SYS	PA13 (JTMS/SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	
GPIO	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

3.2. DMA configuration

nothing configured in DMA service

3.3. NVIC configuration

3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 interrupts	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI1 global interrupt	unused		
FPU global interrupt	unused		

3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

* User modified value

4. System Views

4.1. Category view

4.1.1. Current

Middleware						
FATFS ✓						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA	ADC1 ✓		I2C1 ✓			
GPIO ✓	ADC2 ✓		I2C2 ✓			
NVIC ✓			SP1 ✓			
RCC ✓						
SYS ✓						

5. Docs & Resources

Type	Link
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