DIGITAL DESIGN

LAB1　USING VIVADO + FPGA DEVELOPMENT BOARD(MINISYS/EGO1)

2021 FALL TERM

TOPICS

- Experimental Platform

  EDA tool (Vivado 2017.4) + FPGA Development Board(Minisys/EGO1)

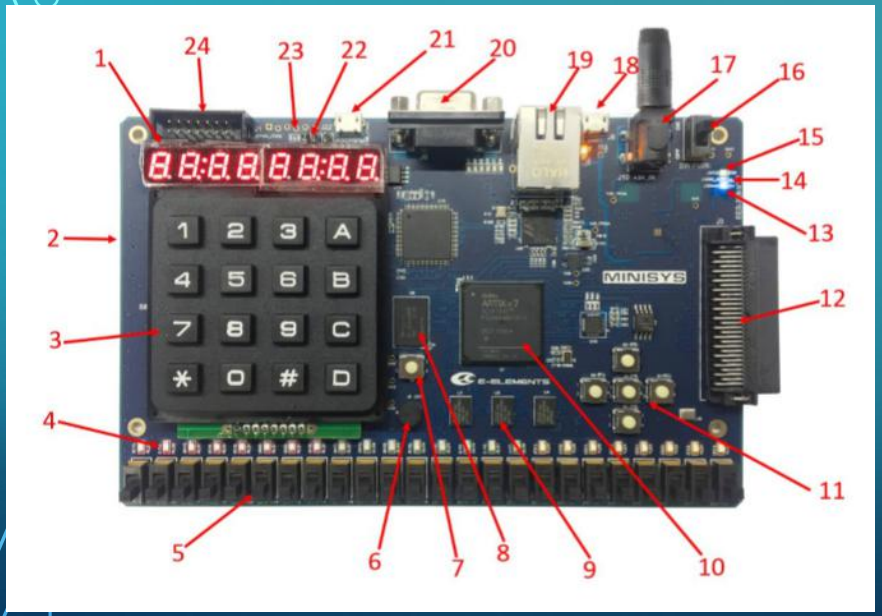
  - Vivado installation tips
  - FPGA Development Board(Minisys/EGO1) introduction
- 1st Lab on Digital Logic course
  - Build a vivado project, add circuit design file and constraint file
  - Connect vivado with FPGA Development Board and program the FPGA chip
  - Test the circuit which runs on the FPGA chip
- Questions and Exercises

EXPERIMENTAL PLATFORM: EDA + FPGA DEVELOPMENT BOARD

- Vivado 2017 (a type of EDA tools):
  - Vivado is a design environment for FPGA products from Xilinx, and is tightly-coupled to the architecture of such chips, and cannot be used with FPGA products from other vendors.
  - Vivado enables developers to synthesize (compile) their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.
  - The version we choose is vivado 2017.4

- Installation of vivado (20 G free hard disk space is suggested)
  - Attention: the name of the directory which includes installation package MUST NOT containing Chinese character

FPGA DEVELOPMENT BOARD

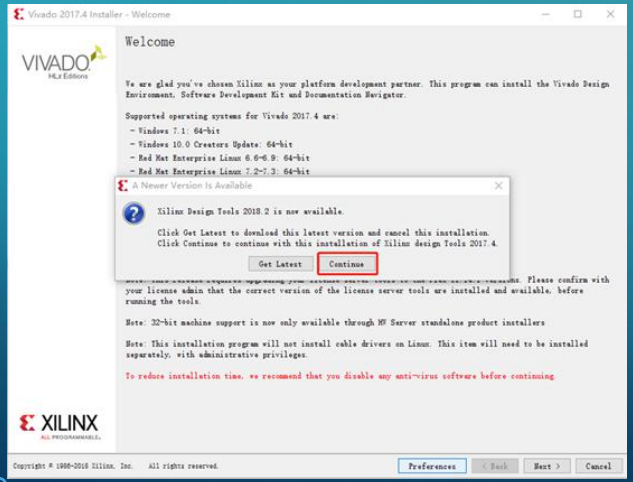


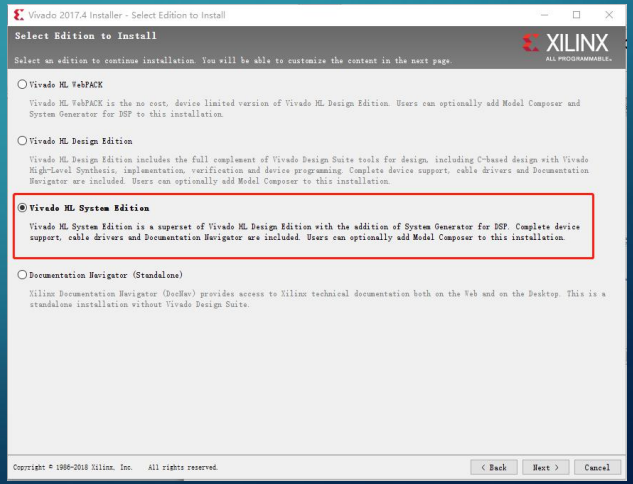
- Power Interface (17)
- USB-JTAG Interface (21)
- **Artix 7 FPGA chip** (10)
- SRAM (9)
- Minisys soc system inside
- **Seven-Segment Digital Tube** (1)
- **Mini Keyboard** (3)
- **Dial Switch** *24 (5)
- **LED** *24 (4)

VIVADO(2017.4) INSTALLATION (TIPS1)

ftp://10.20.118.226/ account: ftp-d-logic password: ggsddu

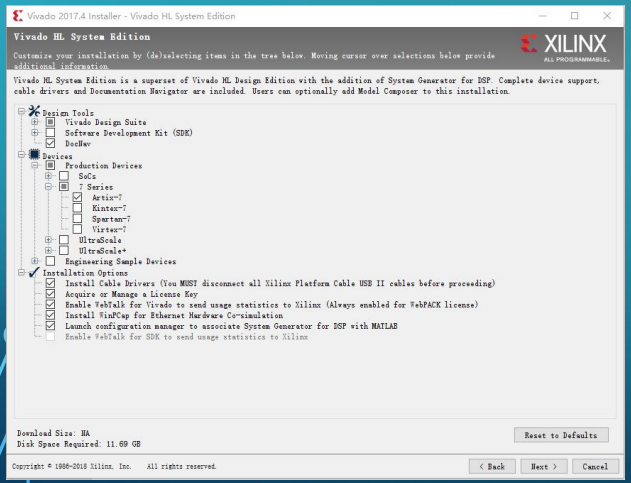
xsetup



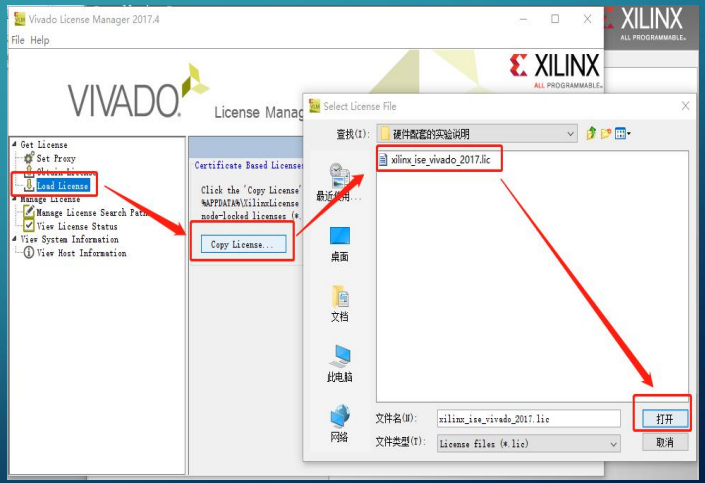


VIVADO INSTALLING (TIPS2)

Select ONLY WHAT IS NEEDED !!

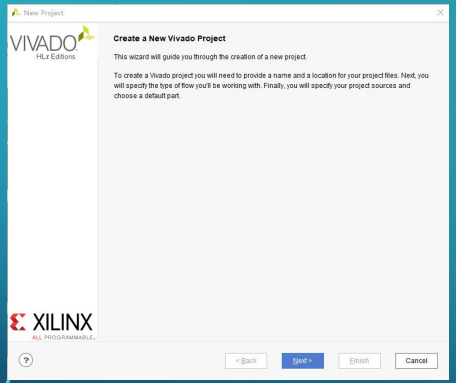


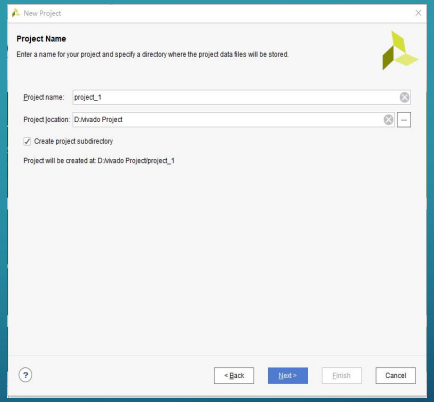
At the end of installing, load license

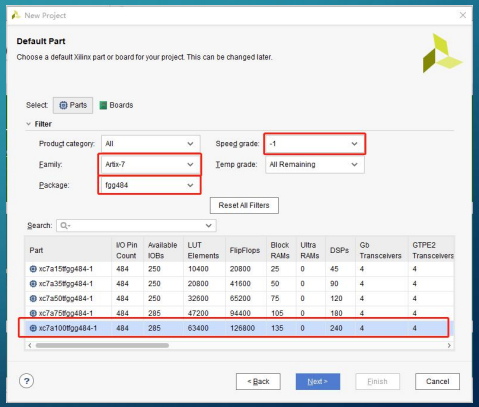


USING VIVADO + FPGA DEVELOPMENT BOARD(1)

1. Create project , select “rtl type” , select the corresponding FPGA chip name





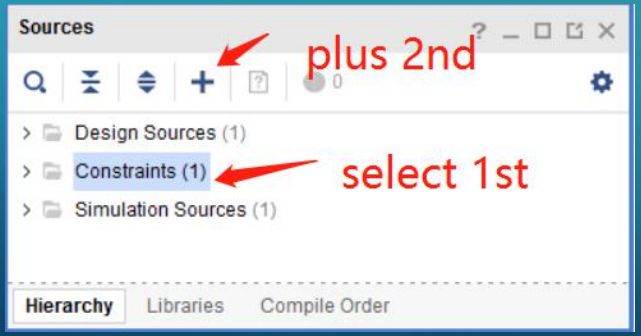


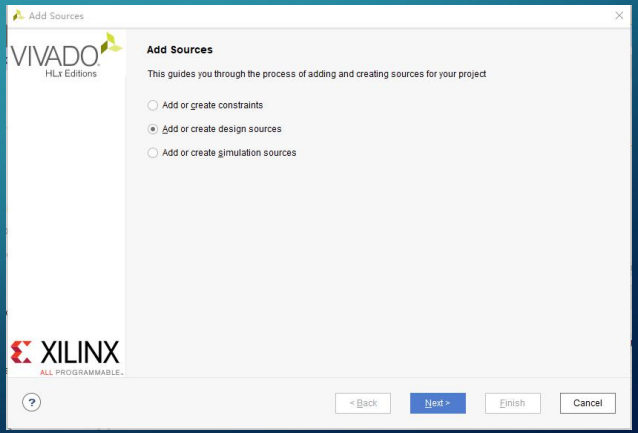
tips: FPGA Chip(Artix 7 xc7a100t fgg484-1) is embedded in Minisys board

FPGA Chip(Artix 7 xc7a35t CSG324-1) is embedded in EGO1 board

USING VIVADO + FPGA DEVELOPMENT BOARD(2)

2. Adding source file, simulation file and constraints file



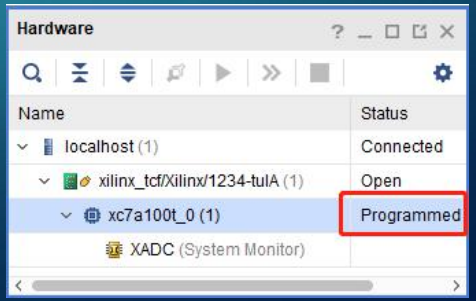


USING VIVADO + FPGA DEVELOPMENT BOARD(2)

- 3.following the steps to verify the function and generate bitstream file which is used to program FPGA chip
  - 1）Do the simulation to verify the function of the designed Circuit
  - 2）After simulation ,there will be a waveform which records the states of circuit's input and output signals
  - 3）if the function of circuit is ok , run synthesis ,then run implements
  - 4) after implementation is finished, Generate Bitstream , there will be a .bit file which will be used to program device

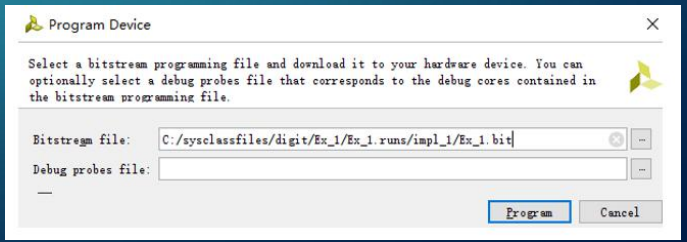
USING VIVADO + FPGA DEVELOPMENT BOARD(3)

- 4. connect Minisys/EGO1 board with PC
  - USB JTAG interface for Minisys(old version) board
  - USB typeC interface for Minisys(new version)/EGO1 board
- 5. turn on the Minisys/EGO1 board
- 6. using the “open Target ” to connect the vivado project with FPGA development board(Minisys/EGO1 board)



USING VIVADO + FPGA DEVELOPMENT BOARD(4)

- 7. right click “program device”, then choose the device name.
- 8. select the bitstream file, click “program” button.
- 9. while the the led of “Done” on Minisys is on, it means the bit file is written into the device.
- Do the testing on the FPGA development board(Minisys/EGO1).



A 8-INPUTS-8-OUTPUTS CIRCUIT ON EGO1

lab1_sw_led_8.v

```
module lab1_sw_led_8(
    input [7:0] sw,
    output [7:0] led
    );
    assign led=sw;
endmodule
```

lab1_sw_led_8_sim.v

```
`timescale 1ns / 1ps
module lab1_sw_led_8_sim( );
reg [7:0] sw=24'h000000;
wire [7:0] led;

lab1_sw_led_8 usrc1(
.sw(sw),
.led(led)
);

always #10 sw=sw+1;
endmodule
```

lab1_ego1.xdc

```
set_property IOSTANDARD LVCMOS33 [get_ports {led[7]}]
...
set_property IOSTANDARD LVCMOS33 [get_ports {led[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sw[7]}]
...
set_property IOSTANDARD LVCMOS33 [get_ports {sw[0]}]
set_property PACKAGE_PIN F6 [get_ports {led[7]}]
...
set_property PACKAGE_PIN K2 [get_ports {led[0]}]
set_property PACKAGE_PIN P5 [get_ports {sw[7]}]
...
set_property PACKAGE_PIN R1 [get_ports {sw[0]}]
```

Q: If “lab1_sw_led_8_sim.v” is removed from the vivado project, will the circuit work or not?

A 24-INPUTS-24-OUTPUTS CIRCUIT ON MINISYS


lab1_sw_led_24.v


lab1_sw_led_24_sim.v


lab1_minisys.xdc

tips:
while using Minisys(old version) board, connect its USB-Jtag interface to the computer which run vivado project by typeB USB wire.

whille using Minisys(new version) board/EGO1 board, connect its typeC interface to the computer which run vivado project by typeC USB wire.

Q: If a 12-inputs-12-outputs circuit is designed to work on Minisys board, which files need to be modified?