

A decorative graphic on the left side of the slide, consisting of a network of white lines and small circles on a dark blue background, resembling a circuit board or a digital network.

# DIGITAL DESIGN

LAB5 TRUTH-TABLE, SOP, POS, VERILOG(LOOP)

2021 FALL TERM @ CSE . SUSTECH

# LAB5

- *Standard form* vs *SOP*(sum of minterms) vs *POS*(product of maxterms)
- Verilog
  - loop: repeat, forever, for, while
  - system task: \$display, \$write, \$monitor
- Practise

# STANDARD FORM VS SOP VS POS

- $F(A,B,C)=A+B'C$
- $F(A,B,C)=AB(C'+C)+AB'(C'+C)+B'C(A'+A)=A'B'C+AB'C'+AB'C+ABC'+ABC$   
 $=m1+m4+m5+m6+m7=\sum(1,4,5,6,7)$
- $F(A,B,C)''=(F(A,B,C))'=(m0+m2+m3)'=M0.M2.M3 = \prod(0,2,3)$

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

```
module lab5(a, b, c, z1, z2, z3);  
  input a, b, c;  
  output z1, z2, z3;  
  
  assign z1 = a | ((~b) & c);  
  assign z2 = (a&b&c) | (a&b&(~c)) | (a&(~b)&c) | (a&(~b)&(~c)) | ((~a)&(~b)&c); //m7+m6+m5+m4+m1  
  assign z3 = (a | b | c) & (a | ~b | c) & (a | ~b | ~c); //M0. M2. M3  
endmodule
```

# TESTBENCH USING LOOP(1)

```
module lab5_tb();  
    reg sa, sb, sc;  
    wire sz1, sz2, sz3;  
    lab5 ulab5(.a(sa),.b(sb),.c(sc),.z1(sz1),.z3(sz3),.z2(sz2));  
  
    initial  
    begin  
        {sa, sb, sc} = 3'b000;  
        forever  
        #100 {sa, sb, sc} = {sa, sb, sc} + 1;  
    end  
endmodule
```



## Tips on Vivado:

- Select the name of the ports you want to see in group (ctrl + select)
- Right click then choose the “New virtual Bus” to group all the selected ports

# TESTBENCH USING LOOP(2)

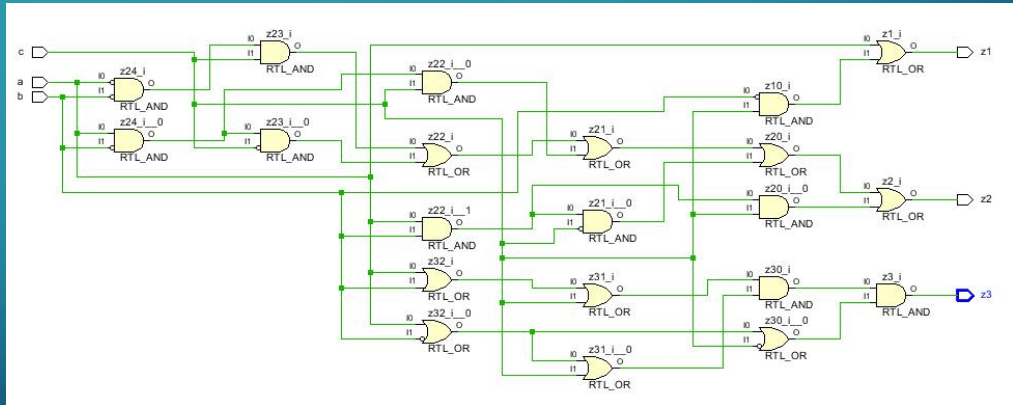
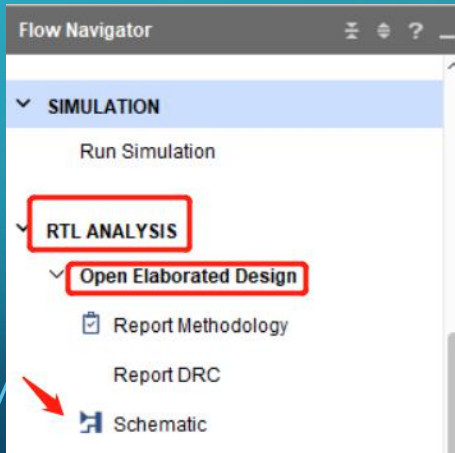
```
initial
begin
    {sa, sb, sc} = 3'b000;
    repeat(7)
    begin
        #100 {sa, sb, sc} = {sa, sb, sc} + 1;
        $display($time, " {sa, sb, sc}:%d", {sa, sb, sc});
    end
    #100 $finish(1);
end
```

```
initial
begin
    {sa, sb, sc} = 3'b000;
    for(integer i=0; i<7; i=i+1)
    begin
        #100 {sa, sb, sc} = {sa, sb, sc} + 1;
    end
    #100 $finish(1);
end
```

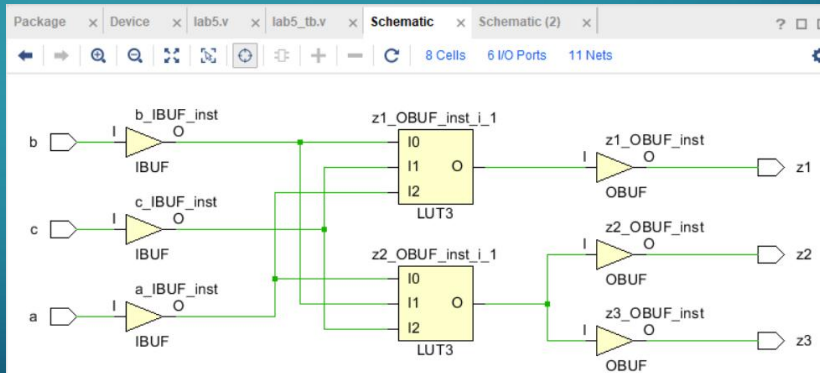
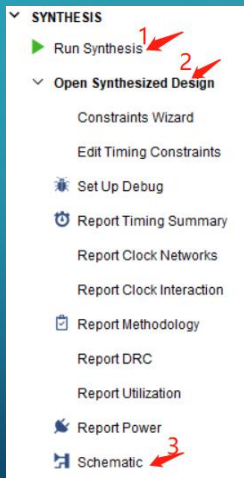
```
initial
begin
    {sa, sb, sc} = 3'b000;
    while({sa, sb, sc} < 3'b111)
    begin
        #100 {sa, sb, sc} = {sa, sb, sc} + 1;
    end
    #100 $finish(1);
end
```



# SCHEMATIC IN 'RTL ANALYSIS'

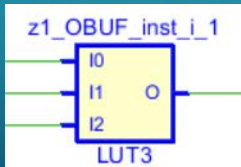


# SCHEMATIC IN 'SYNTHESIS'(1)



# SCHEMATIC IN 'SYNTHESIS'(2)

- Double click the LUT in schematic window
- In the 'Cell Properties' window , choose 'Truth Table', the truth table of the cell is shown



SYNTHESIZED DESIGN - xc7a100tfgg484-1 (active)

Sources Netlist Device Constraints

Internal VREF

0.6V

Drop I/O banks on voltages or the "NONE" folder to set/unset Internal VREF.

Cell Properties Clock Regions

z1\_OBUF\_inst\_i\_1

$O = I0 \& I1 + I2$

I2	I1	I0	O
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1

Edit LUT Equation...

General Properties Power Nets Cell Pins Truth Table



# USING 'DISPLAY', 'WRITE', 'MONITOR' TO DISPLAY THE VALUE

- \$display is a system task, not Synthesizable
- Please try \$write and \$monitor separately

```
initial
begin
    {sa, sb, sc} = 3'b000;
    repeat(7)
    begin
        #100 {sa, sb, sc} = {sa, sb, sc} + 1;
        $display($time, "{sa, sb, sc}:%d", {sa, sb, sc});
    end
    $finish(1);
end
```

```
# run 1000ns
100{sa, sb, sc}:1
200{sa, sb, sc}:2
300{sa, sb, sc}:3
400{sa, sb, sc}:4
500{sa, sb, sc}:5
600{sa, sb, sc}:6
700{sa, sb, sc}:7
$finish called at time : 700 ns :
```

# PRACTICES(1)

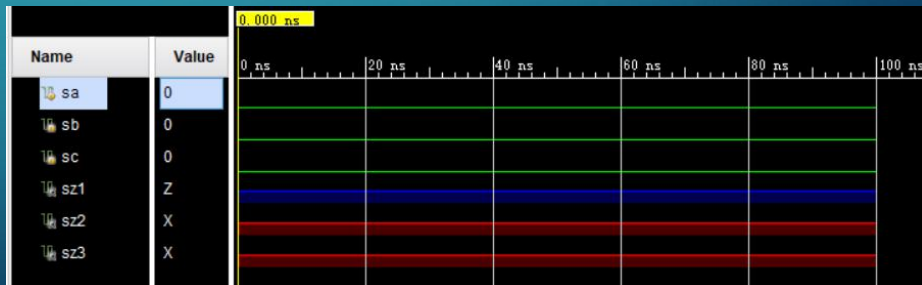
Do the simulation on lab5Tb which is the testbench of lab5, it is found that the waveform is not in line with expectations:

- 1) sa, sb and sc keep 0 in the simulation, why ?
- 2) sz1 is Z, while the state of sz2 and sz3 is X, why?

modify to make it workable and test the function of module lab5

```
1 `timescale 1ns / 1ps
2 //////////////////////////////////////
21 module lab5Tb ( );
22   reg sa,sb,sc;
23   wire sz1,sz2,sz3;
24   lab5 ulab5(sa,sb,sz1,sz2,sz3);
25   initial begin
26     {sa,sb,sc}=3'b000;
27     repeat(7);
28     begin
29       #100 {sa,sb,sc} = {sa,sb,sc}+1;
30       $display($time,"sa,sb,sc:%d",{sa,sb,sc});
31     end
32     $finish(100);
33   end
34 endmodule
```

绑定并绑定 sc  
空循环了, 应删去;



$$x \oplus (y \wedge z)' \mid x' \oplus (y \wedge z) \quad x(yz' + zy')' + x'(yz' + zy')$$

$$x(y' + z)(z' + y) + x'(yz' + zy')$$

## PRACTICES(2)

$$F = xy'z' + xyz + x'yz' + x'y'z$$

$$= \Sigma(1, 2, 4, 7) = \Pi(0, 3, 5, 6)$$

Implement the digital logic circuit and test its function:  $F(x,y,z) = x \wedge y \wedge z$

- Using data flow style in verilog to implement the circuit design in SOP and POS respectively
- Write the testbench in Verilog to verify the function of the design
- Check the Schematic of 'synthesis' and 'RTL analysis' respectively, find the differences between the two schematics
- Generate the bitstream and program the device to test the function

$$m_0 = a/b/c$$

$$M_0 = \pi(0, 3, 5, 6)$$

$$a + b + c \in (1, 2, 4, 7)$$

$$F = (x' + y' + z')(x' + y + z)(x + y' + z)(x + y + z')$$