Computer Organization and Design

Homework 1

1.6 Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2.
Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?
a. What is the global CPI for each implementation?
b. Find the clock cycles required in both cases.

Solution:

a. Count of all instructions is 1×10^6.
So for class A: count = $1 \times 10^6 \times 10\% = 1 \times 10^5\ instructions$
Class B: count = $1 \times 10^6 \times 20\% = 2 \times 10^5\ instructions$
Class C: count = $1 \times 10^6 \times 50\% = 5 \times 10^5\ instructions$
Class D: count = $1 \times 10^6 \times 20\% = 2 \times 10^5\ instructions$
Time = (Number of instructions × CPI)/clock rate
For P1:
Total time=$(1 \times 10^5 \times 1 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3)/(2.5\times 10^9)$
CPI(P1)=Total time × clock rate / count of all instruction
= 2.6
For P2:
Total time=$(1 \times 10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2)/(2.5\times 10^9)$
CPI(P2)= Total time × clock rate / count of all instruction
= 2

b. Clock cycles(P1)= $1 \times 10^5 \times 1 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3$
$= 26 \times 10^5$
Clock cycles(P2)= $1 \times 10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2$
$= 20 \times 10^5$

1.8 The Pentium 4 Prescott processor, released in 2004, had a clock rate of 3.6 GHz and voltage of 1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power.
The Core i5 Ivy Bridge, released in 2012, had a clock rate of 3.4 GHz and voltage of 0.9 V. Assume that, on average, it consumed 30 W of static power and 40 W of dynamic power.
1.8.1 For each processor find the average capacitive loads.
1.8.2 Find the percentage of the total dissipated power comprised by static power and the ratio of static power to dynamic power for each technology.
1.8.3 If the total dissipated power is to be reduced by 10%, how much should the

voltage be reduced to maintain the same leakage current? Note: power is defined as the product of voltage and current.

Solution:

1.8.1

$\text{Dynamic Power} = 1/2 \times \text{Capacitive load} \times Voltage^2 \times frequency\ switched$

So the average capacitive loads

= 2*Dynamic Power /($Voltage^2 \times frequency\ switched$)

Pentium 4: C=2*90/($1.25^2 \times 3.6 \times 10^9$)=$3.2 \times 10^{-8}$F

Core i5 Ivy Bridge: C=2*40/($0.9^2 \times 3.4 \times 10^9$)= 2.9×10^{-8}F

or:

$\text{Dynamic Power} = \text{Capacitive load} \times Voltage^2 \times frequency\ switched$

So the average capacitive loads

= Dynamic Power /($Voltage^2 \times frequency\ switched$)

Pentium 4: C=90/($1.25^2 \times 3.6 \times 10^9$)=$1.6 \times 10^{-8}$F

Core i5 Ivy Bridge: C=40/($0.9^2 \times 3.4 \times 10^9$)= 1.5×10^{-8}F

1.8.2

Pentium 4:

the percentage of the total dissipated power comprised by static power

=10/100=10%

the ratio of static power to dynamic power

=10/90=11.11%

Core i5 Ivy Bridge:

the percentage of the total dissipated power comprised by static power

=30/70=42.86%

the ratio of static power to dynamic power

=30/40=75%

1.8.3

$(S_{new} + D_{new})/(S_{old} + D_{old})$=0.9

$D_{new} = C \times V_{new}{}^2 \times F$

$S_{old} = V_{old} \times I$

$S_{new} = V_{new} \times I$

Therefore:

$V_{new} = [D_{new}/(C \times F)]^{1/2}$

$D_{new} = 0.9 \times (S_{old} + D_{old}) - S_{new}$

$S_{new} = V_{new} \times (S_{old}/V_{old})$

Pentium 4:

$S_{new} = V_{new} \times (10/1.25) = 8V_{new}$

$D_{new} = 0.9 \times 100 - 8V_{new} = 90 - 8V_{new}$

$V_{new} = [(90 - 8V_{new})/(3.2(or\ 1.6) \times 10^{-8} \times 3.6 \times 10^9)]^{1/2}$
$V_{new} = 0.85\ V$ or 1.18V

Core i5 Ivy Bridge:
$S_{new} = V_{new} \times (30/0.9) = 33.3V_{new}$
$D_{new} = 0.9 \times 70 - 33.3V_{new} = 63 - 33.3V_{new}$
$V_{new} = [(63 - 33.3V_{new})/(2.9(or\ 1.5) \times 10^{-8} \times 3.4 \times 10^9)]^{1/2}$
$V_{new} = 0.65\ V$ or 0.83V

1.15 When a program is adapted to run on multiple processors in a multiprocessor system, the execution time on each processor is comprised of computing time and the overhead time required for locked critical sections and/or to send data from one processor to another.
Assume a program requires t = 100 s of execution time on one processor. When run p processors, each processor requires t/p s, as well as an additional 4 s of overhead, irrespective of the number of processors. Compute the per-processor execution time for 2, 4, 8, 16, 32, 64, and 128 processors. For each case, list the corresponding speedup relative to a single processor and the ratio between actual speedup versus ideal speedup (speedup if there was no overhead).

Solution:
p=1, execution time per processor = 100 s.
For p>1, execution time per processor =100/p s
while the total time = execution time per processor + overhead = 100/p +4 s
Therefore, when p=2, 4, 8, 16, 32, 64, and 128

processors	Exec.time/ processor	Time w/overhead	Speedup	Actual speedup/ ideal speedup
1	100			
2	50	54	100/54=1.85	1.85/2=0.93
4	25	29	100/29=3.45	3.45/4=0.86
8	12.5	16.5	100/16.5=6.06	6.06/8=0.76
16	6.25	10.25	100/10.25=9.76	9.76/16=0.61
32	3.125	7.125	100/7.125=14.03	14.03/32=0.44
64	1.5625	5.5625	100/5.5625=17.98	17.98/64=0.41
128	0.78125	4.78125	100/4.78125=20.91	20.91/128=0.16