Computer Organization and Design

Homework 6

5.3 For a direct-mapped cache design with a 32-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31–10	9–5	4–0

5.3.1 What is the cache block size (in words)?
5.3.2 How many entries does the cache have?
5.3.3 What is the ratio between total bits required for such a cache implementation over the data storage bits?
Starting from power on, the following byte-addressed cache references are recorded.

Address											
0	4	16	132	232	160	1024	30	140	3100	180	2180

5.3.4 How many blocks are replaced?
5.3.5 What is the hit ratio?
5.3.6 List the final state of the cache, with each valid entry represented as a record of <index, tag, data>.

Solution:
5.3.1 Since offset field is 5 bits, then block size is 32 bytes(8 words)
5.3.2 Number of entries $= 2^n = 2^5 = 32$
5.3.3 Size of cache: $2^n * (block\ size + tag\ size + valid\ field\ size)$

$$\text{The ratio} = \frac{\text{Size of } cache}{Size\ of\ block} = \frac{2^n(2^m*32+(32-n-m-2)+1)}{2^n*2^m*32} = \frac{32*(8*32+22+1)}{32*8*32} = 1.0898$$

5.3.4 Index = number of block in cache
= ⌊block address/block size⌋ mod (number of entries)

Address	0	4	16	132	232	160	1024	30	140	3100	180	2180
Index	0	0	0	4	7	5	0	0	4	0	5	4
Tag	0	0	0	0	0	0	1	0	0	3	0	2
Hit/Miss	Miss	Hit	Hit	Miss	Miss	Miss	Miss	Miss	Hit	Miss	Hit	Miss
Replace	N	N	N	N	N	N	Y	Y	N	Y	N	Y

2 blocks are replaced.
5.3.5 Hit ratio = 4/12 =0.33
5.3.6

<index	tag	data>
$<00000_2$	00000000000000000011_2	Mem[3072]>
$<00100_2$	00000000000000000010_2	Mem[2176]>
$<00101_2$	00000000000000000000_2	Mem[160]>
$<00111_2$	00000000000000000000_2	Mem[224]>