Computer Organization and Design

Homework 7

5.6 In this exercise, we will look at the different ways capacity affects overall performance. In general, cache access time is proportional to capacity. Assume that main memory accesses take 70 ns and that memory accesses are 36% of all instructions. The following table shows data for L1 caches attached to each of two processors, P1 and P2.

	L1 Size	L1 Miss Rate	L1 Hit Time
P1	2 KiB	8.0%	0.66 ns
P2	4 KiB	6.0%	0.90 ns

5.6.1 Assuming that the L1 hit time determines the cycle times for P1 and P2, what are their respective clock rates?
5.6.2 What is the Average Memory Access Time for P1 and P2?
5.6.3 Assuming a base CPI of 1.0 without any memory stalls, what is the total CPI for P1 and P2? Which processor is faster?

For the next three problems, we will consider the addition of an L2 cache to P1 to presumably make up for its limited L1 cache capacity. Use the L1 cache capacities and hit times from the previous table when solving these problems. The L2 miss rate indicated is its local miss rate.

L2 Size	L2 Miss Rate	L2 Hit Time
1 MiB	95%	5.62 ns

5.6.4 What is the AMAT for P1 with the addition of an L2 cache? Is the AMAT better or worse with the L2 cache?
5.6.5 Assuming a base CPI of 1.0 without any memory stalls, what is the total CPI for P1 with the addition of an L2 cache?
5.6.6 Which processor is faster, now that P1 has an L2 cache? If P1 is faster, what miss rate would P2 need in its L1 cache to match P1's performance? If P2 is faster, what miss rate would P1 need in its L1 cache to match P2's performance?

Solution:

5.6.1 For P1: $\text{clock rate} = \frac{1}{\text{cycle times}} = \frac{1}{0.66\times10^{-9}s} = 1.52\ GHz$

For P2: $\text{clock rate} = \frac{1}{\text{cycle times}} = \frac{1}{0.90\times10^{-9}s} = 1.11\ GHz$

5.6.2

P1: $\text{AMAT} = 0.66 + 8\% \times 70 = 6.26\ \text{ns}$

P2: $\text{AMAT} = 0.90 + 6\% \times 70 = 5.10\ \text{ns}$

5.6.3

$$\text{Miss penalty of P1} = \frac{70}{0.66} = 107\ cycles$$

$$\text{Miss penalty of P2} = \frac{70}{0.90} = 78\ cycles$$

$$CPI_{stall} = CPI_{ideal} + average\ memory\ stall\ cycles$$

For P1: $CPI_{P1} = 1 + 36\% \times 0.08 \times 107 = 4.08\ clock\ cycles = 2.69$ ns

For P2: $CPI_{P2} = 1 + 36\% \times 0.06 \times 78 = 2.68\ clock\ cycles = 2.42$ ns

$$2.42\ ns < 2.69\ \text{ns}$$

So P2 is faster.

5.6.4

$$\begin{aligned}\text{AMAT} &= \text{L1 hit time} + \text{miss rate of L1} \times (\text{L2 hit time} \\ &\quad + \text{miss rate of L2} \times \text{miss penalty}) \\ &= 0.66 + 0.08 \times (5.62 + 0.95 \times 70) \\ &= 6.43\ \text{ns}\end{aligned}$$

The AMAT is worse.

5.6.5

$$\frac{5.62}{0.66} = 8.5 \rightarrow 9\ cycles$$

$$\text{new Total CPI} = 1 + 0.36 \times 0.08 \times (9 + 0.95 \times 107) = 4.19\ \text{clock cycles}$$

5.6.6

$$\text{P1 AMAT} = 6.43\ \text{ns}$$

$$\text{P2 AMAT} = 5.10\ \text{ns}$$

P2 is faster.

For P1 to match P2's performance:

$$5.10 = 0.66 + \text{MR} \times (5.62 + 0.95 \times 70)$$

So $\text{MR} = 6.1\%$

5.9 This Exercise examines the single error correcting, double error detecting (SEC/DED) Hamming code.

5.9.1 What is the minimum number of parity bits required to protect a 128-bit word using the SEC/DED code?

5.9.2 Section 5.5 states that modern server memory modules (DIMMs) employ SEC/DED ECC to protect each 64 bits with 8 parity bits. Compute the cost/performance ratio of this code to the code from 5.9.1. In this case, cost is the relative number of parity bits needed while performance is the relative number of errors that can be corrected. Which is better?

5.9.3 Consider a SEC code that protects 8 bit words with 4 parity bits. If we read the value 0x375, is there an error? If so, correct the error.

Solution: 5.9.1 Assume that number of parity bit = p, and number of data bits = d.
So there are $p + d$ bit word.

$$2^p \geq p + d + 1$$

and we get $p \geq 8$, and then add 1. So the minimum number of parity bits required to protect a 128-bit word using the SEC/DED code is 9.

5.9.2 For (72,64) code, $\text{cost} = \frac{8}{64} = 12.5\%$, $\text{performance} = \frac{1}{72} = 1.4\%$

$$\frac{12.5}{1.4} = 8.9$$

For (128,137) code, $\text{cost} = \frac{9}{128} = 7.0\%$, $\text{performance} = \frac{1}{137} = 0.73\%$

$$\frac{7.0}{0.73} = 9.6$$

The (72,64) code has a better cost/performance ratio.

5.9.3 $0x\ 375 = 0011\ 0111\ 0101$

Bit position		1	2	3	4	5	6	7	8	9	10	11	12
Encoded date bits		p1	p2	d1	p4	d2	d3	d4	p8	d5	d6	d7	d8
Parity bit coverate	p1	X		X		X		X		X		X	
	p2		X	X			X	X			X	X	
	p4				X	X	X	X					X
	p8								X	X	X	X	X

Position 1 checks bits 1, 3, 5, 7 ,9, 11
Position 2 checks bits 2, 3, 6, 7 ,10, 11
Position 4 checks bits 4, 5, 6, 7 ,12
Position 8 checks bits 8, 9, 10, 11, 12

Parity bits 1 = XOR(0,1,0,1,0,0) = 0
Parity bits 2 = XOR(0,1,1,1,1,0) = 0
Parity bits 4 = XOR(1,0,1,1,1) = 0
Parity bits 8 = XOR(1,0,1,0,1) = 1

C = 1000, it is a single error in bit 8. Corrected value =0011 0110 0101 = 0x365