Homework 4

June 4, 2022

1 Problem 1

1. Since the offset is 5-bit, with 2-bit byte offset, the cache block size is $2^5/4 = 8$ word.

2. Since the index is 5-bit, the cache has $2^5 = 32$ entries.

3.

Address	0	4	16	132	232	160	1024	30	140	3100	180	2180
Index	0	0	0	4	7	5	0	0	4	0	5	4
Tag	0	0	0	0	0	0	1	0	0	3	0	2
Hit/Miss	Miss	Hit	Hit	Miss	Miss	Miss	Miss	Miss	Hit	Miss	Hit	Miss
Replace	N	N	N	N	N	N	Y	Y	N	Y	N	Y

4.

$$hit\ ratio = \frac{hit}{hit + miss} \times 100\% = \frac{4}{12} \times 100\% = 33.3\%$$

5.

Index	Tag	Data
0	3	$Men[3072_{10}]$
4	2	Mem[2176 ₁₀]
5	0	$Mem[160_{10}]$
7	0	Mem[224 ₁₀]

2 Problem 2

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Address	17	32	2	2059	4124	65	2067	2200	30	0	4102	360
Index	1	2	0	0	1	4	1	9	1	0	0	22
Tag0	0	0	0	0	0	0	1	1	1	0	0	0
Tag1				1	2		2		0	1	2	
Hit/Miss	Miss	Hit	Miss	Miss								
Replace	N	N	N	N	N	N	Υ	N	Υ	N	Υ	N

• The cache size is $2^7 \times (2^2 \times 32 + (32 - 7 - 4) + 1) = 19200$ bit = 600 word.

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Index	Tag	Data	Tag	Data
0	0	$Men[0_{10}]$	2	$Men[4096_{10}]$
1	1	$Mem[2064_{10}]$	0	$Men[16_{10}]$
2	0	$Mem[32_{10}]$		
4	0	$Mem[64_{10}]$		
9	1	$Mem[2192_{10}]$		
22	0	$Mem[352_{10}]$		

3 Problem 3

- 1. Since $4KiB = 2^{12}$ byte, the needed number of PTEs is $2^{43} \div 2^{12} = 2^{31}$.
- 2. The needed physical memory is $2^{31} \times 4$ byte = 2^{33} byte.

4 Problem 4

1. To protect a 128-bit word, it must be

$$2^{p} \ge p + d + 1$$

$$\implies p \ge \log_{2}(p + d + 1)$$

where p is the number of parity bits, d is the number of digital bits. Here d = 128. To solve this inequality, we can get the minimum number of parity bits is 8.

2. We have $0x5C6 = (0101_1100_0110)_2$ with 12 bits. Then we can encode the SEC.

Bit position	1	2	3	4	5	6	7	8	9	10	11	12	
Bits	0	1	0	1	1	1	0	0	0	1	1	0	
Encoded date bits	<i>p</i> 1	<i>p</i> 2	d1	<i>p</i> 4	d2	d3	d4	<i>p</i> 8	d5	d6	d7	d8	
<i>p</i> 1	х		х		x		х		x		х		0
<i>p</i> 2		х	х			х	х			х	х		0
<i>p</i> 4				x	x	x	x					x	1
<i>p</i> 8								x	x	x	x	x	0

Since $\{p8, p4, p2, p1\} = 0100$, the bit position of 4. The correct value is $(0100_1100_0110)_2$, i.e., 0x4C6.