



Index

Index 1

2024_R2.3 Release Notes..... 2

2024_R2.2 Release Notes..... 5

2024_R2.1 Release Notes..... 8

2024_R2.0 Release Notes..... 12



2024_R2.3 Release Notes

Introduction	2
General Enhancements	2
Thermal Integrity Flow	2
Signal/Power Integrity Flow	3
Issues Resolved	4
Thermal Integrity Flow	4
Setup3DIC	4
Signal/Power Integrity Flow	4

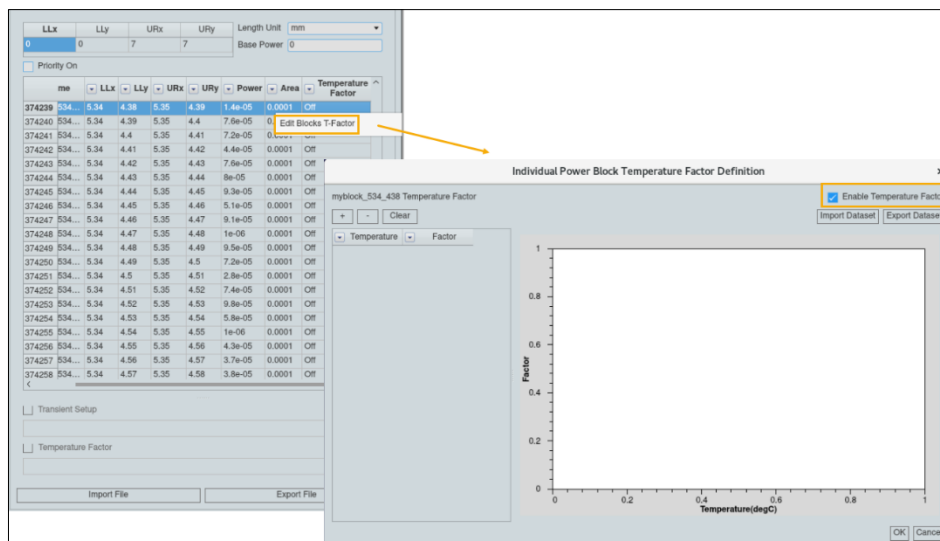
Introduction

Software version 2024_R2.3 continues improvements to the general functionality, speed, and usability of RedHawk-SC Electrothermal (ET).

General Enhancements

Thermal Integrity Flow

- Improved the GUI of the CTM data sheet to reduce the import time of multi heat source (mhs) files consisting of large number of sources. Now, to edit the temperature factor for a block as **On** or **Off**, right-click under the **Temperature Factor** column and select the **Edit Blocks T-Factor** option. This opens the **Individual Power Block Temperature Factor Definition** window to enable or disable the temperature factor as shown below:



Signal/Power Integrity Flow

- Enhanced the tool to support the GDS conversion for 3nm technology node. Now, you can select the 3nm as the technology type under **Tools > GDS Conversion > Options > GDS Advance Option** window.

GDS Advance Option

TOP GDS extraction option: full

Generate PLOC pins in DEF file: Use TEXT label

Set the region in top design for extraction

Lowest Left Postion
X: (um) Y: (um)

Upper Right Postion
X: (um) Y: (um)

☐ Uniquify target cells
☒ Merge Internal Nets
☒ Specify text labels for LEF pin creation
*:

☒ Set pin creation layer:

☐ Include TSV

Append config file:

Append GSR file:

MISC Control

Technology Type: 3nm

☒ Disable MINLVS
☐ Merge Circular Vias
☐ Compress the generated DEF file
☐ Select multi-threading method to speed up extraction
☐ Replace name with IO Mapping File

OK Cancel

Issues Resolved

Thermal Integrity Flow

- Fixed an issue where the tool calculated the wrong power value when scaling is defined to the CTM.
- Fixed an issue where the TCL command does not export the region map and section view in 3D Postprocessing.
- Fixed an issue where the tool displayed the wrong power dissipation data in the native transient simulation.

Setup3DIC

- Fixed an issue where the wrapper script did not distinguish two CPM files with the same sub-circuit name.

Signal/Power Integrity Flow

- Fixed an issue where the cell LEF file was not added automatically in the 3Dblox PI automation flow.



2024_R2.2 Release Notes

Introduction	5
General Enhancements	5
Thermal Integrity Flow	5
Setup3DIC	6
Signal/Power Integrity Flow	6
Issues Resolved	7
Thermal Integrity Flow	7
Setup3DIC	7
Chip Package Analysis (CPA) Flow	7
Signal/Power Integrity Flow	7

Introduction

Software version 2024_R2.2 continues improvements to the general functionality, speed, and usability of **RedHawk-SC Electrothermal (ET)**.

General Enhancements

Thermal Integrity Flow

- Enhanced the tool to support waveguide syntax in the general thermal technology file. The waveguide syntax is:

```
<Waveguide>
  <Material>Si_Sub</Material>
  <Dielectric>Diell_25c</Dielectric>
  <Thickness>0.22</Thickness>
  <Height>2</Height>
  <Trench_depth>0.13,0.06</Trench_depth>
</Waveguide>
```

where,

<material>/<Dielectric> specify the material name.

<Thickness>: specify the waveguide thickness

<Height>: specify the height of the die bottom to the waveguide bottom

<Trench_depth>: specify the waveguide trench depth, there are three types, deep, median, and shallow.

Setup3DIC

- Enhanced the tool with a new `.msg` log file under the project directory. This log file contains all the messages of the Message Window.
- The tool now shows the warning message if the bmap file only has 4 columns and lacks net information.

Signal/Power Integrity Flow

- Removed the `redhawk_sc_electrothermal_beta_a` license for the RedHawk-SC based interposer PI flow.
- Improved the Power Integrity 3Dblox automation flow with the following enhancements:

- You can now directly use the model for PDN extraction in the flow if a DEF or LEF file is present. To use the model, define the model in the configuration file in the following format:

```
chiplet:
```

```
model_type: DEFLEF
```

```
top_def:
```

```
tech_lef:
```

- You can now set the target cell in the flow. To set the target cell, define the cell in the configuration file in the following format:

```
chiplet:
```

```
gds_target_cell: [cell_name]
```

```
model_type: GDS
```

- You can now automatically import the TxV sub-circuit and eDTC models in the flow. To import the models, define the models in the configuration file in the following format:

```
txv:
```

```
txv_model: <model file>
```

```
txv_layer_name: <layer name>
```

```
edtc:
```

```
edtc_model: <model_file>
```

```
edtc_model_name: <subckt name>
```

```
Corner: <>
```

```
edtc_cell_name: <lef cell name>
```

```
edtc_model_type: capacitance
```

Issues Resolved

Thermal Integrity Flow

- Fixed an issue where the detail run failed after the AMC flow process.
- Fixed an issue where the tool terminated unexpectedly during GDS2XFL conversion.
- Fixed an issue where the tool displayed incorrect side HTC value in the NEU when the side HTC was enabled in the Fixed HTC dialog box.
- Fixed an issue where the thermal simulation terminated unexpectedly due to a duplicate layer name.
- Fixed an issue where the value in the **Minimum Angle (deg)** field of the General Mesh dialog box was not saved.
- Fixed the issue of detail run failure that occurred when the cut layer name was not found in the global run.
- Fixed an issue where the tool does not display the transient simulation result when the **Dz(mm)** was set to 0 value.
- Fixed an issue where the tool did not load the Icepak HTC file when the transient flow was set.
- Fixed an issue where the *.fld file generated from the external Icepak flow jumps to the internal Icepak flow.
- Fixed an issue where the tool calculated incorrect power position.

Setup3DIC

- Fixed an issue where the 6th column of the configuration or ploc file was not updated when the copper pillar model was set between the physical die and CPM model.

Chip Package Analysis (CPA) Flow

- Fixed an issue where the report menu does not work as expected in Simulation Setup GUI.
- Fixed an issue where the tool displayed a `Fatal <SCH.114>` error on the package ExtractView stage, resulting in a huge database import with capacitance components.

Signal/Power Integrity Flow

- Fixed an issue where interposer PDN extraction used only 16 workers. Now, the tool invokes the number of workers defined by the user.
- Fixed an issue where the tool terminated unexpectedly when the On-die grid model and physical die were deleted.
- Fixed an issue where the frequency sweep setting does not work as expected in AC simulation.



2024_R2.1 Release Notes

Introduction	8
General Enhancements	8
Thermal Integrity Flow	8
Signal/Power Integrity Flow	8
Issues Resolved	11
Thermal Integrity Flow	11
Setup3DIC	11
Signal/Power Integrity Flow	11

Introduction

Software version 2024_R2.1 continues improvements to the general functionality, speed, and usability of **RedHawk-SC Electrothermal (ET)**.

General Enhancements

Thermal Integrity Flow

- You can now export the thermal gradient file report for **interposer** using the following Tcl command:

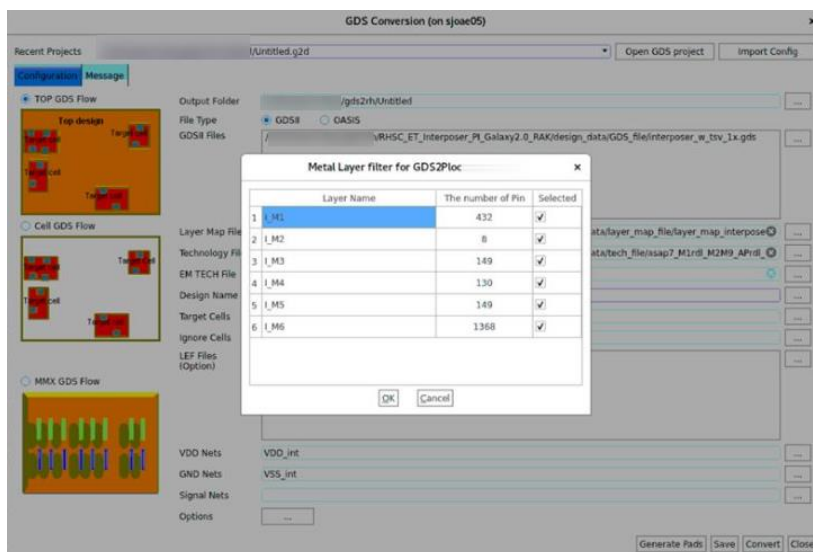
```
> analysis simulation export -name <model_name> -die <die_name> -static  
-device -distance {<distance_list>} -thermalprofile -outputfolder  
<path>
```

Example

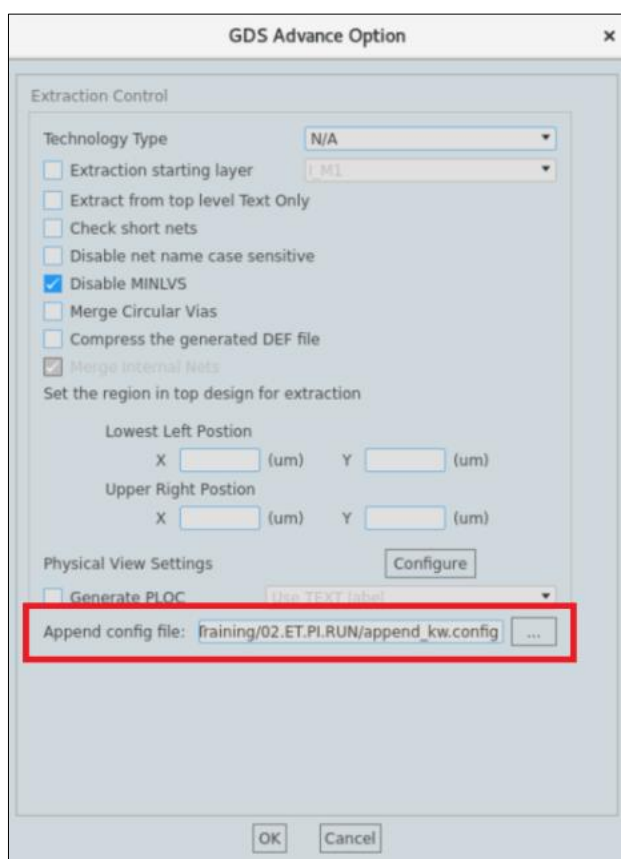
```
> analysis simulation export -name Case1 -die Interposer_1 -static -  
device -distance { 11, 16, 21 } -thermalprofile -outputfolder  
/testcase/3Dblox/11
```

Signal/Power Integrity Flow

- You can now select the metal layers to create the plocs during the pads generation using the **Metal Layer filter for GDS2Ploc** filter dialog box. The filter dialog box appears by clicking the **Generate Pads** button during the GDS to ploc conversion and displays metal layers (having text labels) and the number of pins.



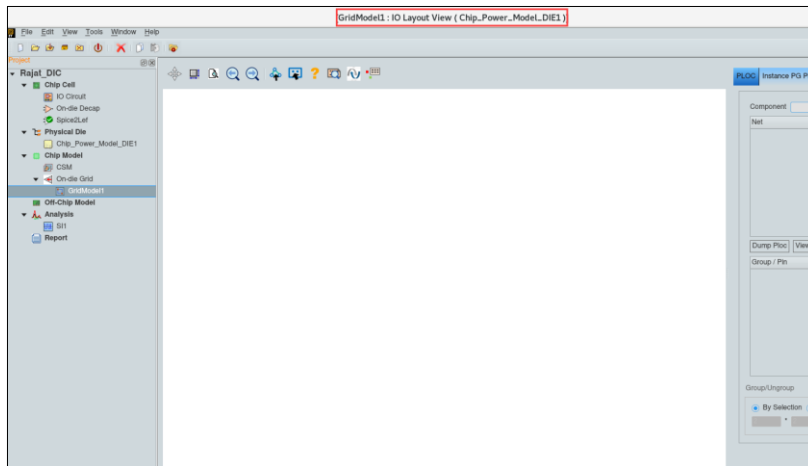
- Enhanced the tool to add advanced keywords in the GDS configuration file for GDS conversion. To add keywords, include the keywords in a file and import the file in the tool using the **GDS Advance Option > Append config file** option.



You can also use the following Tcl command to add the keywords and append the configuration file:

```
> diegdstransl advopt set -append_conf {append_file}
```

- Enhanced the tool to display the physical die name in the title of the On-die Grid model window. This helps you to verify the physical die that was used to generate the On-die Grid model.



Issues Resolved

Thermal Integrity Flow

- Fixed an issue where the simulation does not abort even after clicking the Abort button for Electro-Thermal flow.
- Fixed an issue where the internal Icepak flow in boundary condition did not work and displayed an error message.
- Fixed an issue where the molding was flipped on flipping the die object in the 3Dblox.
- Fixed an issue where the tool displayed an incorrect maximum value when using the section view.
- Fixed an issue where the tool terminated unexpectedly during the detail run simulation when the physical die size exceeded the power size.

Setup3DIC

- Fixed an issue where the tool terminated unexpectedly while performing net and footprint connections with quality mode.
- Fixed an issue where the spice model was listed as a die in the 3DIC configuration file in the 3DIC setup flow.

Signal/Power Integrity Flow

- Fixed an issue where when saving Translate GDS as a project, the output folder points to an incorrect area.



2024_R2.0 Release Notes

Modified June 21, 2024

Introduction	12
General Enhancements	12
Thermal Integrity Flow	12
Setup3DIC	28
Chip Package Analysis (CPA) Flow	29
Signal/Power Integrity Flow	30
Issues Resolved	32
Thermal Integrity Flow	32

Introduction

Software version 2024_R2.0 continues improvements to the general functionality, speed, and usability of **RedHawk-SC Electrothermal (ET)**.

General Enhancements

Thermal Integrity Flow

Modified June 21, 2024

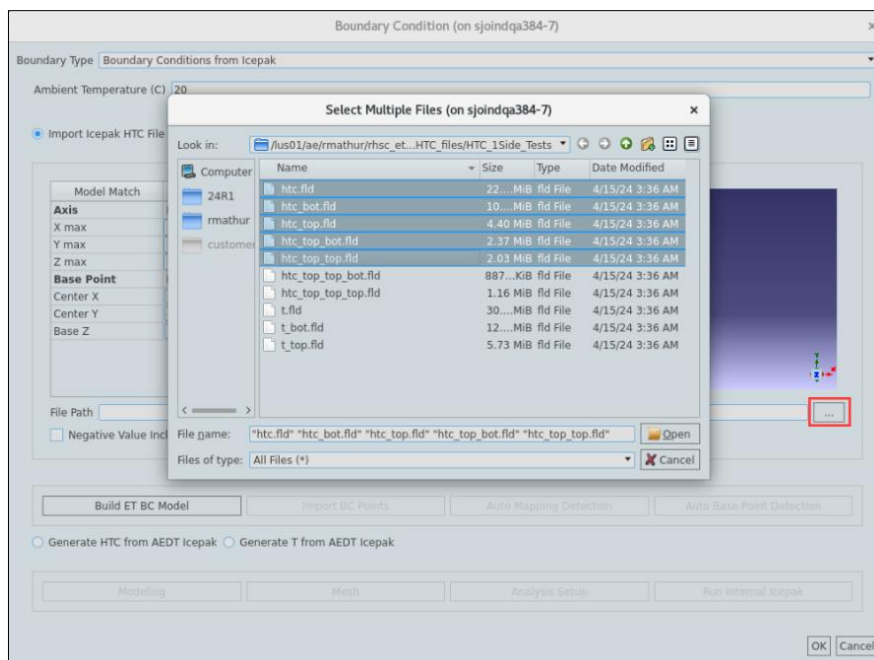
- **Recording all Overlapped Power Block Messages in Log File**

Enhanced the tool to record all messages in the log file related to power block overlap.

- **Importing Multiple HTC Files**

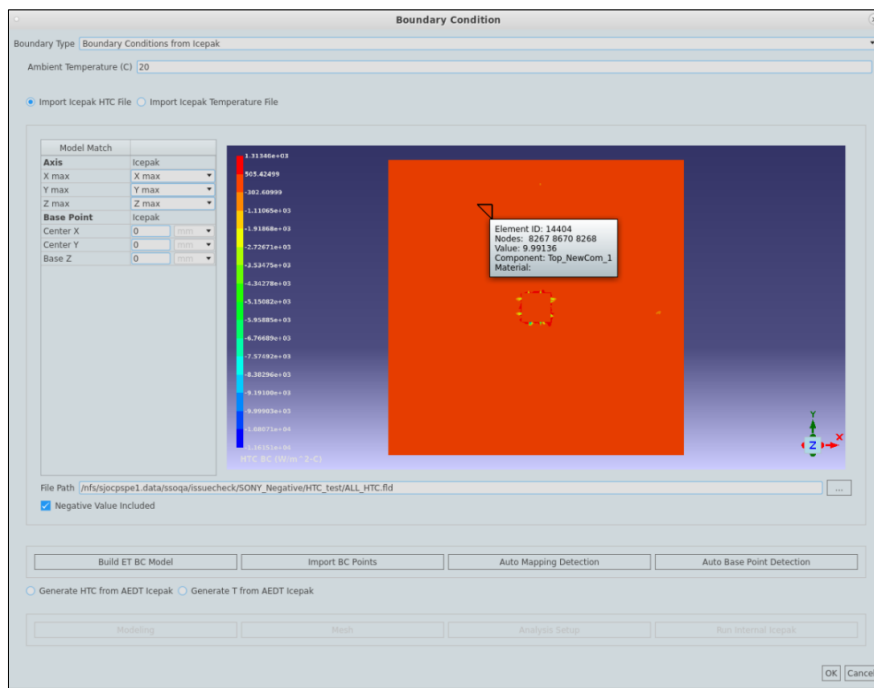
Enhanced the tool to import multiple external heat transfer coefficient (HTC) files (in .fld format) from Icepak, Mechanical, and Workbench. This helps cover multiple surfaces of a 3DIC for accurate boundary condition modeling.

You can get the .fld files from the system-level simulation and input them to the tool thermal model to run the simulation.



- **Supporting Negative HTC Values from Icepak**

The tool now supports the boundary condition with negative HTC values present in the imported .fld files from Icepak. To include the negative HTC values in the boundary condition, select the **Negative Value Included** checkbox while importing the HTC files from Icepak.



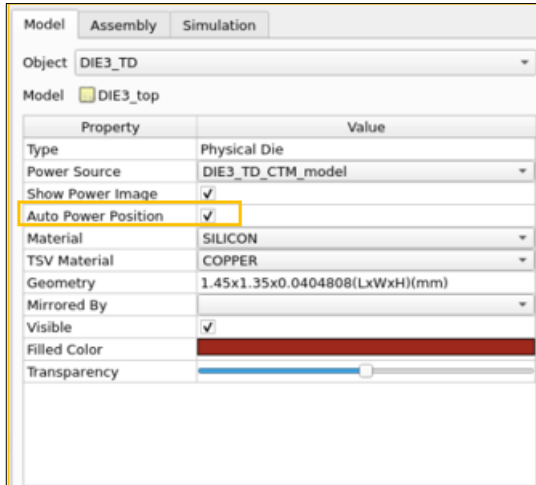
- **Enhancement in Power Position Calculation**

You can now calculate the power position in the tool using the following ways:

- Automatic
- Manual

Automatic Power Position Calculation

To automatically calculate the power position, enable the **Auto Power Position** checkbox under the **Model** tab.



When a CTM model has a substrate layer and a thermal technology file is available, the Auto Power Position checkbox is enabled by default to calculate the power position automatically. The power position information is saved in the project log file after the thermal simulation.

```
Thermal_TOP: Handling for BOT
Thermal_TOP: Update power position to 0.279416 for BOT
Thermal_TOP: Handling for DIE1
Thermal_TOP: Update power position to 0.606985 for DIE1
Thermal_TOP: Handling for DIE2
Thermal_TOP: Update power position to 0.606985 for DIE2
Thermal_TOP: Handling for DIE3
Thermal_TOP: Update power position to 0.606985 for DIE3
```

If the CTM model does not include a substrate layer, but the Auto Power Position check box is selected, the thermal simulation terminates with the following error message:

```
ERROR: Power position can not be auto calculated. No substrate but
total power is not 0. Please set the power position manually
```

Tcl Command

```
> analysis object setproperty -name <model name> -object <object name>
-autopowerposition <value>
```

where,

The <value> can be 1 (enable) or 0 (disable).

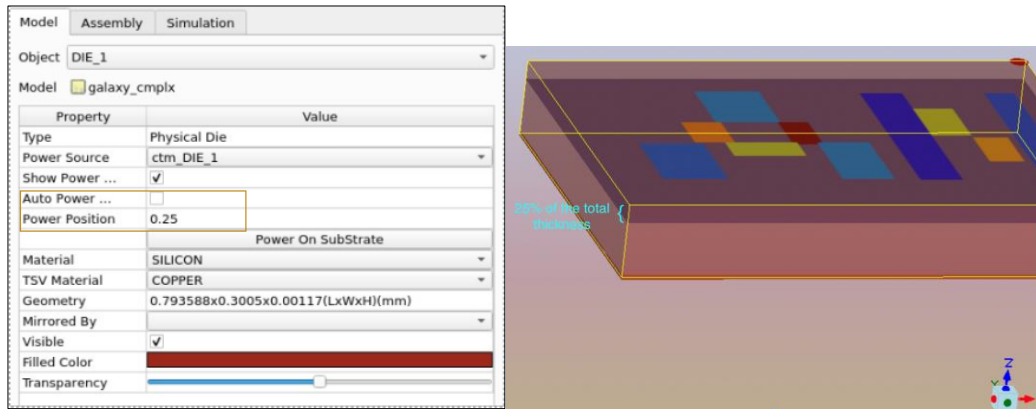
Example

To disable the automatic power position calculation, use the following Tcl command:

```
> analysis object setproperty -name TI -object DIE1 -autopowerposition
0
```

Manual Power Position Setup

To manually assign the power position, disable the **Auto Power Position** checkbox and define the fraction (between 1 to 0) of power position from the top surface to the total thickness of the 3D layer stack as the **Power Position** property.



The project log outputs the power position information after the thermal simulation.

```
Thermal_top_power: Handling for interposer
Thermal_top_power: Using power position from setup: 0.0114739
Thermal_top_power: Handling for DIE_1
Thermal_top_power: No substrate layer in CTM ctm_DIE_1 used by DIE_1
Thermal_top_power: Using power position from setup: 0.25
Thermal_top_power: Handling for DIE_2
Thermal_top_power: No substrate layer in CTM ctm_DIE_1 used by DIE_2
Thermal_top_power: Using power position from setup: 0.25
```

Tcl Command

```
> analysis object setproperty -name <model_name> -object <object_name>
-powerposition <value>
```

Example

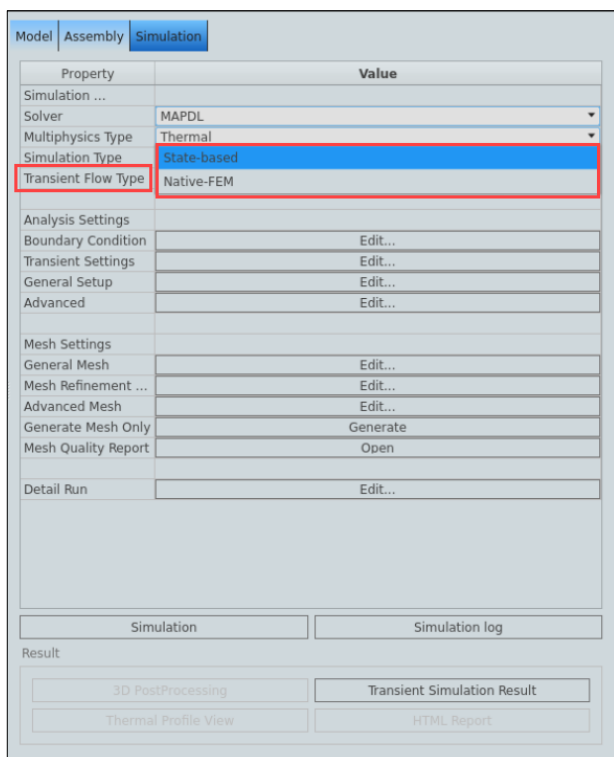
```
> analysis object setproperty -name TI -object DIE1 -powerposition
0.242
```

• Transient Thermal Simulation Enhancement

You can now perform transient thermal simulation based on one of the following transient flow types:

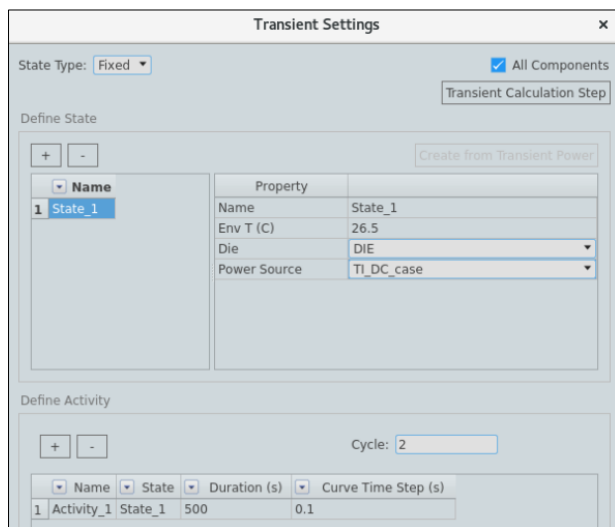
- State-based
- Native-FEM

To select the transient flow type, use the **Transient Flow Type** option under the **Simulation** tab in GUI. By default, the State-based transient flow type is selected.



State-based Transient Flow

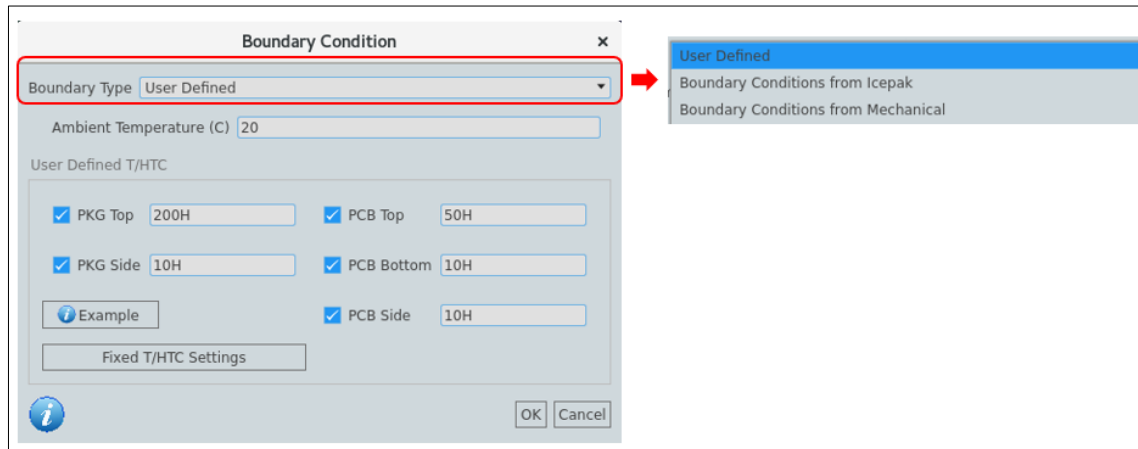
For State-based transient flow type simulation, the **Transient Settings** window in the GUI remains the same as in previous releases, when the Transient simulation type is selected.



Native-FEM Transient Flow

For the Native-FEM transient flow type simulation, three types of **Boundary Conditions** are supported:

- **User Defined**
- **Boundary Conditions from Icepak**
- **Boundary Conditions from Mechanical**



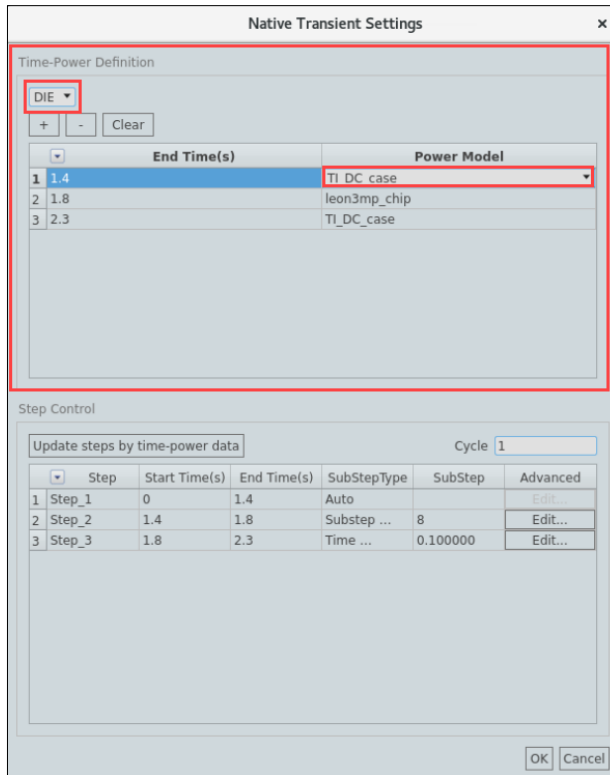
In the **Native Transient Settings** window, each die has its time-power table. You can define the time and power in these tables. The power sources can be selected from the existing power sources (constant power, MHS, or CTM) or can be kept as NULL.

Tcl Command

```
> analysis simulation control -name <analysis_name> -nativetransient -
timepower -add -die <die_name> -timepoints {} -powerlist {}
```

Example

```
> analysis simulation control -name T1Native -nativetransient -
timepower -add -die DIE -timepoints {1.4, 1.8, 2.3} -powerlist
{T1_DC_case, leon3mp_chip, T1_DC_case}
```



The **Native Transient Settings** window also includes a **Step Control** table. For each step, you can select the **SubStepType** column as Auto (default), SubStep Number, or Time Increment(s).

For SubStep Number or Time Increment(s) SubStepType, you must define the values in the **SubStep** column. The **Advanced** column is optional to define the maximum or minimum substeps.

Tcl Command

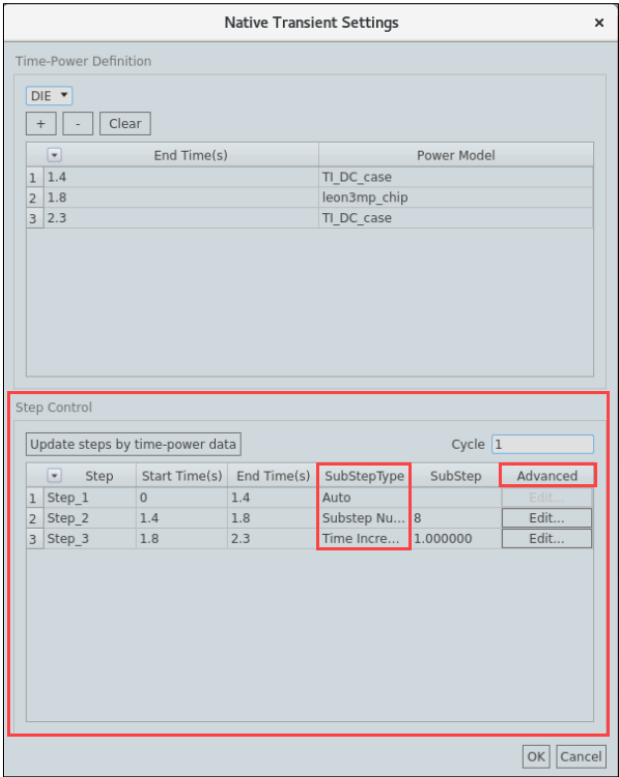
```
> analysis simulation control -name <analysis_name> -nativetransient -
stepcontrol -add -step <step_name> -tstart <value> -tend <value> -type
<1 or 2> -substepnum <value> -haslimit <value>
```

Example

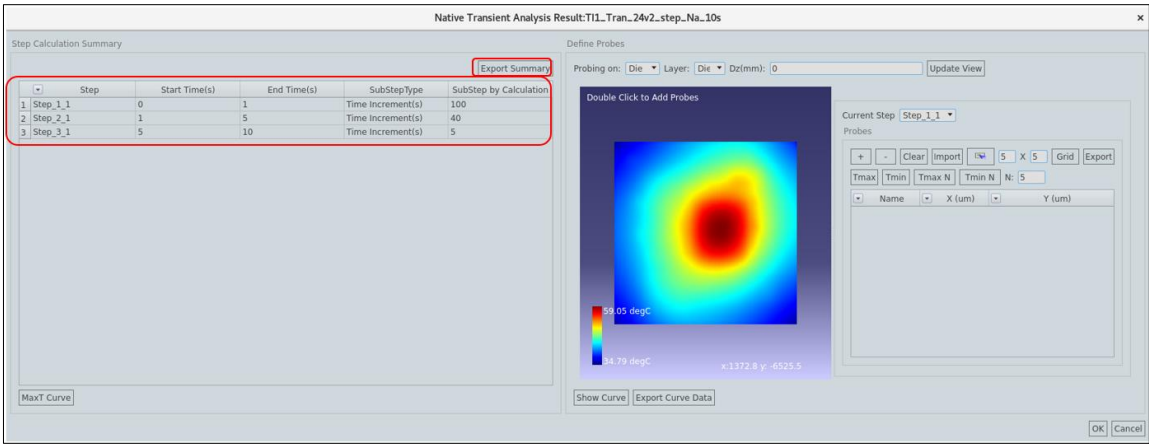
```
> analysis simulation control -name TlNative -nativetransient -
stepcontrol -add -step Step_1 -tstart 0 -tend 1.4

> analysis simulation control -name TlNative -nativetransient -
stepcontrol -add -step Step_2 -tstart 1.4 -tend 1.8 -type 1 -substepnum
8

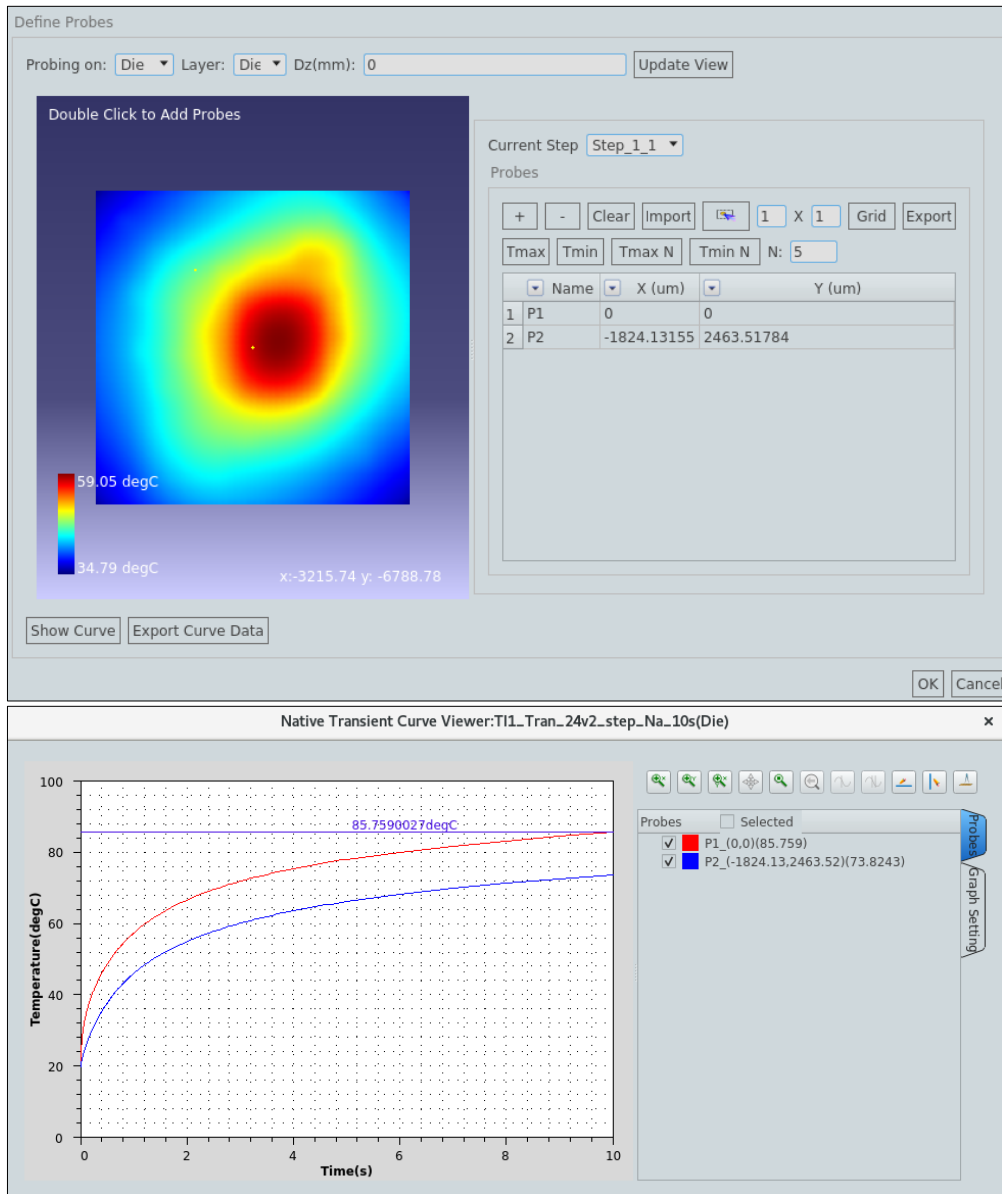
> analysis simulation control -name TlNative -nativetransient -
stepcontrol -add -step Step_3 -tstart 1.8 -tend 2.3 -type 2 -haslimit 1
```



After the simulation run, the **Transient Simulation Result** window displays the Step Calculation Summary table for reference. You can export this summary table using the **Export Summary** option.

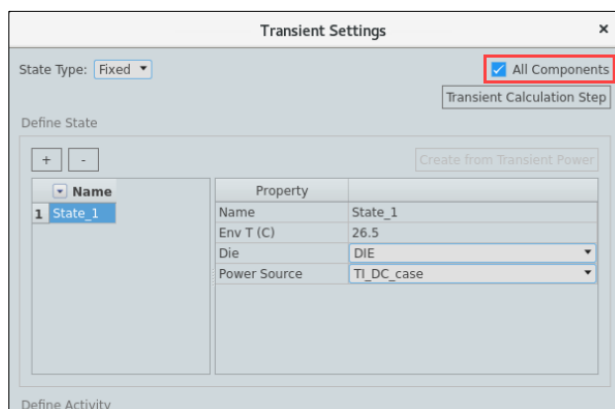


You can define the probe and show the curve. You can also export the curve data if needed.



- **Enabling All Components Checks for Transient Thermal Simulation**

The **All Components** checkbox of the **Transient Settings** window is now checked by default for State-based transient thermal simulation to analyze all components of the model.



- **Tcl Command to Add or Edit Bondwire and Bondwire Profile**

Enhanced the tool to add or edit the bondwire and bondwire profile using Tcl commands.

- To add the bondwire, use the following Tcl command:

Syntax

```
> layout setup bondwire -add -name <bondwire_name> -net <net_name> -
start <starting location> -end <ending location> -flip <true | false> -
profilename <profile_name> -model <model_name>
```

Example

```
> layout setup bondwire -add BW11 -net VDD -start METTOP -end VSS_C1 -
flip true -profilename BWProfile1 -model fccp
```

- To add the bondwire profile, use the following Tcl command:

Syntax

```
> layout setup bwprofile -add -name <bondwireprofile_name> -type
<profiletype> -segment {Angle , Length} -model <model_name>
```

Example

```
> layout setup bwprofile -add -name BWProfile11 -type NSegment -
segment {Angle, 90, Length, 0.178, Length, 0.1, Length, 0.02, Angle,
30, Length, 0.1} -model fccp
```

- **MAPDL Detection Enhancement**

Enhanced the tool to capture the error message in the MAPDL log (stderr.log file) when there is a MAPDL running issue to be debugged.

- **Enhanced Thermal Profile Result**

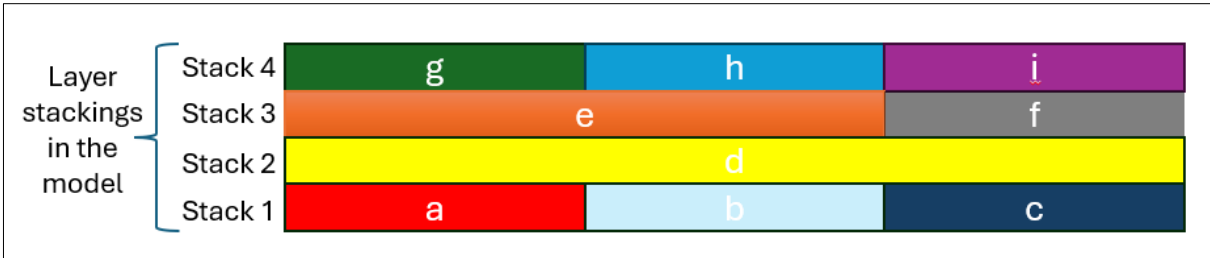
Added the following GSR keywords to report the thermal profile layers' result for CTM modeling:

Keyword	Condition
ThermalProfileVersion 1	Default setting. The behavior is the same as before, that is, the setting outputs non-zero thickness layers defined in the "LAYER" section of the CTM header.

ThermalProfileVersion 2	<ol style="list-style-type: none">1. Output layers following the layer stackings in the model. One dumped layer for one layer stack, except condition 2.2. Output all layers with material definition in the thermal technology file (TF).3. If a stacking layer has no layer defined in thermal TF, the tool finds one layer, defined in the LAYER section of the CTM header.
-------------------------	--

The following example shows how the use of `ThermalProfileVersion 1` and `ThermalProfileVersion 2` GSR keywords outputs different layers in thermal profile results.

Consider the following layer-stacking structure in the CTM model:



The CTM header consists of the **a, b, c, e, g, h, i** layers and the thermal technology file consists of the material for the **a, g, h** layers.

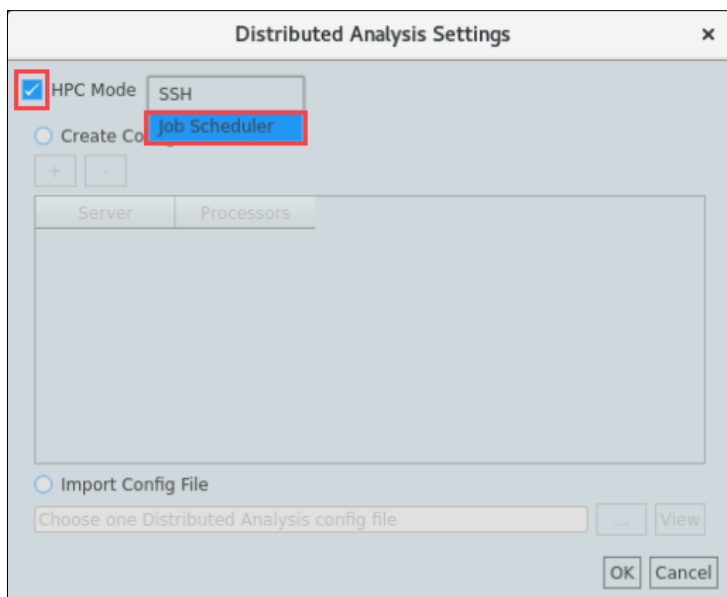
On using the `ThermalProfileVersion 1` GSR keyword, the thermal profile result outputs the **a, b, c, e, g, h, i** layers.

On using the `ThermalProfileVersion 2` GSR keyword, the thermal profile result outputs **a, e, g, h** layers.

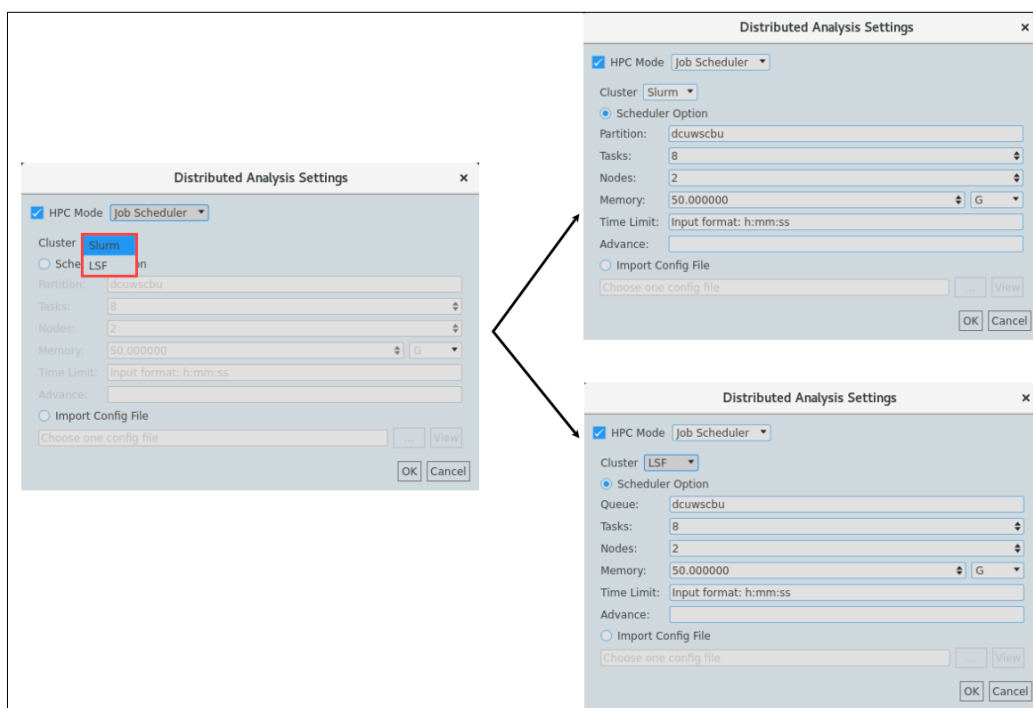
- **Slurm and LSF Support in HPC Mode**

Enhanced the tool to support Slurm and Load Sharing Facility (LSF) in high-performance computing (HPC) mode.

To use Slurm or LSF in HPC mode, check the **HPC Mode** checkbox and select the **Job Scheduler** option in the Distributed Analysis Settings window.



Choose the **Cluster** as Slurm or LSF and select the **Scheduler Option**.



Slurm Specific Settings

On the Scheduler option, you can specify the following:

- Partition – specify the partition name in the Slurm system.
- Tasks – specify the core number per node.
- Nodes – specifies the number of nodes that the job runs for, it indicates the number of machines.
- Memory – the amount of physical memory (specified in integer GigaBytes) allowed on a node to be eligible for selection.

- **Time Limit** – specifies the job run time, and if exceeded, the job will be killed.

You can also specify the Slurm command to a configuration file and import it. The configuration file is as below.

```
NodeNum, 2
ProcessPerNode, 16
MemPerNode, 120G
TimeLimit, 2:00:00
NodeName, sjoall, 32
```

Tcl Command

```
> analysis simulation control -name <analysis model> -hpcsetting -
hpcenable 1 -hpcsupporttype <type value> -hpcmodetype 1 -
hpcschedulerconfigstatus 1 -hpcschedulercluster <partition name> -
hpcschedulertasks <value> -hpcschedulernodes <value> -
hpcschedulermemory <value>
```

here,

- hpcsupporttype: Specify the HPC mode, there are 5 types, 0|1|2|3|4.

0: smp mode

1: local server dmp mode

2: SSH dmp

3: Slurm

4: LSF

- hpcschedulercluster: Specify Slurm partition.

Example

```
> analysis simulation control -name TI1 -hpcsetting -hpcenable 1 -
hpcsupporttype 3 -hpcmodetype 1 -hpcschedulerconfigstatus 1 -
hpcschedulertasks 16 -hpcschedulernodes 4 -hpcschedulermemory 100
```

LSF Specific Settings

On the Scheduler option, you can specify the following:

- **Queue** – specify partition name in the LSF system.
- **Tasks** – specify the number of processes, whether they are for exclusive use by the job or a limited number of processes per node.
- **Nodes** – specifies the number of nodes that the job runs for.
- **Memory** – the amount of physical memory (specified in integer GigaBytes) allowed on a node to be eligible for selection.
- **Time Limit** – specifies the job run time, and if exceeded, the job will be killed.

You can also specify the LSF command to a configuration file and import it. The configuration file is as below.

```
NodeNum, 3
ProcessPerNode, 24
MemPerNode, 100G
```

Tcl Command

```
> analysis simulation control -name <analysis model> -hpcsetting -
hpcenable 1 -hpcsupporttype <value> -hpcmodetype 1 -
```



```
hpcschedulerconfigstatus 1 -hpcschedulercluster <queue name> -
hpcschedulerntasks <value> -hpcschedulerntodes <value> -
hpcschedulermemory <value>
```

Example

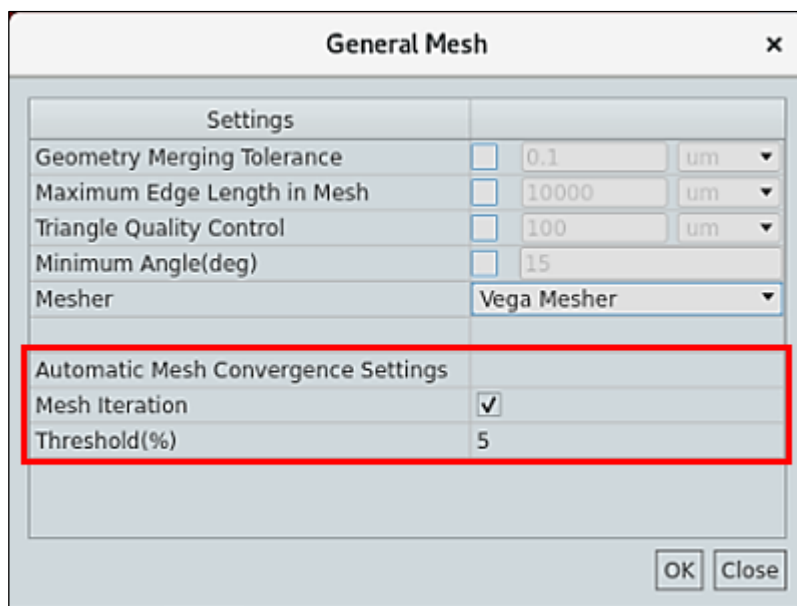
```
> analysis simulation control -name TI1 -hpcsetting -hpcsupporttype 4 -
hpcmodetype 1 -hpcschedulerconfigstatus 1 -hpcschedulercluster
testchip_1 -hpcenable 1 -hpcschedulermemory 100 -hpcschedulerntodes 1 -
hpcschedulerntasks 8
```

The options in Slurm are configured per node while the ones in LSF represent the whole job. If the memory setting is 100 GB, then Slurm requests 100 GB on every machine while LSF requests 100 GB in total irrespective of the number of machines used.

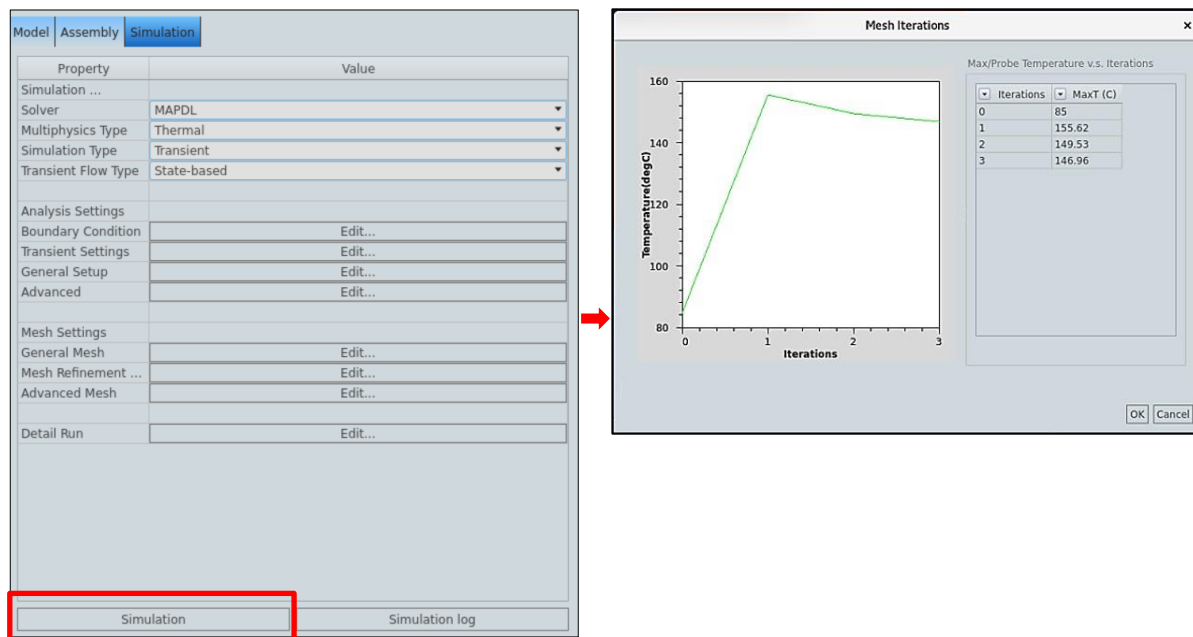
- **Automatic Mesh Convergence Flow**

Enhanced the tool to automatically calculate an initial mesh structure for user reference based on diverse 3DIC designs with power distribution. This results in a more stable simulation to reduce user setting steps before the simulation.

To use the automatic mesh convergence flow, select the **Mesh Iteration** option and define the **Threshold (%)** in the General Mesh window under **Simulation > General Mesh**. The tool determines the density of mesh nodes for simulation based on the value set in the Threshold (%).



After defining the Threshold (%), you can click the **Simulation** button to perform the mesh iterations-based simulation.



- **Assigning Via Material for Padstack in GDS**

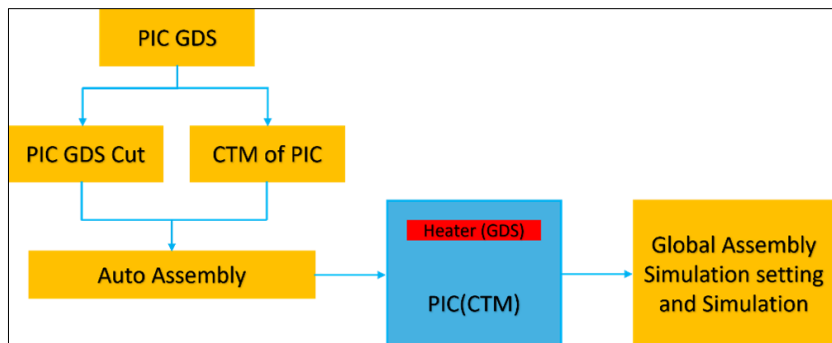
Added the following Tcl command for assigning via material for padstack in GDS Layout:

```
> layout setup padstack -name <Padstack Name> -viamaterial <material name> -model <model name>
```

- **3DIC Photonic Thermal Flow**

Enhanced the tool to support the detailed photonic integrated circuit (PIC) in thermal analysis. There are two parts of the 3DIC photonic thermal flow:

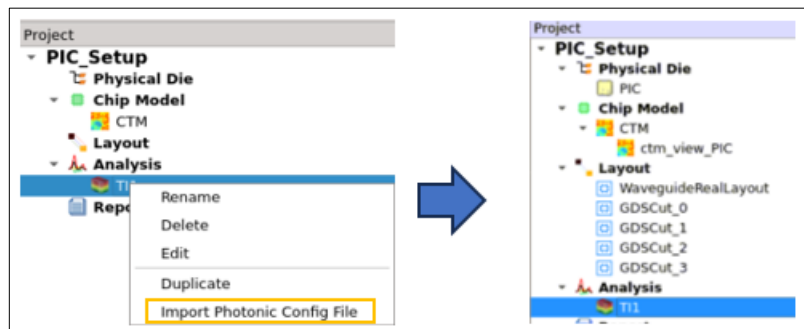
- **Heater of PIC:** Select the GDS section and cut the heater structure for detailed thermal modeling.
- **CTM of PIC:** Generates CTM for the rest of the structure in the PIC.



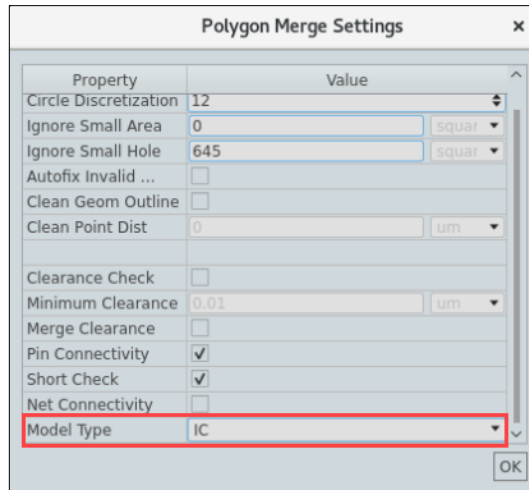
PIC Model Setup

To set the PIC model, perform the following steps:

1. **Define the PIC configuration file:** Create the photonic configuration file to assemble the models in a consolidated thermal model automatically. In the configuration file, define the following options:
 - PIC CTM: specify a PIC CTM model.
 - PIC GDS file: specify the full PIC GDS file.
 - Apache technology file: To import standard design information.
 - GDS Layer map file: specify GDS layer number to LEF layer name mapping.
 - Thermal Tech file: specify thermal material for the PIC model.
 - TOP CELL: specify the top cell name in GDS.
 - Selected Layer: specify the cut section.
 - Ring Layer: specify the ring layer name in GDS.
 - Marker Layer: specify the marker layer ID in GDS
 - WaveGuide GDSLayers: specify the waveguide layer information.
 - WaveGuideBooleanPattern: Boolean operations between the basic layers, and the different trench options defined in the thermal tech file.
2. **GUI Setup**
 - **Import PIC Configuration File:** Import the PIC configuration file using the **Import Photonic Config File** option from **Project > Analysis**. The Physical Die, CTM, and Layout models are created automatically.



- **Polygon Setting:** Select the layout Model Type as **IC** in the **Polygon Merge Settings** window.

**Tcl Command:**

```
> analysis setup importphotonic -name <model_name> -file
<PIC_config_file>
```

- **Simulation Setting:** Add the molding, heatsink, or PCB and specify the boundary conditions and mesh setup in the Simulation tab.
3. **Thermal Result:** After the simulation, you can view the temperature distribution of the PIC model using the **Simulation > 3D PostProcessing** option.

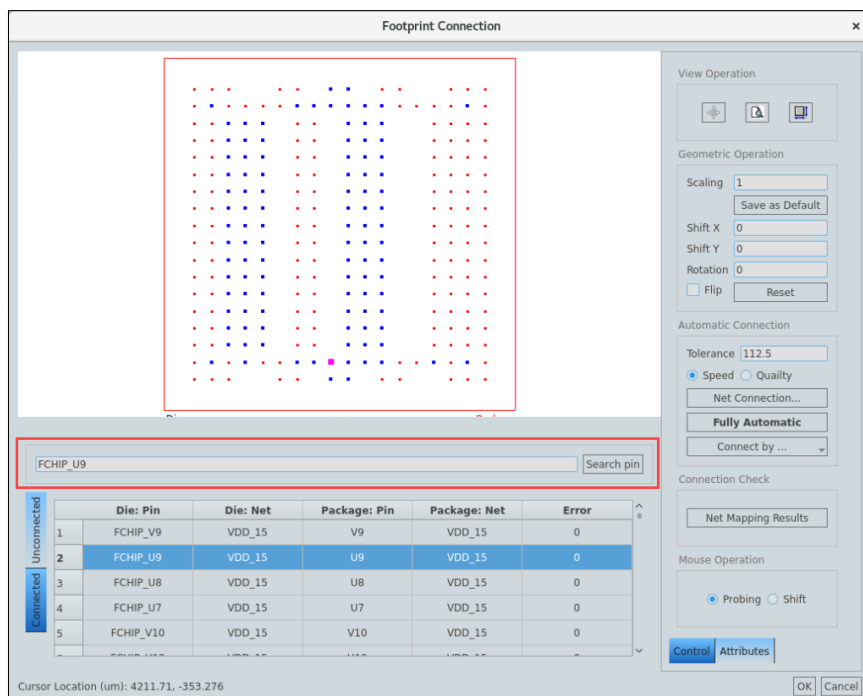
Setup3DIC

- **Reporting Interconnection Inside Chiplet**

Enhanced the tool to report an interconnection inside a chiplet to map a net name while converting from GDS to LEF or DEF format. The report is present in the `./<project name>/analysis/3DIC_CoWoS_L/output/` directory.

- **Search Bar in Footprint Connection Window**

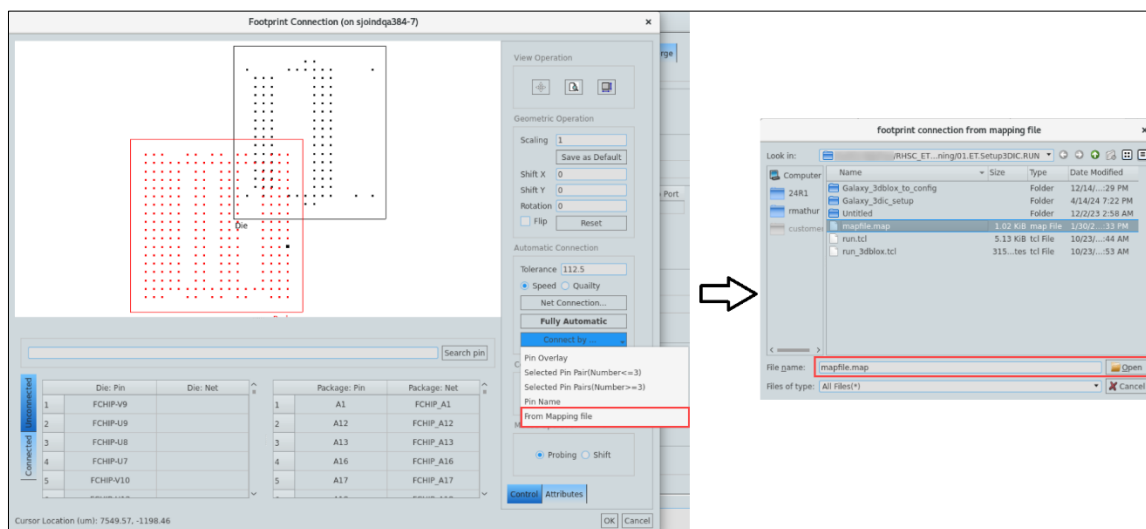
Added a search bar in the **Footprint Connection** window to search for a specific pin by its name. To search for a pin, enter the pin name in the search bar and press the enter key or click the **Search pin** button to initiate the search. If an exactly matched pin name in the connection result is found, the pin is highlighted in the connection table.



Note: The search bar supports case-insensitive exact match, that is, the search returns only one match result. Search for a partial match or fuzzy search is not supported.

- **Mapping File to Map Die Ploc Name to the Package Pin Name**

You can now import a file to map the die ploc name to the package pin name during the footprint connection. To import the mapping file, select **From Mapping File** in the **Connect by** drop-down list of the **Footprint Connection** window and load the mapping file.

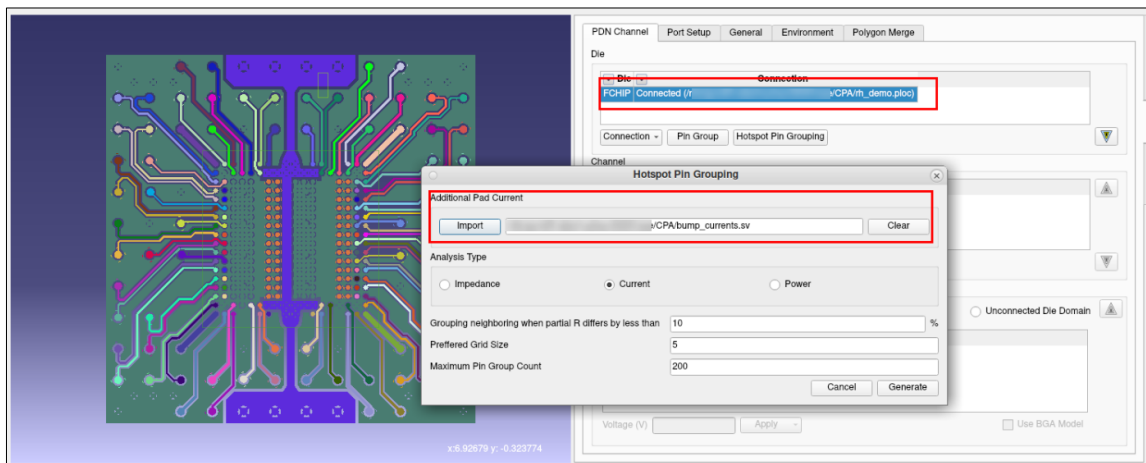


Chip Package Analysis (CPA) Flow

- **Supporting Pad Current File in Current and Power Pin Grouping Extraction**

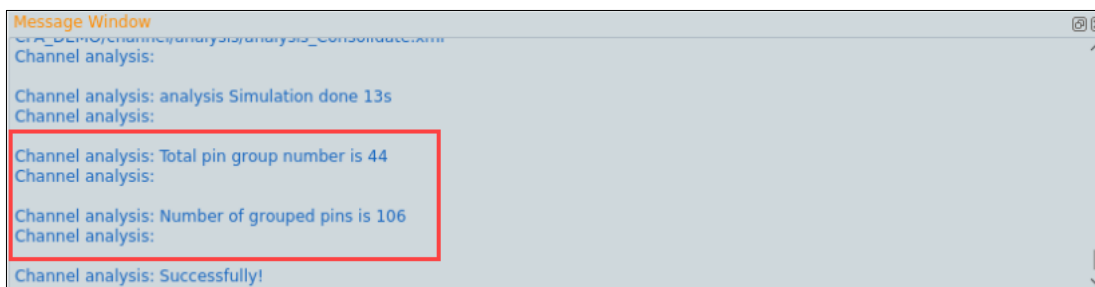
Enhanced the tool to support pad current file generated by RedHawk-SC to perform current or power-based smart grouping for package extraction. You can import the pad current file from the **Hotspot Pin Grouping** dialog as shown in the following figure.

Note: You must provide the ploc file together with the pad current file to perform the current or power-based smart grouping.



- **Reporting Smart Grouping Result**

The tool now prints a summary of pin grouping results in the **Message Window** after smart grouping. This summary consists of the highlighted information:



Signal/Power Integrity Flow

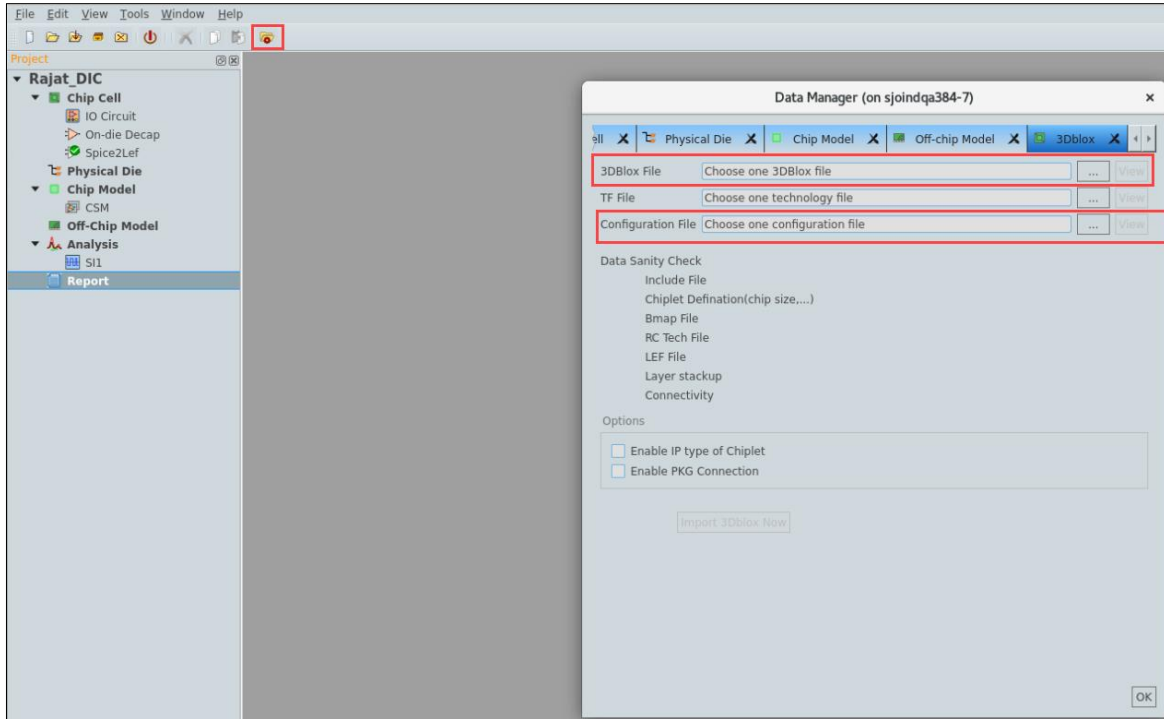
- **3Dblox Support in PI Flow**

Enhanced the tool to support 3Dblox in Signal/Power Integrity (SI/PI) flow. The 3DbloxPI flow needs the 3Dblox file (.3dbx) and configuration file (config.txt). The table shows the input data required in the 3Dblox and configuration files:

Function	Input Data	File
Die	CPM	Configuration file
Channel Model	GDS	3Dblox
	Apache technology file	3Dblox
	Layer mapping file	Configuration file

	Nets for analysis	Configuration file
	Pin grouping	Configuration file
	Voltage source setting	Configuration file
Connection	-	3Dblox

To enable the 3Dblox PI flow, set the environment variable `PISIFLOW` to 1 and import the 3Dblox and configuration file under the **3Dblox** tab of the **Data Manager** dialog box.



Note: To use the RedHawk GDS to DEF conversion, set the environment variable `ET_PISIFLOW_RHGDS2DEF` to 1.

Issues Resolved

Thermal Integrity Flow

- Fixed an issue where the tool displayed an incorrect power block shape when the 3Dblox2.0 Feasibility database was imported.
- Fixed the inconsistent metal density map size that occurred during a change in layer selection.
- Fixed an issue where the Z height calculation for a region was incorrect in 3Dblox 2.5.

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