Application Note

Interposer Extraction for Signal/Power Integrity

VERSION: 2024R1.0

Outline

The size of Interposer becomes large year-over-year as technology evolves. The legacy RedHawk extraction engine integrated in RedHawk-SC Electrothermal is motivated for scalability improvement to handle large interposer for 3D-IC power integrity analysis. This application note introduces a new RedHawk-SC Electrothermal flow to employ RHSC engine for interposer extraction with exceptional performance and capacity.

The new Ansys RedHawk-SC Electrothermal (RH-SC ET) flow for interposer extraction features:

1) GDS Conversion to convert GDS file to DEF/LEF file.
2) Chip-level frequency-dependent RLCG parasitic generation
3) Support TSV (through-silicon via) and eDTC (embedded deep trench capacitor) spice model.

The details of the flow usage are described below.

Usage

Tool Version and License

1. Tool Version
   RedHawk-SC Electrothermal v2024R1.0
2. License
   redhawk_sc_et_beta_a + redhawk_csm/redhawk_sc_electrothermal + 3 redhawk_sc_token + redhawk_chip_power_model

New a project

1. Open RHSC-ET by command “redhawk_sc_et -3dic”.
2. Click **File** --> **New** and select “**Signal/Power Integrity**” to create a new project.

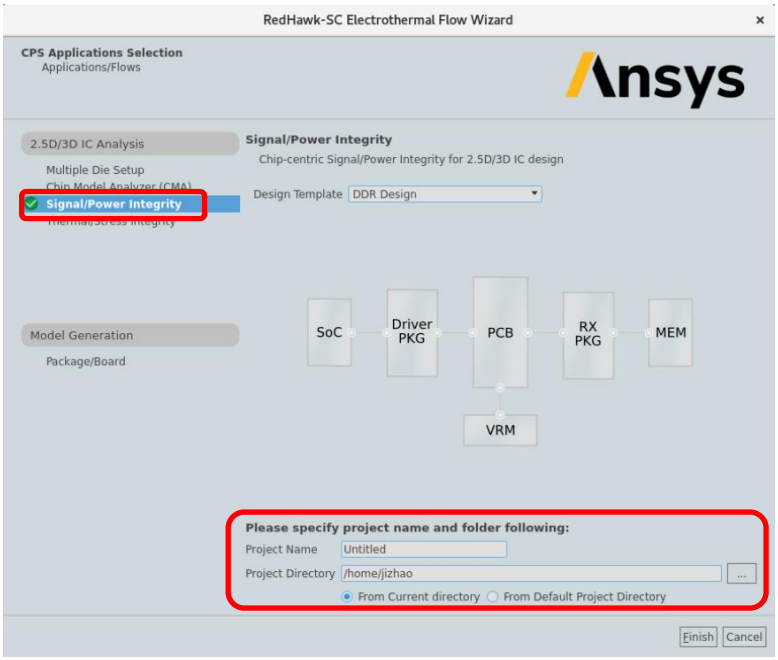

Figure 1 – New a Project

RedHawk-SC Root and Worker Setting

1. Click **Tools** -> **Simulators** to open **Simulator Path** setting dialog.

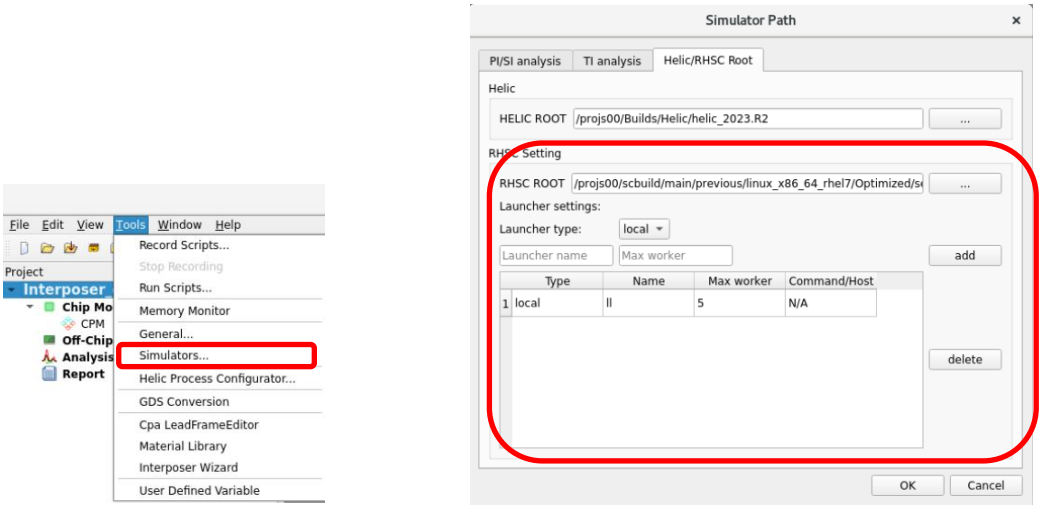

Figure 2 – Set Simulator Path

2. RHSC ROOT Setting
   Need to use RedHawk-SC v2023R2.2 and later versions.
3. Launcher Setting
   3 types of setting support as RHSC: local, ssh and grid.
   local: Add Launcher name and Max worker, then click **add** button.

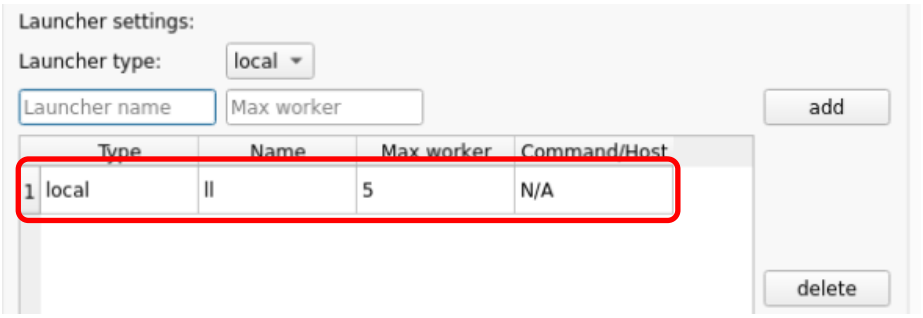

Figure 3 – Launcher Setting 1

ssh: In an SSH-based launcher, the workers are directly launched on the execution hosts with SSH protocol instead of relying on the compute cluster to manage and launch jobs.

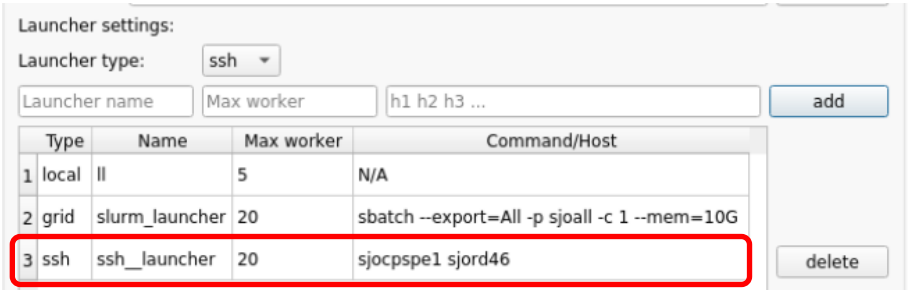

Figure 4 – Launch Setting 2

grid: The grid type is a general command to define launchers for any custom grid depending on the argument that you provide.

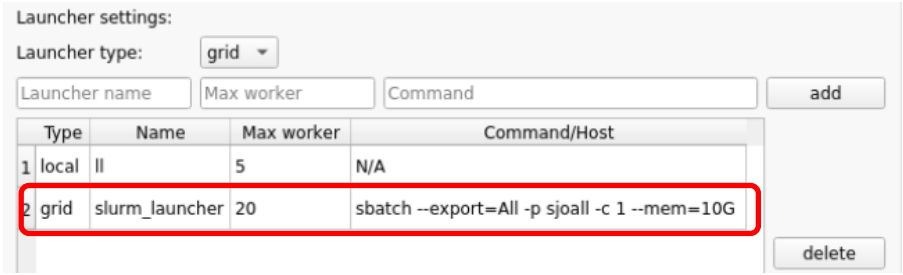

Figure 5 – Launch Setting 3

Interposer Extraction

1. Click **Tools** -> **Interposer Wizard** to open Interposer Wizard dialog.

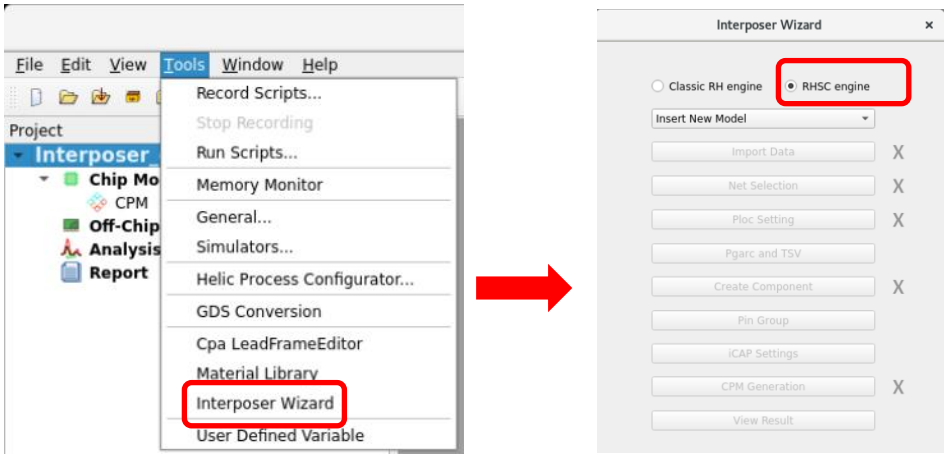

Figure 6 – Interposer Wizard

2. Double click **Insert New Model** to open **Die Selection** dialog, then click Insert a **New Die** to add a new die.

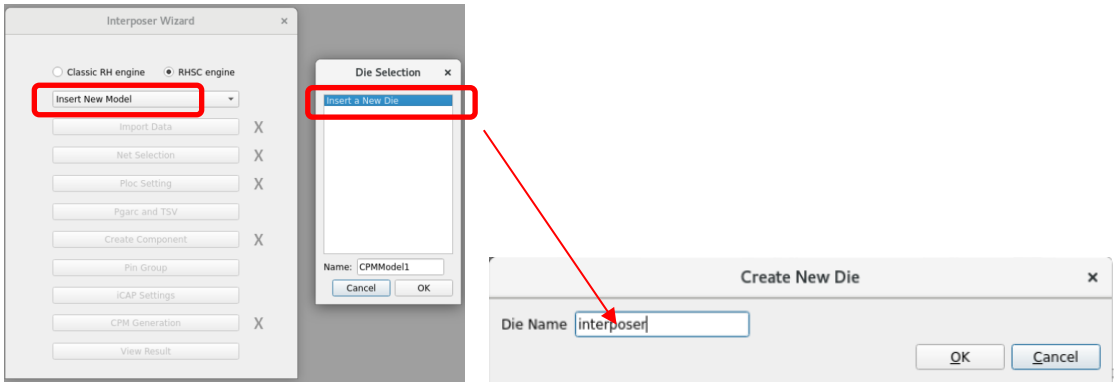

Figure 7 – Create New Interposer

3. In the **Die Design Data** dialog, the input can be either DEF/LEF or GDS.
   If design data is DEF/LEF, user needs to import Apache Tech File/DEF files/LEF files.
   If design data is GDS, user needs to click **Translate GDS** to convert GDS to DEF/LEF first.

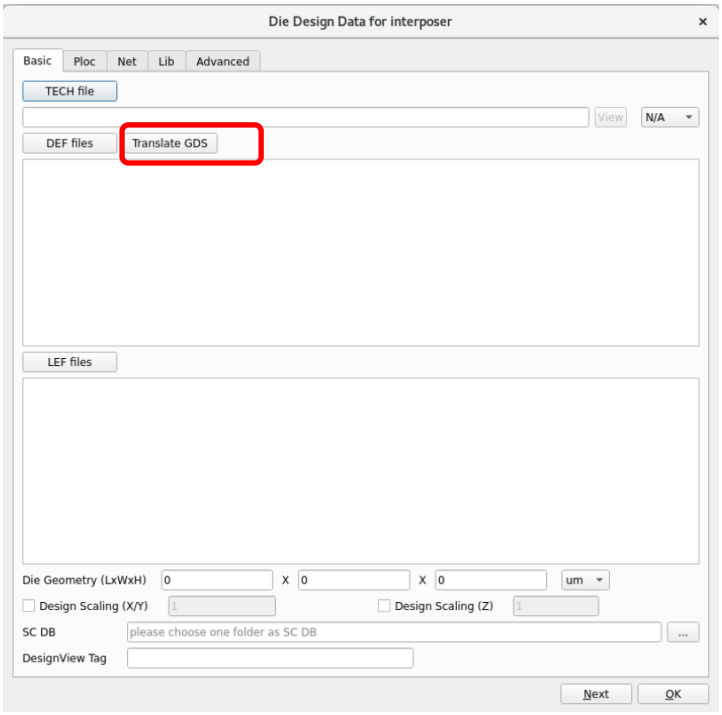

Figure 8 – Translate GDS

4. Translate GDS: Configuration
   1) Import GDS file, Apache Tech file and Layer map file.
      The layer map file format is as bellow.
      <Layer_name> <Layer_type> <Layer_num: datatype_number > <Text_layer_num: datatype_number >

I_MB	m	17:0	-
I_TSV1	v	18:0	-
I_M1	m	19:0	-
I_V1	v	21:0	-
I_M2	m	20:0	-
I_V2	v	25:0	-
I_M3	m	30:0	-
I_V3	v	35:0	-
I_M4	m	40:0	-
I_V4	v	45:0	-
I_M5	m	50:0	-
I_V5	v	55:0	-
I_M6	m	60:0	60:0

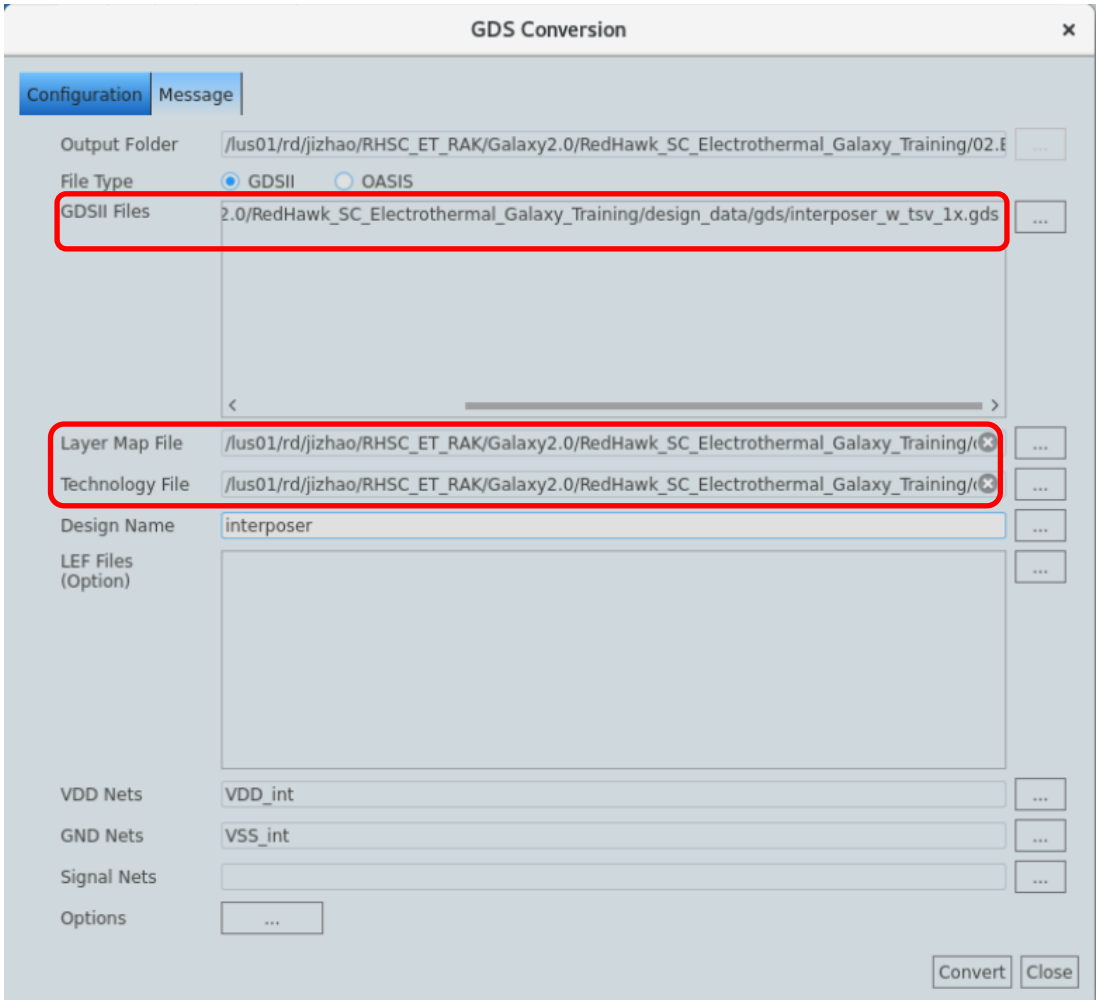

Figure 9 – GDS Conversion Settings

2) Select the top cell as design name for def.

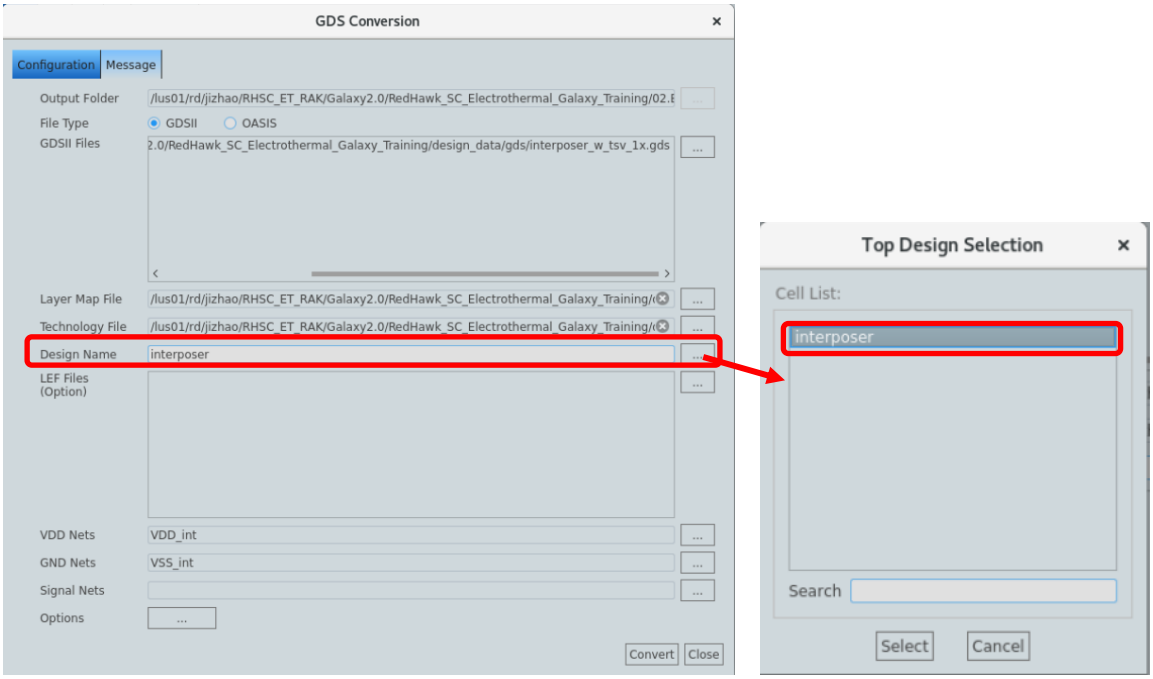

Figure 10 – Set Top Cell

3) Specify VDD/GND nets.
   a. Add a def net name which will be written to def file.
   b. Select the GDS net to be extracted.

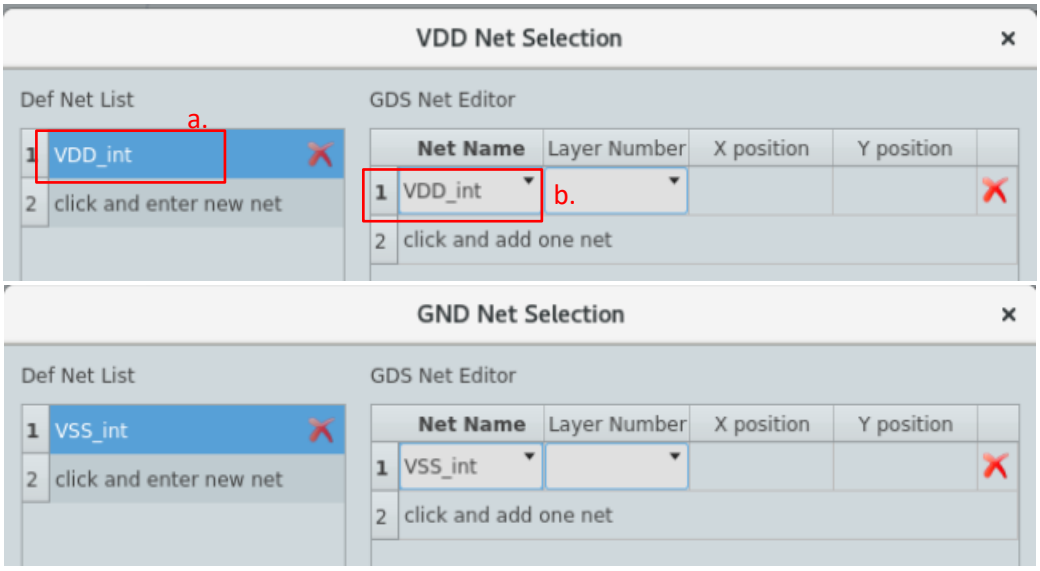

Figure 11 – Specify VDD and GND Nets

4) Other options setting.
   Use the default setting. Users can also select other options needed.
   Extraction starting layer: Sets the lowest starting layer for extraction and tracing. The default is to trace and extract all the layers specified in the layer map file.
   Extract from top level Text Only: When selected, only the text in the top cell is extracted and used for power/ground net which is defined in VDD_NETS and GND_NETS.

Disable net name case sensitive: Turns the search of text layer case insensitive. By default, text label name searching is case sensitive.

Disable MINLVS: If you cannot provide all device layers, such as p-well, n-well, p-diffusion, n-diffusion, poly and contact layer, in the GDS layer map file, this keyword must be set to 1 to disable the LVS features, such as tap contact recognition, device contact array extraction and modeling. Otherwise, GDS2DB aborts with an error. Layers below M1 are ignored when this keyword is set, thus improving run-time and memory footprint.

Merge Circular Vias: When set, large circular vias are merged into a single via, rather than split into segments.

Compress the generated DEF file: Performs a gzip on the output DEF file. When this keyword is turned on, the output DEF file is gzipped and given the filename.def.gz.

Generate PLOC: When specified, GDS2RH creates pads in the PINS section of the DEF file it creates. The locations where these pads are created depends on the option specified. USE_TEXT_LABEL: generates plocs at the location of text labels.

USE_LEF_PINS: generates plocs that have the same size and position as all pin geometries that are present in the input LEF.

USE_PIN_LAYERS: generates plocs that have the same size and location as all metal geometries.

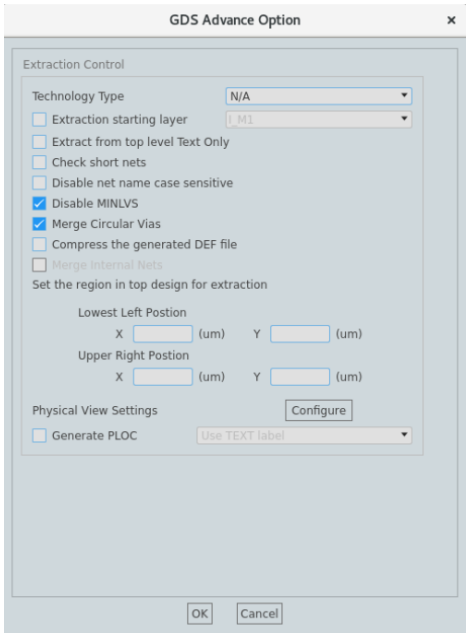

Figure 12 – GDS Advance Option

5) Click **Convert** to do the conversion.

5. Setup design data.

After **Translate GDS**, Tech/LEF/DEF file will be added automatically. User also can,

1) Input Technology file (support both encrypted and unencrypted file) and select the process <7/10/14/16/20nm>
2) Input DEF files and set one file as TOP DEF by right clicking the file.
3) Input LEF files and set one file as technology lef by right click the file.
4) User can also set design scaling, the value should bigger than 0.

Then click **OK**. In the opened dialog to select the die and based on this die to create a new CPM model.

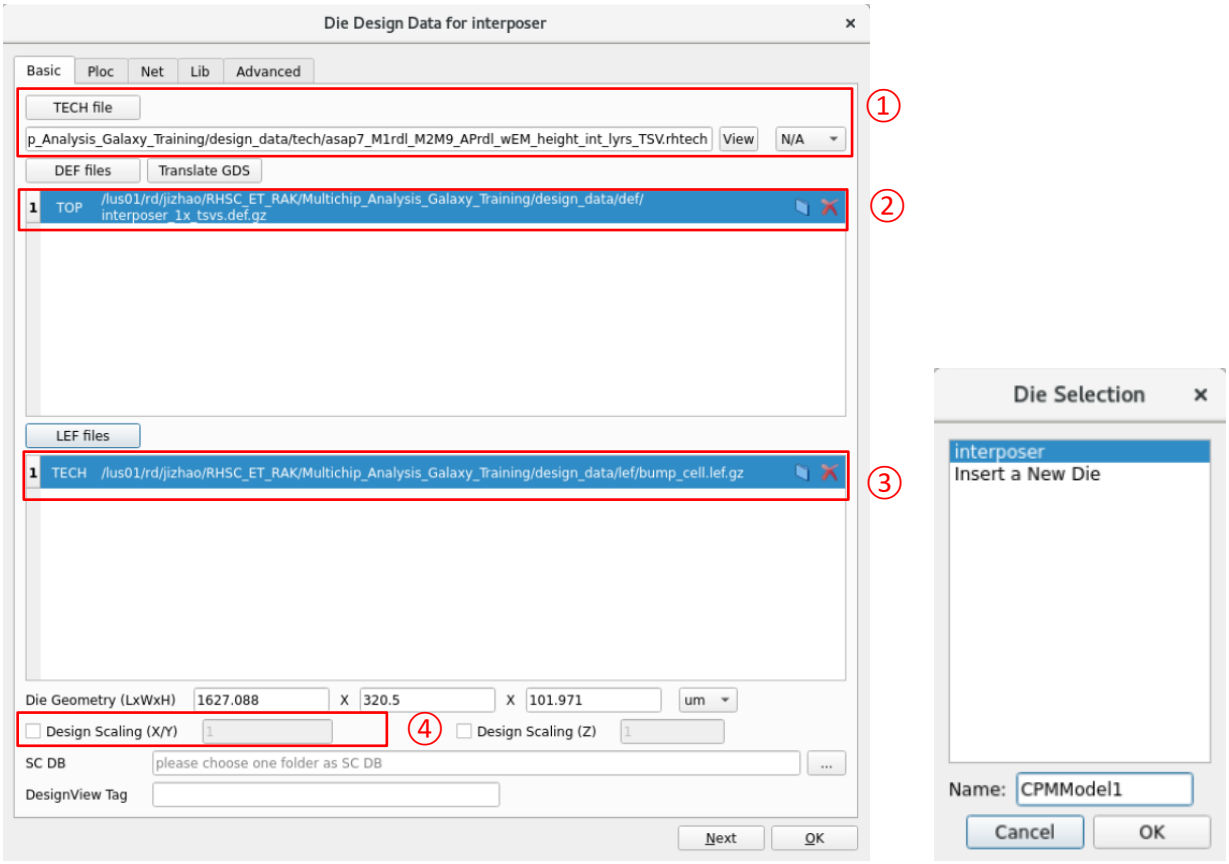

Figure 13 – Design Data for Interposer

6. Select nets to be extracted.
   Select PG nets, then click **OK**.

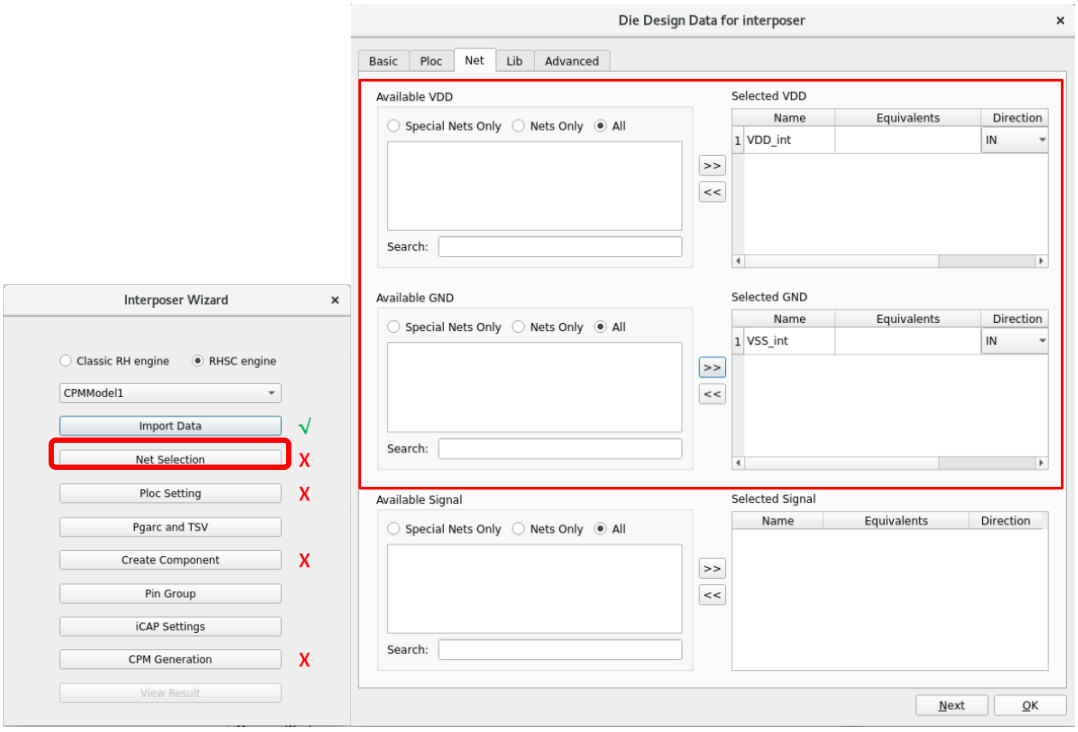

Figure 14 – Net Selection

7. Pad/bump setting

   Click **Ploc Setting** to set ploc. Specify in ploc file and then import ploc file directly. Users can add 1 or more ploc files.

   File name: xxxxx.ploc

#pad name	*#xy-coordinate*		*#layer*	*#net name*
Bump_1_9_10	1576.745	851.610	UBM	VDD
Bump_1_9_11	1526.745	851.610	UBM	VSS
PAD81	1622.500	409.000	C4	VDD
PAD82	1262.500	229.000	C4	VSS
PAD83	1442.500	949.000	C4	VSS

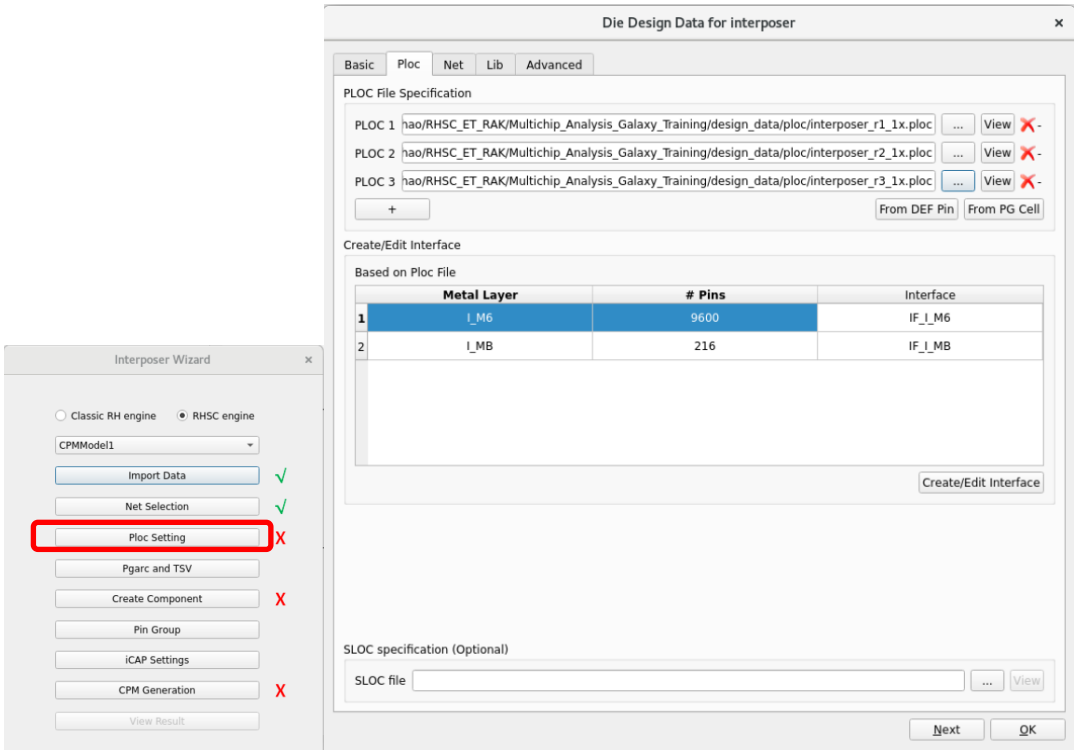

Figure 15 – PLOC Setting

8. Pgarc and TSV

1) Pgarc is to define PG pins in pairs.

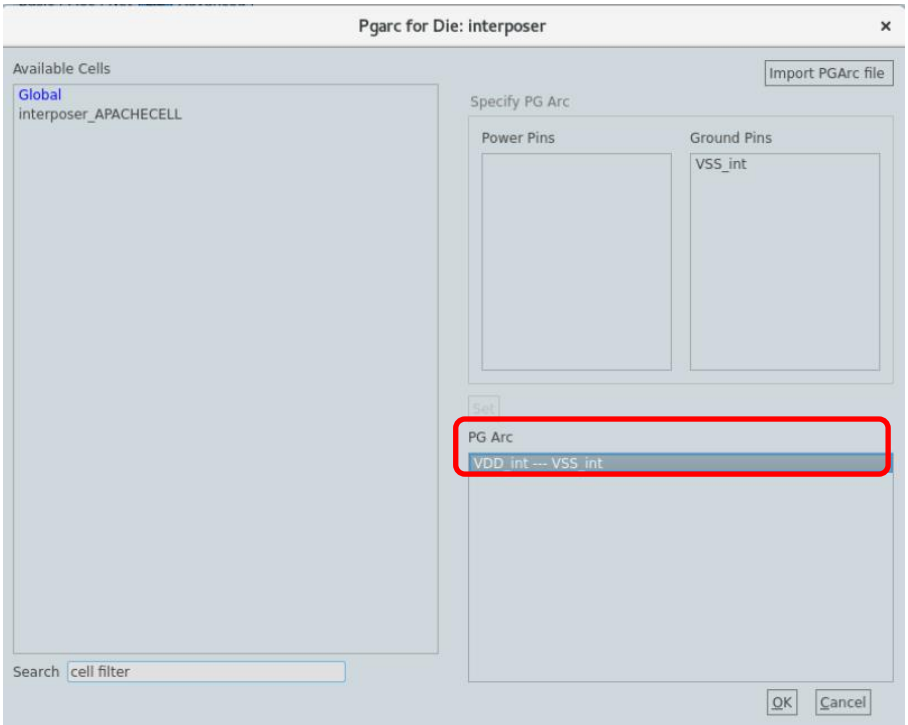

Figure 16 – Pgar Setting

2) User can include TSV models,

TSV subckt model defined by other companys. User should select the subckt name and TSV Layer Name. TSV Coupling: consider the couple C between TSV branches. This information should be specified in the Technology file. (From TSMC)

The TSV model format should be as below, the subckt node should be top and bottom.

```
.subckt tsv_rc top   bottom
      r1    top   n2      0.042
      r2    n2    bottom  0.042
      C     n2    0       1.048E-13
.ends
```

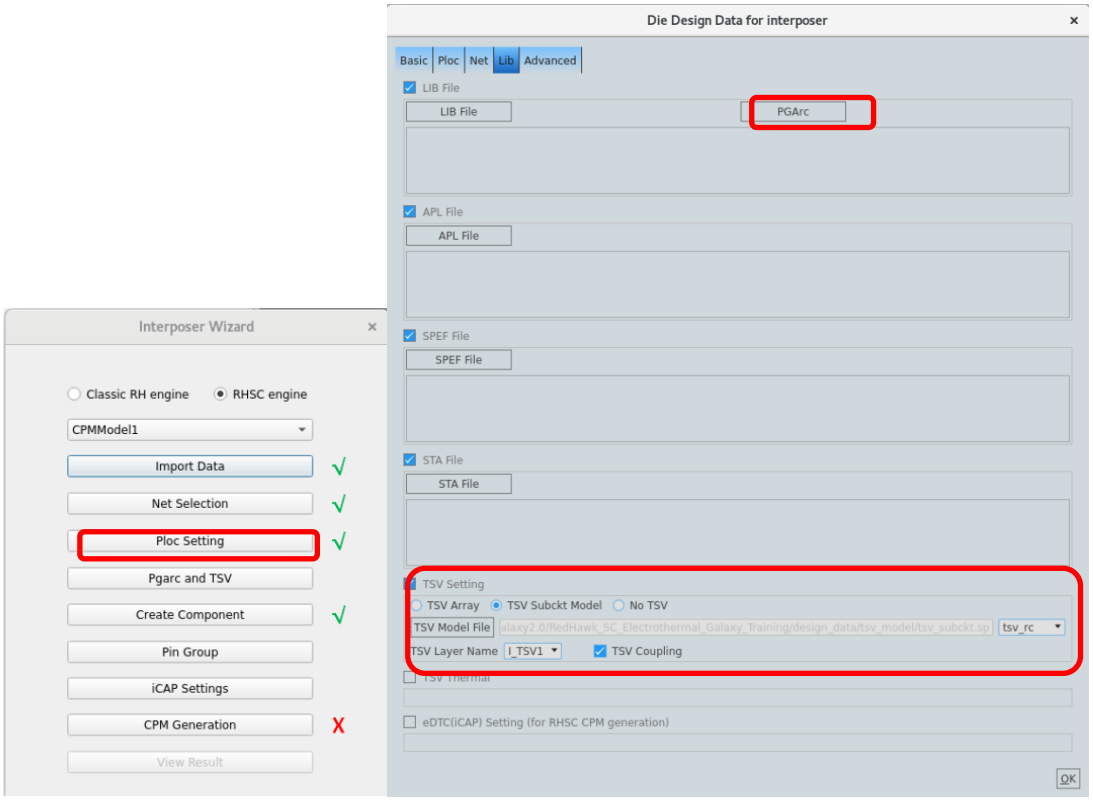

Figure 17 – TSV Option

9. Create components.

   Tool has created components according to layers. If there are multiple components in one layer, the user needs to create manually.

   Box select pins from GUI and enter the Interface name, then create a new interface.

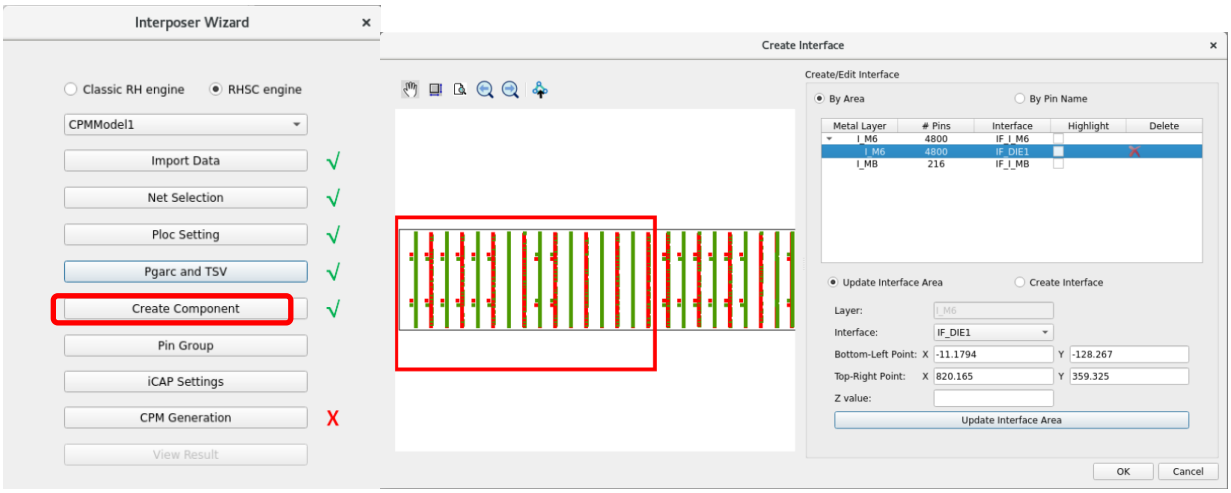

Figure 18 – Create Component

10. Do pin group for each component.
    1) Select component.
    2) Select net.
    3) Select pins to be grouped from layout or pin list.
    4) Enter group name and click “Group” to finish pin group.

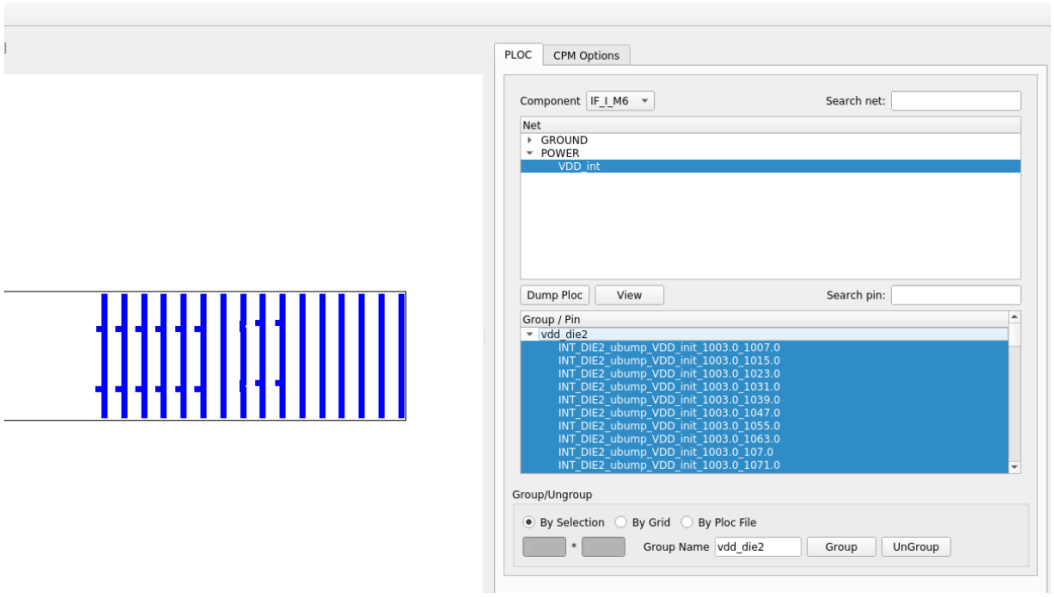

Figure 19 – Pin Group Setting

11. iCAP Setting

    If there is eDTC inside the interposer design, then user can add.

    From RHSC v2023R2.1.P1, we support spice model directly. So, recommend users to use **eDTC Spice Model**.

    Design Cell Name: eDTC cell name in DEF/LEF

    Model Name: spice model subckt name

Corner: Corner defined in spice model

Model Type: capacitance

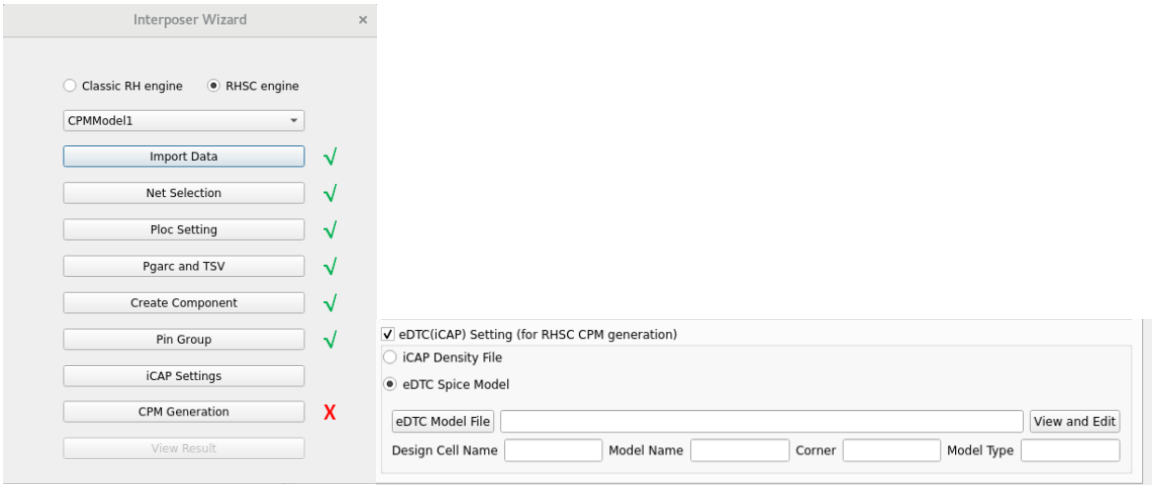

Figure 20 – iCPA Setting

12. CPM Generation
    1) Select CPM mode, Flat CPM or Distributed CPM.
        a) Flat CPM mode: Only use 1 worker.
        b) Distributed CPM mode: Use multiple workers.
    2) Specify the extraction temperature and extraction type, select RLC will include inductance.
    3) Sampling type and frequency setting.
    4) Add CPM config, supply an additional options file (used by the reduction engine APM).
    5) Generic RHSC settings, Any RHSC View settings can be provided.

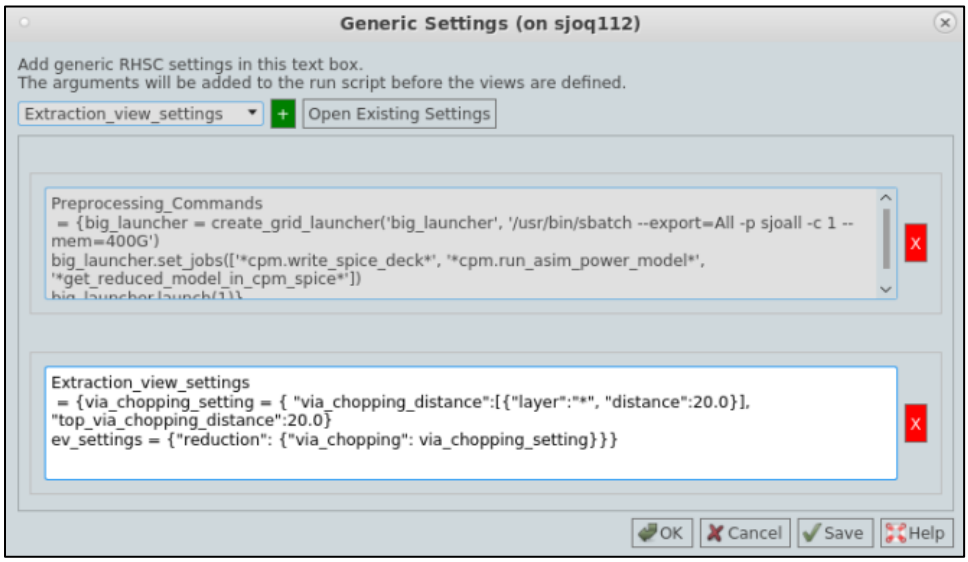

Figure 21 – RHSC Setting

    6) Then the user can click **Generate CPM** to generate the spice model.

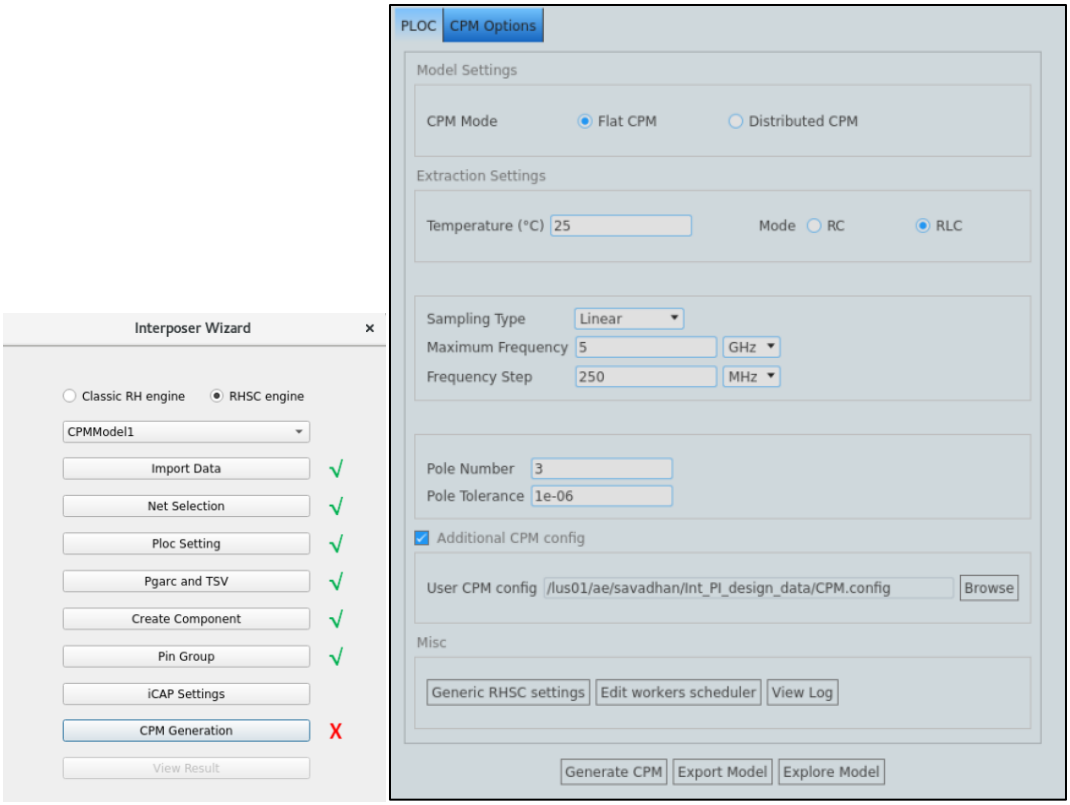

Figure 22 – CPM Options

13. Impedance Check

    User also can check impedance, Reff, Leff, Ceff each port pair.

    1) Create ports.
    2) User can also group all pg pins and auto generate ports, in this case, ports only created for same nets.
    3) Frequency sweep setting
    4) Run simulation.
    5) Show results.

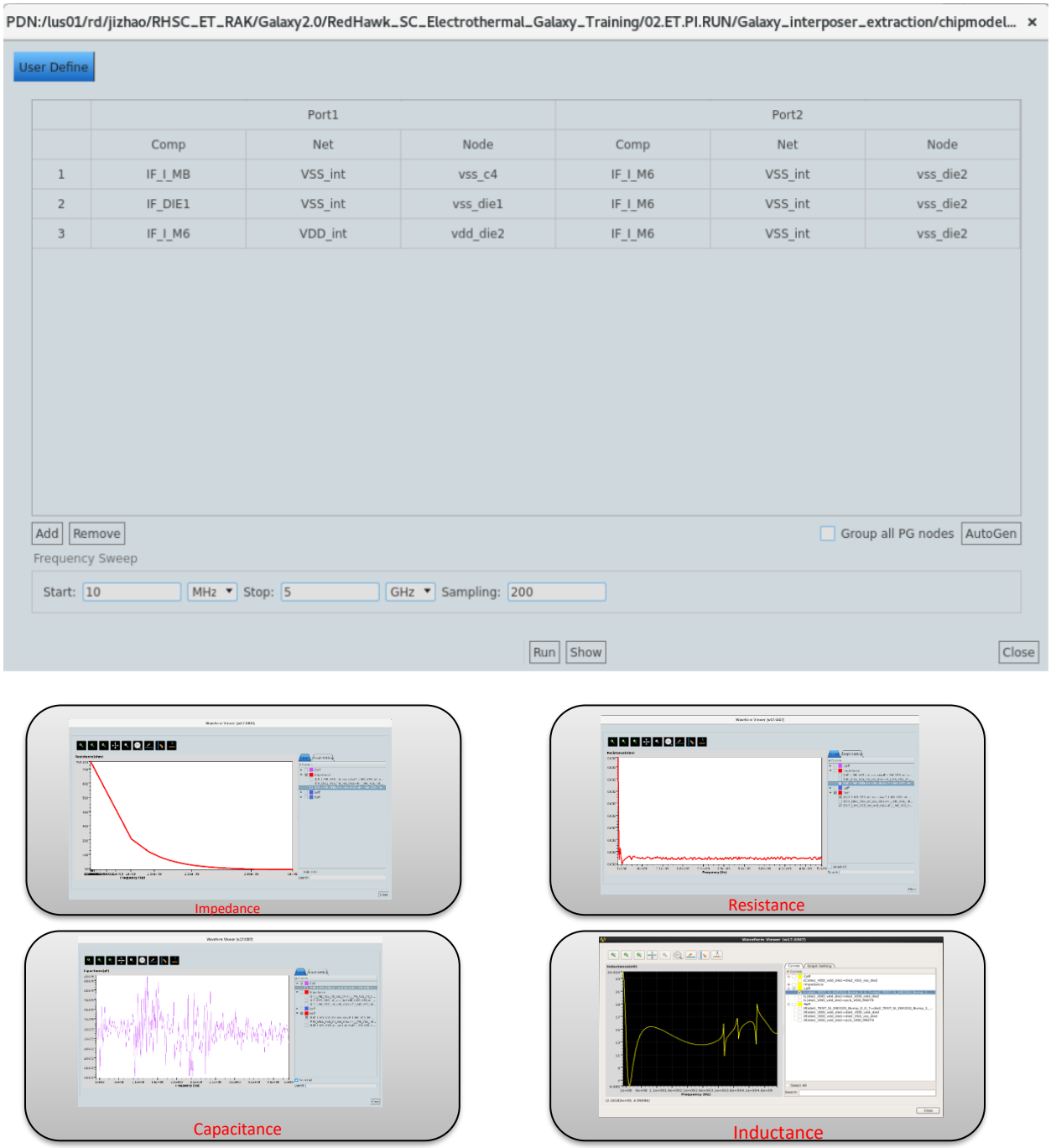

Figure 23 – Extraction Result