Linfang Zheng

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Profile

A highly motivated Ph.D. researcher specialises in computer vision, deep learning, and robotics, with expertise in visual 6D object pose estimation and tracking. Demonstrates a strong aptitude for quickly comprehending complex concepts and exhibits excellent collaboration and problem-solving skills.

Education

Ph.D. in University of Birmingham (UoB) **01/2020 – Expected Graduation: 07/2024**
Computer Science | Supervisors: Aleš Leonardis, Hyungjin Chang

Ph.D. in Southern University of Science and Technology (SUSTech) **04/2021 – 04/2024**
Visiting Student | Control and Learning for Robotics and Autonomy (CLEAR) Lab | Supervisor: Wei Zhang

Master in Harbin Institute of Technology (HIT) **08/2015 – 07/2017**
Integrated Circuit Engineering | Outstanding Master's Graduate

Bachelor in Harbin Institute of Technology (HIT) **08/2011 – 07/2015**
Electronic Information Science and Technology | Direct Admission to Graduate School

Research Experience

Category-level Articulated Object Pose Estimation | UoB **01/2024 – 03/2024**

- Submitted to **ECCV 2024** (co-author). Under review.

Cloth Pushing via Trajectory and Contact Pose Optimisation | SUSTech **12/2023 – 03/2024**

- Submitted to **IROS 2024** (co-author). Under review.

Category-level 6D Object Pose Refinement | UoB & SUSTech **03/2023 – 11/2023**

- Developed an object pose refinement algorithm, resolving challenges in geometric discrepancies among category-level objects.
- Significantly enhanced category-level object pose estimation performance, surpassing current state-of-the-art methods with substantial performance advantages.
- Accepted by **CVPR 2024** (first author).
- Paper: GeoReF: Geometric Alignment Across Shape Variation for Category-level Object Pose Refinement

Visual Planar Region Extraction for Uneven Terrains | SUSTech **11/2022 – 09/2023**

- Collaboratively Introduced a multi-resolution planer region extraction strategy for uneven terrains from point cloud data. Contributed to designing deep learning-based plane segmentation.
- Accepted by **ICRA 2024** (co-author).
- Paper: Multi-Resolution Planar Region Extraction for Uneven Terrains

Category-level Object Pose Estimation | UoB & SUSTech **08/2022 – 05/2023**

- Proposed a real-time and outlier-robust hybrid-scope feature extraction network, substantially enhancing category-level pose estimation performance, **notably enhancing the** $5^{\circ}2$**cm metric by 14.5%.**
- Introduced a network facilitating joint extraction of local-global geometric structure features, enhancing pose estimation for complex-shaped objects.
- Published in **CVPR 2023** (first author).

- Paper: HS-Pose: Hybrid Scope Feature Extraction for Category-Level Object Pose Estimation

3D Joint Gaze Estimation | UoB **01/2022 – 04/2023**

- Collaboratively introduced a cutting-edge depth-aware joint attention estimation framework, surpassing current benchmarks.
- Addressed the previously unexplored problem of integrating a depth prior and a 3D joint field-of-view probability map to estimate attention targets in a scene.
- Published in **CVPR Workshop 2023** (co-author).
- Paper: Where are They Looking in 3D Space

Instance-level 6D Object Pose Tracking | UoB & SUSTech **02/ 2020 – 03/2022**

- Introduced the first neural network-based prior pose generation scheme using object pose history to forecast future poses effectively.
- Developed a real-time temporally-primed pose estimation architecture, proficient in handling occlusions for textureless and symmetric objects.
- Published in **ICRA 2022** (first author).
- Paper: TP-AE: Temporally Primed 6D Object Pose Tracking with Auto-Encoders

Instance-level Object Pose Estimation and Refinement | UoB **08/2022 – 03/2022**

- Collaboratively introduced a Transformer-based network, leveraging global feature correlation to enhance object pose estimation performance.
- Published in **ECCV Workshop 2022** (co-author).

  Paper: Trans6D: Transformer-Based 6D Object Pose Estimation and Refinement

Reinforcement Q-Learning for Switched Linear Systems | SUSTech **05/2019 – 12/2019**

- Collaboratively proposed an algorithm with a carefully designed parametric approximator that respects the analytical structure of the exact Q-function, paired with an associate parameter training algorithm.
- Published in American Control Conference **ACC 2020** (co-author).
- Paper: Optimal Control Inspired Q-Learning for Switched Linear Systems

Work Experience

SUSTech | Prof. Wei Zhang's CLEAR Lab | Research Assistant **03/2019 – 01/2020**

- Assisted in project and research work including embedded software and hardware design, algorithm implementation, and project proposal writing.
- Participated in research on reinforcement learning based on optimal control, resulting in publication at ACC 2020.

DJI | Hardware Department | Embedded Hardware Engineer **07/2017 – 03/2019**

- Evaluated the rationality of electronic component selection in the company's embedded hardware circuit design, enhancing design efficiency.
- Managed arrangements and follow-ups for electronic component performance verification, improving the stability of the electronic component supply chain.
- Achieved cost savings for the company through optimised electronic component selection, receiving recognition and rewards.

Internship at DJI | RM Department | Embedded Hardware Engineer. **07/2016 – 09/2016**

- Supported Robomasters competition field hardware circuit-related tasks and summer camp activities.

Awards

- Outstanding Master's Graduate, HIT, China, 2017
- Silver Award for Outstanding Master's Thesis, HIT, China, 2017
- First Prize Scholarship, HIT, China, 2011-2017
- Second Prize in the Technology Innovation and Entrepreneurship Training Program, HIT, China, 2014
- Second Prize in the First Physics Academic Competition, HIT, China, 2014
- Second Prize Scholarship, People's Daily (People.cn), China, 2014

Skills

- Language: English (IELTS 6.5), Mandarin (Mother Language)
- Programming Languages: Python, C, Verilog
- Deep Learning: PyTorch, TensorFlow
- Mandarin: Mother Language
- Hardware Design: Embedded Hardware Design, Integrated Circuits, FPGA
- Embedded Software Design