Analysis in VeGen

1 Consecutive Check

Whether load or store instructions touch consecutive addresses is important for vector memory instruction generation. Determining whether two instructions touch consecutive memory should be easy for hardware, but not for software. This is because the address may not be computable, and is often not computable at compile time. Additionally, load and store instructions may be in different basic blocks. Therefore, a non-trivial analysis is needed.

1.1 findConsecutiveAccesses

1.2 isConsecutive

1.3 isEquivalent

2 Control Dependence

Control dependence analysis is a key technique in VLoop, as it appears 24 times in the VLoop. It has various applications, such as computing the incoming conditions for phi nodes, assigning conditions to instructions within a block, finding the condition for taking the backedge versus exiting the loop, determining the feasibility of loop fusion, and performing coiteration (which seems to be a novel contribution of VeGen).

2.1 getConditionForBlock

2.2 getConditionForEdge

3 Global Dependence Analysis

Global dependence analysis is only used in the vector packer to determine whether a vector pack is valid and feasible.

3.1 getDepended